1961 Solid - State Circuits Conf.

# 1961 INTERNATIONAL

# SOLID-STATE CIRCUITS CONFERENCE

# DIGEST of TECHNICAL PAPERS



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# 1961 International Solid-State Circuits Conference

## DIGEST OF TECHNICAL PAPERS



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# Foreword

IN A RAPIDLY-EXPANDING TECHNOLOGY—as solid-state electronics—there is a sweeping obligation to provide a dynamic forum to explore the latest developments in circuitry and applications.

Each year — since 1954 — this challenge has been met in timely conferences, held on the campus of the University of Pennsylvania, covering broad advancements in the field.

Originating as a meeting devoted to transistors only, programs have been constantly enlarged — as progress dictated — to include other areas, until three years ago, the *Solid-State Circuits Conference* identity was adopted. And, last year, in a continuing drive to mirror exciting world-wide activities in the art, the international theme was added, attracting a number of distinguished speakers from abroad.

Maintaining this spirited interest, the 1961 program committee has fashioned a topical 51-paper meeting — with 12 informal sessions — accenting the most recent accomplishments in this country and overseas.

It is hoped that all of the talks — and the evening discussions — will be of significant value to device and circuit physicists and engineers working on assorted problems in solid-state electronics, and, as in the past, the conference will provide leadership in the field.

***Tudor R. Finch***
***Conference Chairman***

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## SESSION I: New Device Characteristics

Chairman: E. O. Johnsen
RCA, Somerville, N. J.

### 1.1: A Survey of the Tunnel-Diode Equivalent Circuit

E. Baldinger

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Basel, Switzerland

THE DC CHARACTERISTIC of tunnel diodes (Figure 1) may be explained by splitting up the total current into three fractions; Figure 2. Electrons pass the junction from the valence band of the *n*-region (*Zener* current) and in reverse direction (*Esaki* current). At a high enough forward bias, minority carrier injection will be appreciable[3]. This current may be proportional to $\Sigma\ ^{qV/kT}$ provided the influence of recombination centers in the depletion layer can be neglected. Irradiation by fast neutrons will increase the number of recombination centers and will therefore increase the valley current[2]. It will also be noted that the tunneling process (*1* and *2* in Figure 2) is complicated by phonon interaction and by states for electrons within the forbidden gap[3,1].

#### *Small Signal Equivalent Circuit*

Since we are interested in switching speed and high-frequency performance, we shall discuss the small signal equivalent circuit. The circuit shown in Figure 3 may be considered as a very useful first order approximation. Only one lumped parameter for the electric field, the magnetic field, the losses in the *leads* and the negative characteristic is introduced. It has to be noted nevertheless that this circuit does not take account of minority carrier storage effects, which would modulate the conductivity of the regions near the junction[4]. Since this means a change of the small lead resistance $r$, only this is not important for switching applications. However, for a detailed discussion and precise interpretation of measured parameters this effect deserves consideration.

The charge stored in the junction will determine precision and speed of fast amplitude discriminators. A typical response to a current pulse just exceeding the peak current is shown in Figure 4. This behavior can be explained by the equivalent circuit (Figure 3) and the variation of the parameters with voltage, especially $R$; Figure 6.

The bridge represented in Figure 5 ($R_1$ $R_2$ $R_3$ $R_4$) permits one to trace the dc characteristic. With an additional low-frequency oscillator, the differential value

$$r + R = \partial V / \partial I = f\ (V)$$

can be measured for any point of operation. Stable operation (no oscillations) is assured when $R_2 < R$ and $L_{total} < rRC$. The voltage $V_2$ is proportional to the diode current. A suitable extrapolation of the measured value $(r + R)$ yields the resistance $r$; Figure 6.

#### *L-C Analysis*

To determine $L$ and $C$ an *hf*-bridge may be used[5]. In the region of the negative slope an alternative method is feasible. One may adjust the short circuit stub in Figure 5 to the critical position where oscillation just starts. The frequency of oscillation and the associated critical value of inductance of the short circuited line permit the determination of $L$ and $C$. Results of such an analysis will be presented and discussed.

Figure 3 implies a maximum frequency of oscillation

$$f = \frac{1}{2\pi}\sqrt{\frac{1}{LC} - \frac{1}{R^2C^2}}$$

This equation is useful only if the lumped parameters of the equivalent circuit are frequency independent. At a high enough frequency we would expect that additional lumped parameters must be introduced or, in other words, that $C$ and $R$ become frequency dependent quantities. Reasons for such a behavior may be due to processes associated with electron tunneling. Further the damping of the electromagnetic field in *Ge* of high conductivity is appreciable; this means that the penetration depth of a plane wave into the highly doped material becomes rather short; for $\Sigma = 300\Omega^{-1}\text{cm}^{-1}$ and $f = 10^{10}$ *cps*, the penetration depth becomes $\delta = 0.03$ *mm*.

---

[1] Tiemann, J. J., "Shot Noise in Tunnel Diode Amplifiers," *Proc. IRE*, p. 1418; 48, 1960.

[2] "How Radiation Affects Tunnel Diodes," *Electronics*, p. 32; May, 1960.

[3] Price, P. J., Radcliffe, J. M., "Esaki Tunnelling," *IBM Journal of Research*, p. 364; 3, 1959.

[4] Heinlein, "Ueber die Trägheit von Halbleiterdioden in Impulsbetrieb," *Arch. Elektr. Uebertr*, p. 387; 11, 1957.

[5] General Radio Experimenter; July-August, 1960.

[6] Baldinger, E., Spycher, U., "Ueber das Impulsverhalten von Tunneldioden"; to be published.

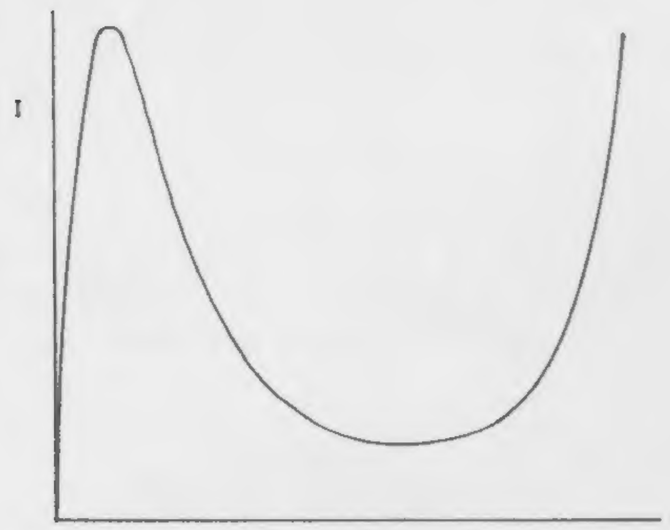


Figure 1—The *dc* characteristic.

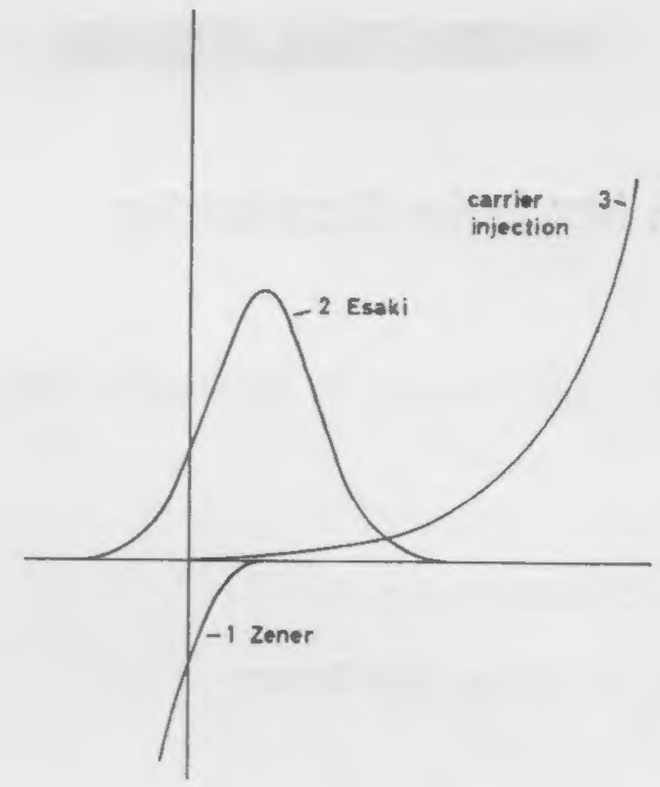


Figure 2—Decomposition of the *dc* characteristic.

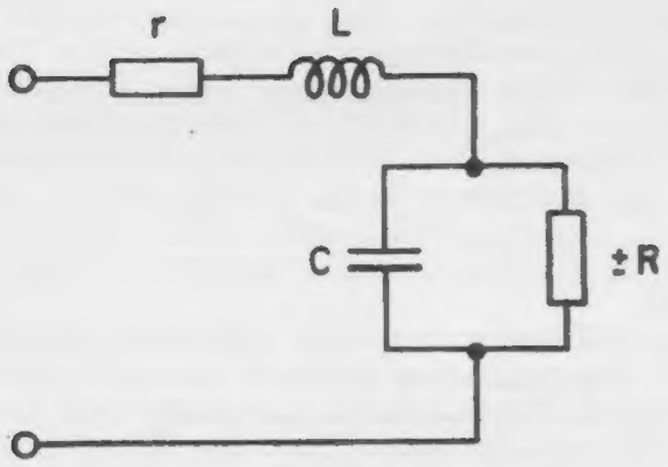


Figure 3—Small-signal equivalent circuit.

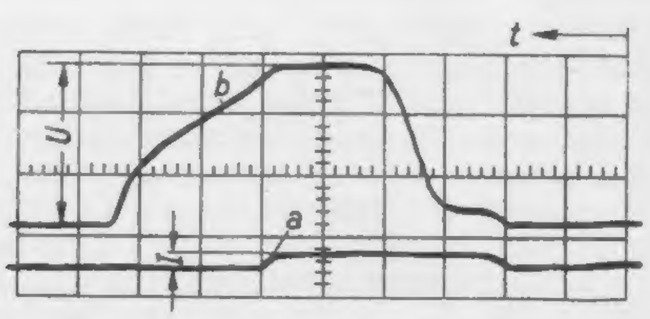


Figure 4—Driving current pulse is illustrated in *a*; diode voltage in *b*.

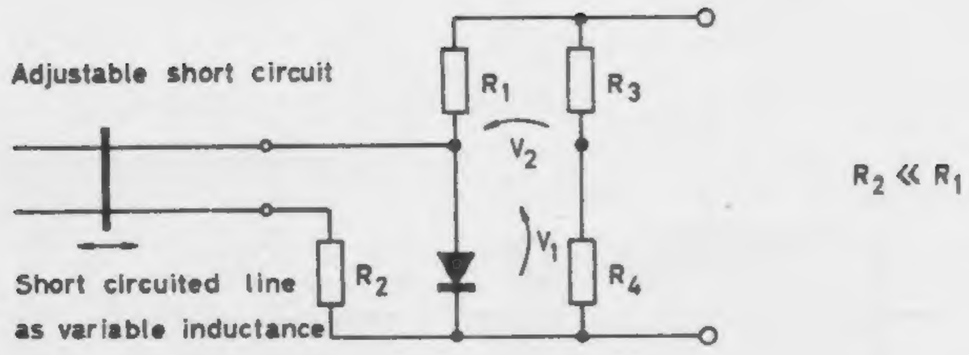


Figure 5—Circuit for measuring parameters; principal only.

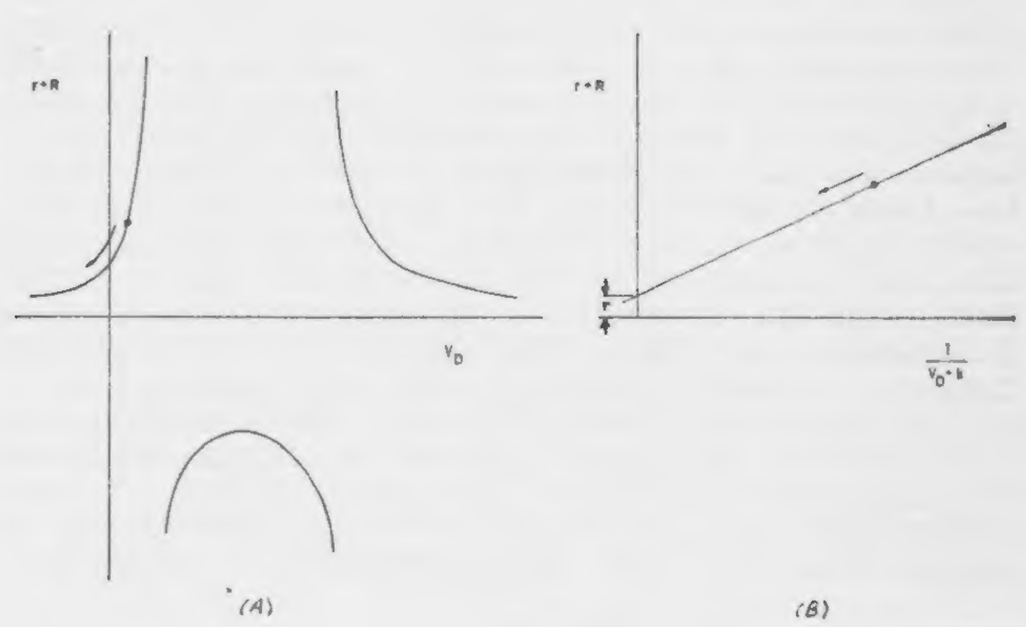


Figure 6—Curves illustrating resistance of the tunnel diode measured at low frequency are shown in *a*; extrapolation to determine *r* appears in *b*.

## SESSION I: New Device Characteristics

### 1.2: Efficiency and Linearity of Multicontact Hall Plates

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Philips Zentrallaboratorium

Laboratorium Aachen, West Germany

WITHIN THE LAST YEARS significant attention has been given to the application of the *Hall* effect. After the semiconducting compounds with high carrier mobility *InSb* and *InAs* were developed, it was possible to produce *Hall* generators giving a power of some 100 *mw* to the load of the *Hall* circuit. The usual arrangement shown in Figure 1 with two current contacts and two *Hall* contacts does not satisfy all requirements of efficiency[1], power output and linearity[2] for applications as gyrators, isolators or multipliers. The use of multicontact *Hall* plates[3], increases the power output, and the efficiency, and decreases the multiplication errors.

Figure 2 shows a *Hall* plate with three separated equal input circuits which are fed by three secondary windings of the input transformer. Furthermore, instead of one pair of *Hall* contacts, as in Figure 1, the multicontact *Hall* plates of Figure 2 has four pairs of output contacts. An output transformer collects the output power of the four *Hall* circuits into the normal two-wire output. This multicontact method lowers the disturbance of the electrical field due to the contacts at the boundaries of the *Hall* plate. The current density in the plate has a higher degree of homogeneity with increasing number of input and output circuits. The field disturbance in the boundary zone of the plate, however, is a source of power losses. Therefore, multicontact *Hall* plates are network elements with low insertion losses. Because of the lower losses and the homogeneous current distribution, the multicontact plate can deliver higher output than a normal plate of equal area.

#### *Low-Loss Nonreciprocal Passive Devices*

Figure 3 represents the efficiency of square *Hall* plates (high quality *InSb*) with equal numbers of input and output circuits as a function of the magnetic induction *B*. A square with six pairs of current contacts and six pairs of *Hall* contacts can deliver some 50% of the input power to the load at a moderate field strength of about 10 *kG*, i.e., it has an insertion loss of 3 db. The normal *Hall* generator as used up to now has an efficiency of only about 12%, i.e., an insertion loss of 9.2 db in the same magnetic field. Since the *Hall* effect is nonreciprocal, multicontact *Hall* plates in a constant magnetic field represent low-loss gyrators. A rhombic plate, as shown in Figure 4, used in a constant magnetic field delivers to the non-reciprocal *Hall* voltage at the output, a reciprocal voltage due to the non-symmetrical nature of the plate. If both of these voltages are equal they cause an enlarged energy flow in one direction, but in the other direction they cancel each other and stop the energy flow. For a multicontact rhomb-shaped *Hall* plate of *InSb*, Figure 5 shows the resistance matrix elements, $R_{11}$ and $R_{12}$, as function of the magnetic induction *B*. The mutual resistance, $R_{12}$, is zero at about 3 *kG*. At this field strength, isolation takes place in one direction and low-loss transmission in the other one. This is shown in Figure 6, where the insertion loss for both directions are plotted. The commonly-reached backward losses in the low-frequency region were always higher than 80 db. With multicontact plates insertion losses of only 1 db in the direction of energy flow can easily be reached. Because the *Hall* effect is independent of frequency, the frequency limit of this isolator is only given by the transformers. With split lines used as transformers it should be possible to build up low loss *Hall* isolators up to 500 *Mc*.

For a *Hall* generator with single circuit, as shown in Figure 1, the resistance depends strongly on the magnetic field strength. Furthermore, the shape and the size of the contacts cause a deviation from the linearity between *Hall* voltage and magnetic field. Theory shows that the size- and shape-dependent nonlinearity should vanish for infinite number of input and output circuits. In Figure 7 the resistance, $R_{11}$, of the plate and the mutual resistance, $R_{12}$, which is proportional to the open circuit *Hall* voltage is plotted against the magnetic field strength *B*. The plates are common with six circuits for the input and six circuits for the output. The multicontact element shows only little dependence of $R_{11}$ on *B*, and the linearity of the *Hall* voltage versus *B* is improved.

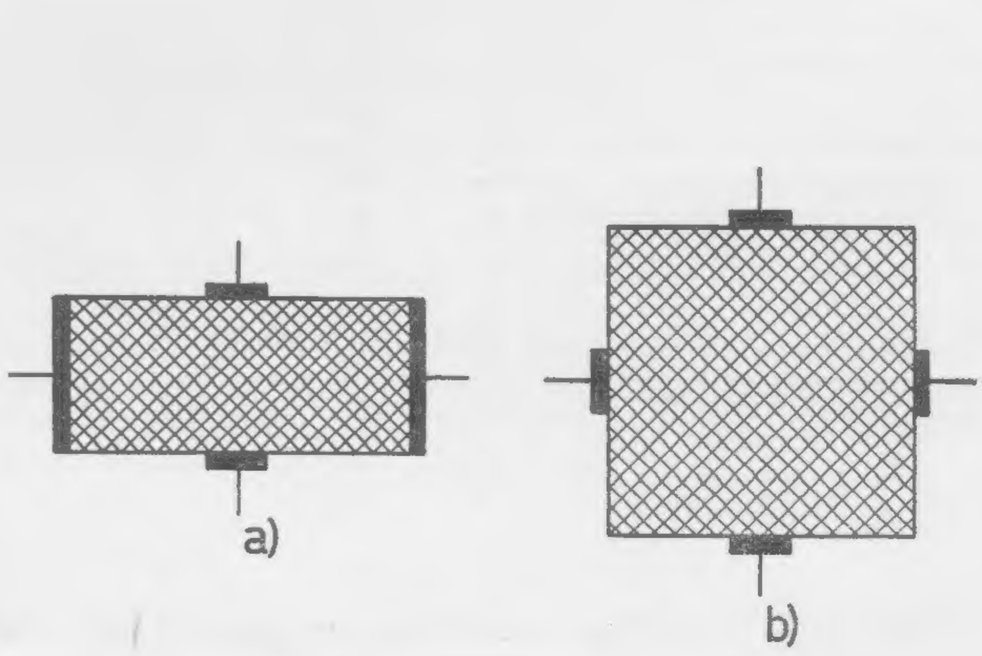



**Figure 1—Common shapes of *Hall* generators.**

[1] Wick, R. F., "Solution of the Field Problem of the Germanium Gyrator," *Journal of Applied Physics;* 741, 1954.

[2] Kuhrt, F., Hartel, W., "Der Hallgenerator als Vierpol" *Archiv fur Elektrotechnik;* 1, 1957.

[3] Arlt, G., "Halleffekt-Vierpole mit Hohem Wirkungsgrad," *Solid-State Electronics;* 75, 1960.

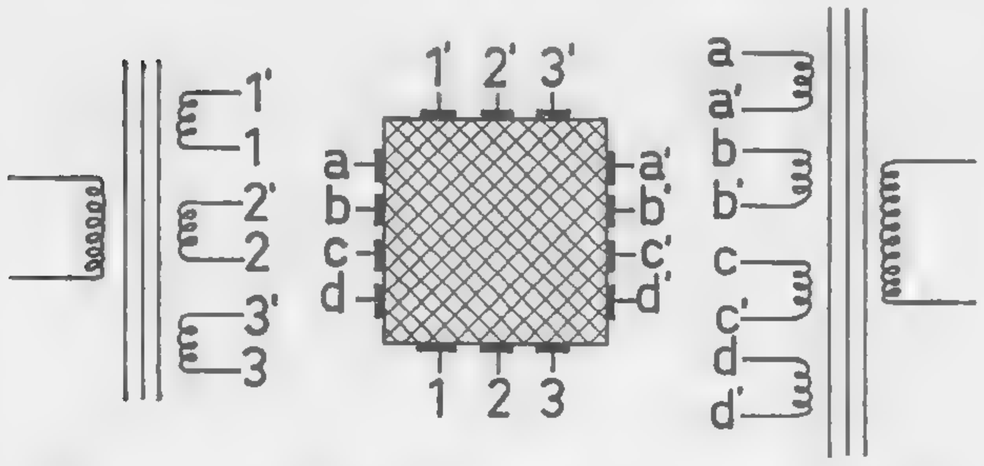



**Figure 2—The multicontact *Hall* plate with input and output transformer. The drawn plate has three input and four output circuits.**

*(Right)*

**Figure 3—Quality factor $\varepsilon = R_{12}/R_{11}$ and insertion loss (in db) of square *Hall* plates for equal numbers of input and output circuits, measured on plates of *InSb* of *Hall* constant $R = 179\ cm^3/A\ sec$.**

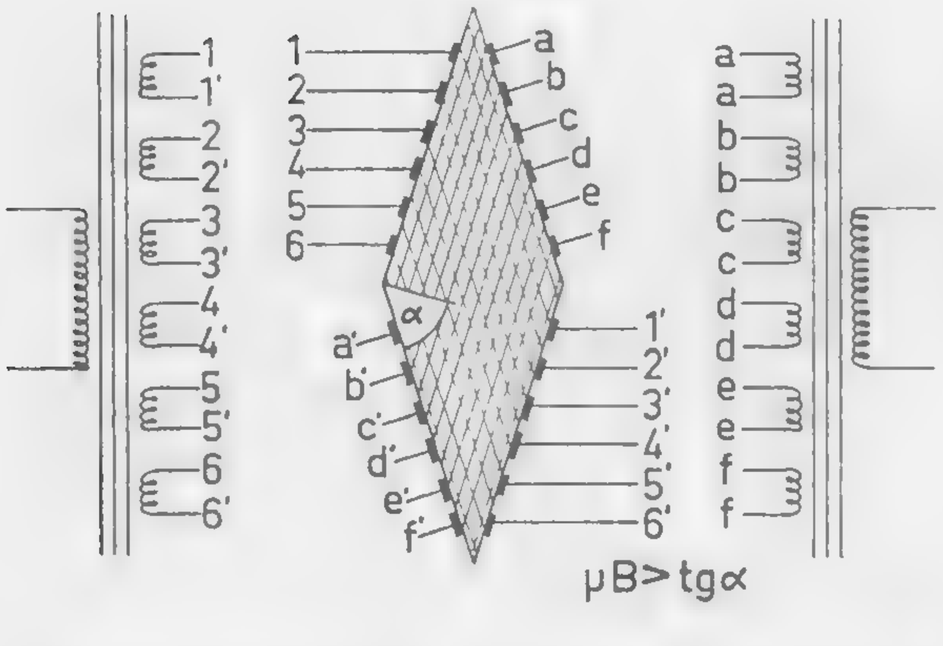



**Figure 4—Rhomb-shaped multicontact *Hall* plate as an isolator.**

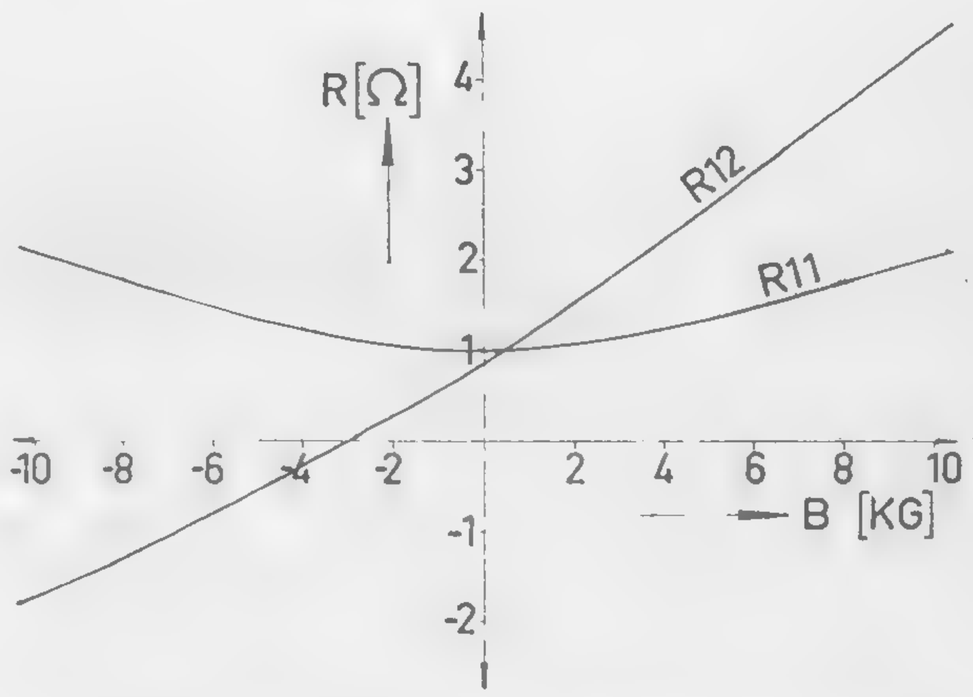
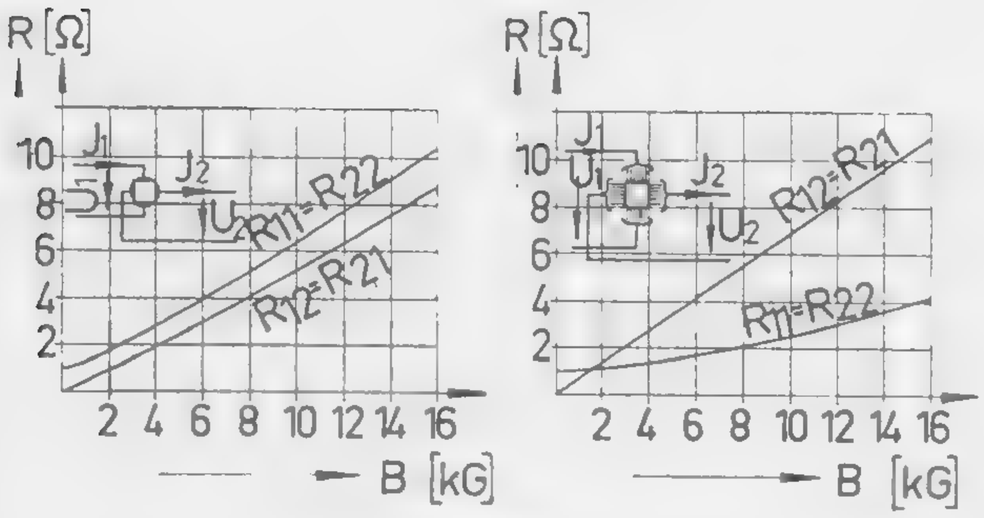



**Figure 5—Network resistances of six-circuit rhomb-shaped *Hall* plate as a function of the magnetic induction for *InSb* with a *Hall* constant of $R = 390\ cm^3/A\ sec$.**

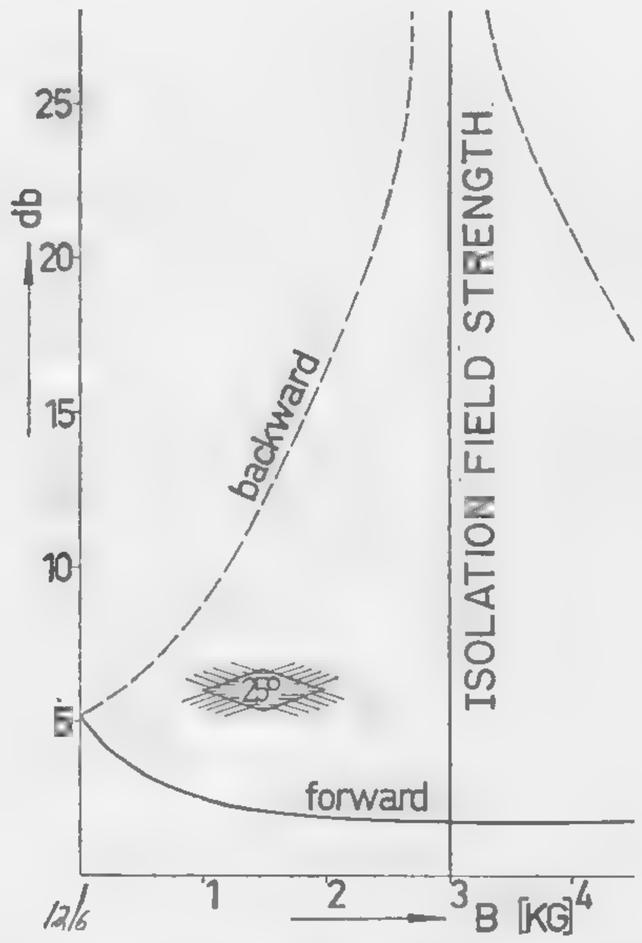



*(Right)*

**Figure 6—Forward and backward insertion losses for the isolator of Figures 5 and 6.**

*(Above)*

**Figure 7—Network resistance of single circuit (upper diagram) and six circuit (lower diagram) square *Hall* plates as a function of the magnetic induction *B*, for *InSb* with a *Hall* constant of $R = 390\ cm^3/A\ sec$.**



## SESSION I: New Device Characteristics

### 1.3: Analysis of a Nonlinear Transmission Line*

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Hewlett-Packard Company

Palo Alto, Calif.

THE TRANSMISSION LINE shown in Figure 1 includes nonconstant capacitance which is voltage-dependent; consequently, the transmission line is nonlinear. As a first step toward understanding the properties of such a distributed line, it can be shown, for a wave propagating in one direction, that each voltage value propagates with velocity given by $v = 1/\sqrt{LC(V)}$[1,2,3]. This situation is illustrated in Figure 2, where each straight line marks the path of a particular voltage level in the $(x,t)$ plane.

Such considerations lead to simple schemes for calculating the changes in a propagating wave. For example, Figure 3 shows waveforms calculated for a particular nonlinear line driven with a sine wave at the input. Experimentally obtained waveforms are shown in Figure 4. The excellent agreement should be noted.

In case there are waves propagating in both directions on the line, the situation is much more complex. However, the nonlinear transmission line equations can be transformed into a set of four *characteristic* equations which can be interpreted in terms of Figure 5. The curved lines of positive slope represent the paths of waves propagating to the right in the sense that the lines have a reciprocal slope that is equal to the voltage-dependent velocity $v = 1/\sqrt{LC\ (V)}$. Also, the voltage and current changes along one of these lines of positive slope are related by the voltage-dependent characteristic impedance; i.e., $dV/dI = -\sqrt{L/C(V)}$. The minus sign appears since an observer traveling with the wave will see current and voltage changes only as a result of encountering an oppositely propagating wave. Similarly, the curved lines of negative slope represent the paths of waves propagating to the left. A finite difference scheme for calculating $V(xt,)$ and $I(x,t)$ can be developed fom these properties[3].

One of the most interesting features of a nonlinear transmission line is that it can generate electromagnetic shock waves which have extremely fast rise times. The mechanism of shock formation is that different voltage levels propagating at different velocities can *pile up* with the result that $V(xt,)$ can become nearly discontinuous. The inevitable losses associated with the line keep $V(x,t)$ from becoming perfectly discontinuous. In fact, if the loss mechanism is assumed to be a series resistance in the nonlinear capacitive elements of the line, then the waveforms associated with typical shock waves can be obtained exactly. Also, the velocity of propagation and the energy loss associated with a shock wave can be calculated in terms of the line parameters and the voltages just ahead of and just behind the shock.

Some experimental work with shock waves has been carried out. For a nonlinear line made with reverse biased junction diodes, the theory indicates a rise time associated with a shock wave which is approximately equal to the period of the *cutoff* frequency of the diode capacitors. For example, it should be possible to obtain 0.1 nanosecond rise times with 10 *kMc* diodes. Rise times of 0.5 nanosecond have actually been observed with a sampling oscilloscope known to have a rise time of about 0.5 nanosecond. For the purpose of checking the waveform associated with a shock wave, a lumped approximation to a distributed line was made with diode capacitors with cutoff frequencies which were artificially lowered to 500 *Mc* by adding series resistance. Figure 6 shows the output waveform of this line when driven by a 50-*Mc* sine wave. The waveform calculated for a single shock arriving at the output is shown in Figure 7, while Figure 8 shows an expanded view of the region near the shock of Figure 6. The 10% to 90% rise time is 2 nanoseconds. Thus, the shock wave theory has received excellent experimental verification.

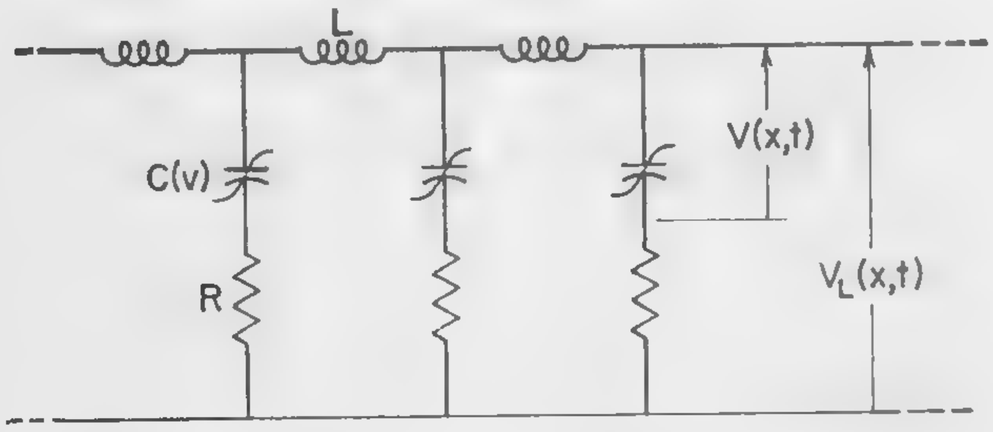
---

* Work covered by paper was performed at Stanford University.

[1] Landauer, R., "Parametric Amplification Along Nonlinear Transmission Lines," *J. Appl. Phys.*, p. 479-484; March, 1960.

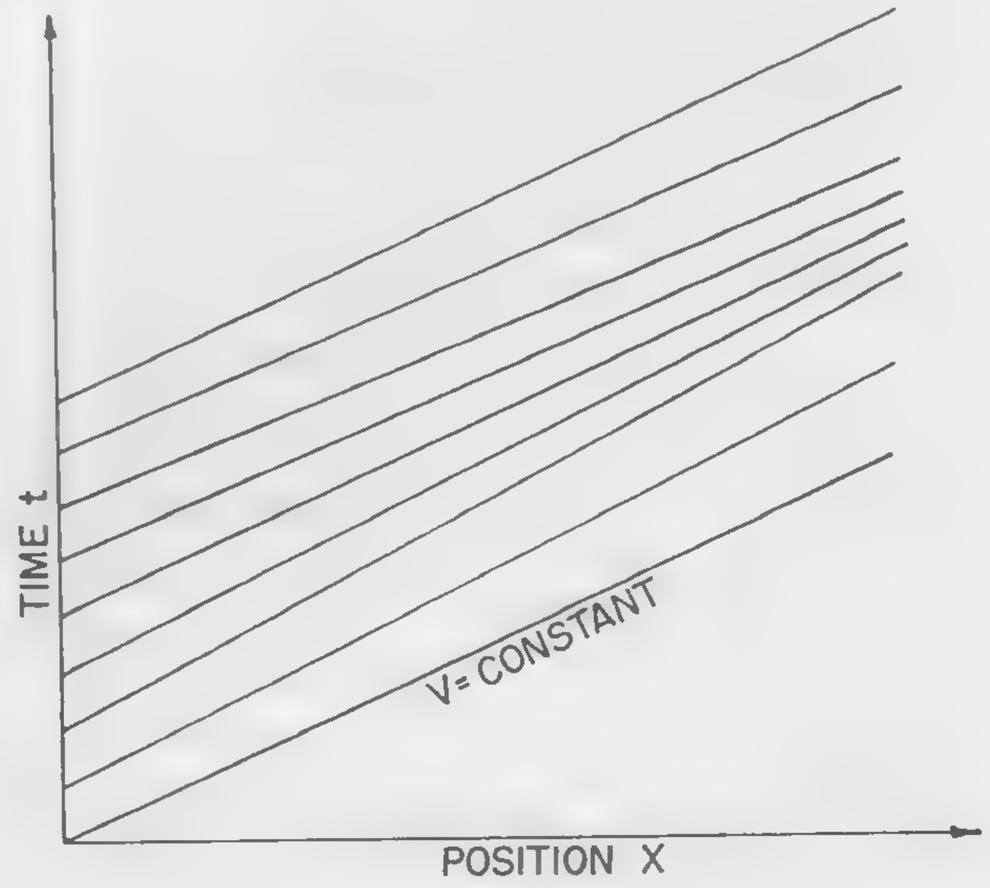
[2] Landauer, R., "Shock Waves in Nonlinear Transmission Lines and Their Effect on Parametric Amplification," *IBM Journal*, p. 391-401; October, 1960.

[3] Riley, R. B., "An Analysis of a Nonlinear Transmission Line," Ph.D. Thesis, Stanford University.




(Above)

**Figure 1—Nonlinear transmission line. A distributed line is assumed for the analysis; $R = O$ for a lossless line.**




(Right)

**Figure 2—Paths in the $(x, t)$ plane of constant voltage for a forward propagating wave on a lossless nonlinear line $(R = O)$.**

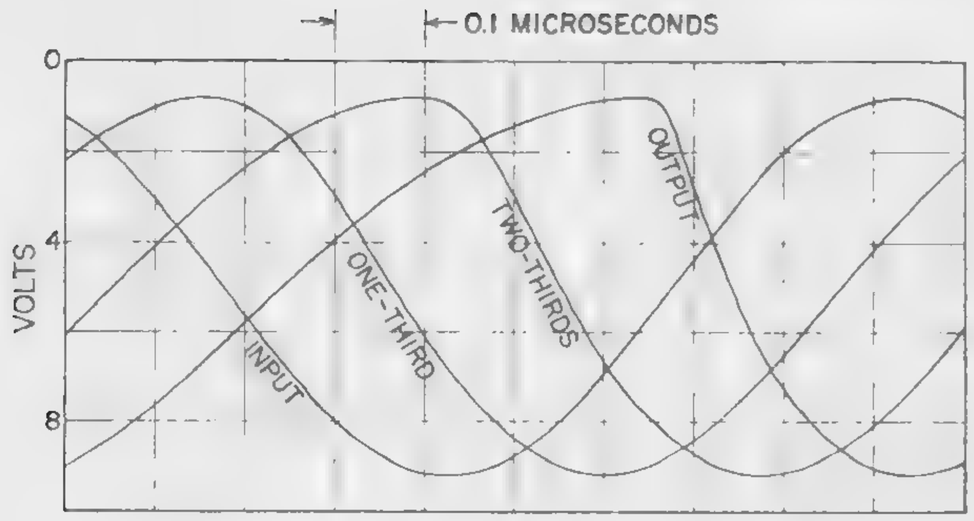



Figure 3—Calculated waveforms on a nonlinear line without shock waves; input, one-third of distance along line, two-thirds, and output. Compare with Figure 4.

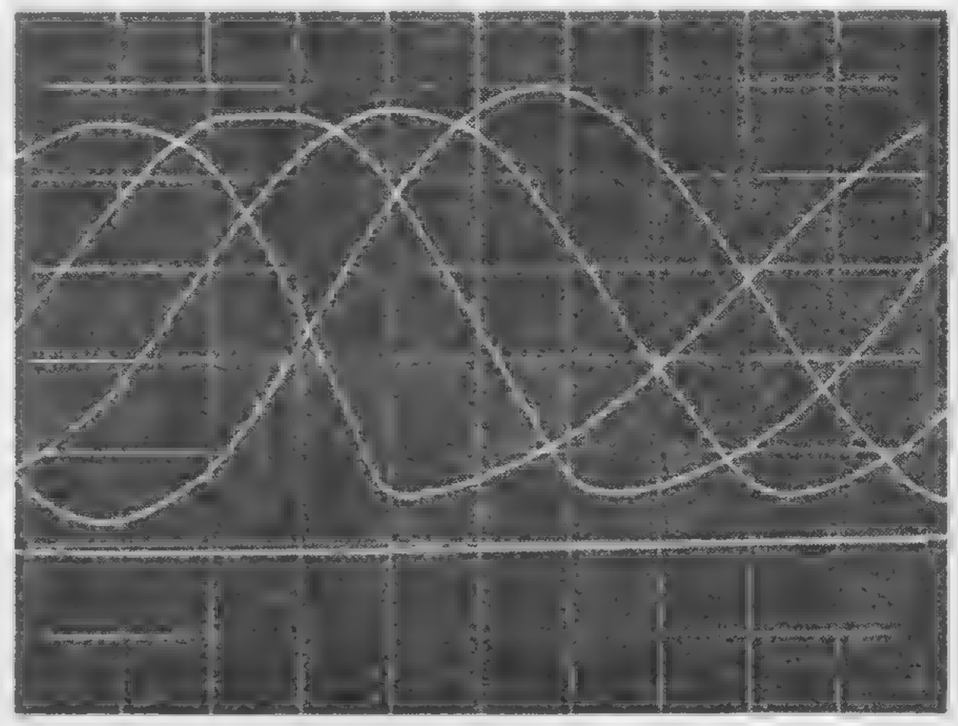


Figure 4—Measured waveforms on a nonlinear line without shock waves. (Horizontal—0.1 microsec/div.; vertical—2 volts/div.)

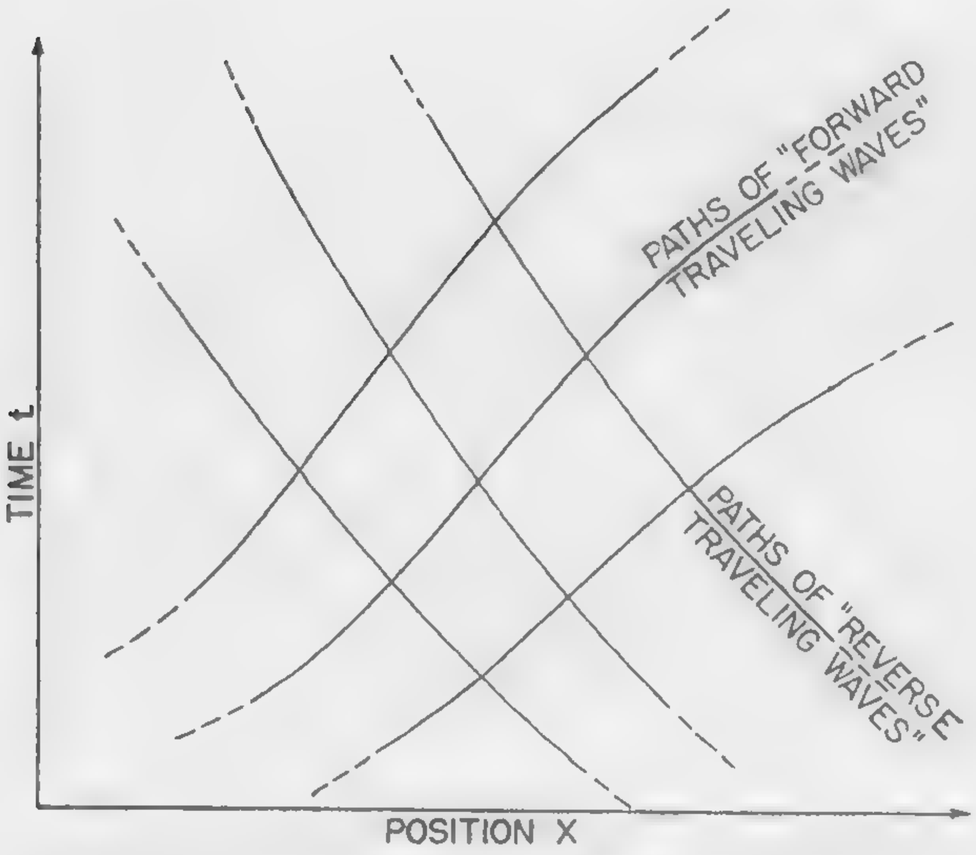



Figure 5—*Characteristic* curves (paths of forward and backward propagating waves) for a lossless nonlinear line ($R = O$).

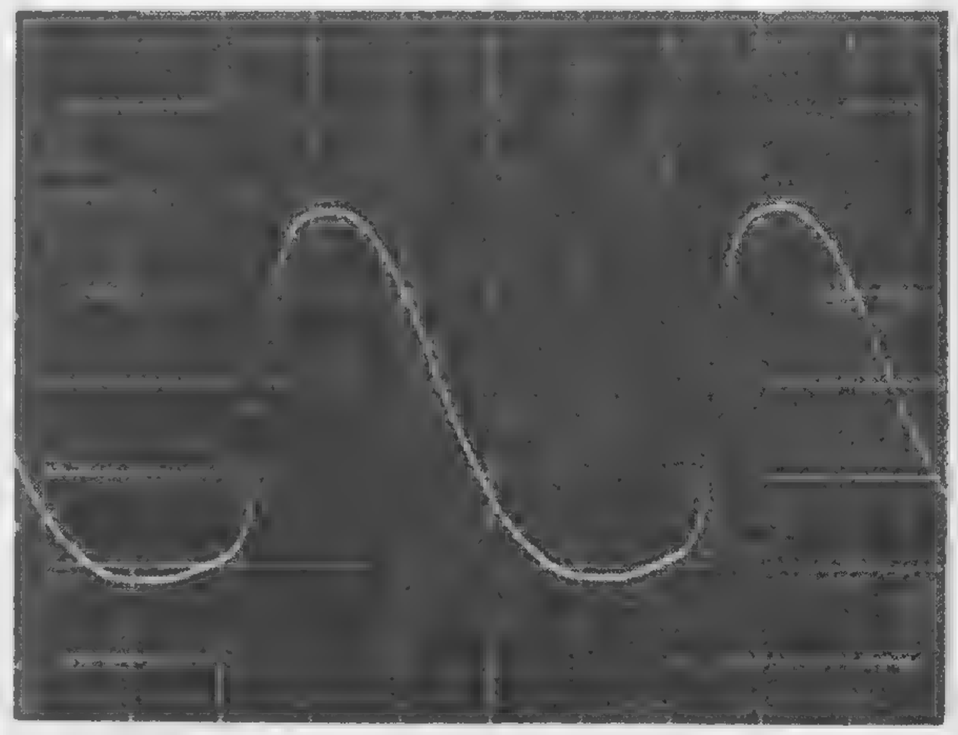


Figure 6—Measured waveform on a lossy nonlinear line with a shock wave. (Horizontal—4 nanosec/div.; vertical—2 volts/div.)




Figure 7—Calculated waveform near a shock wave. Compare with Figure 8.

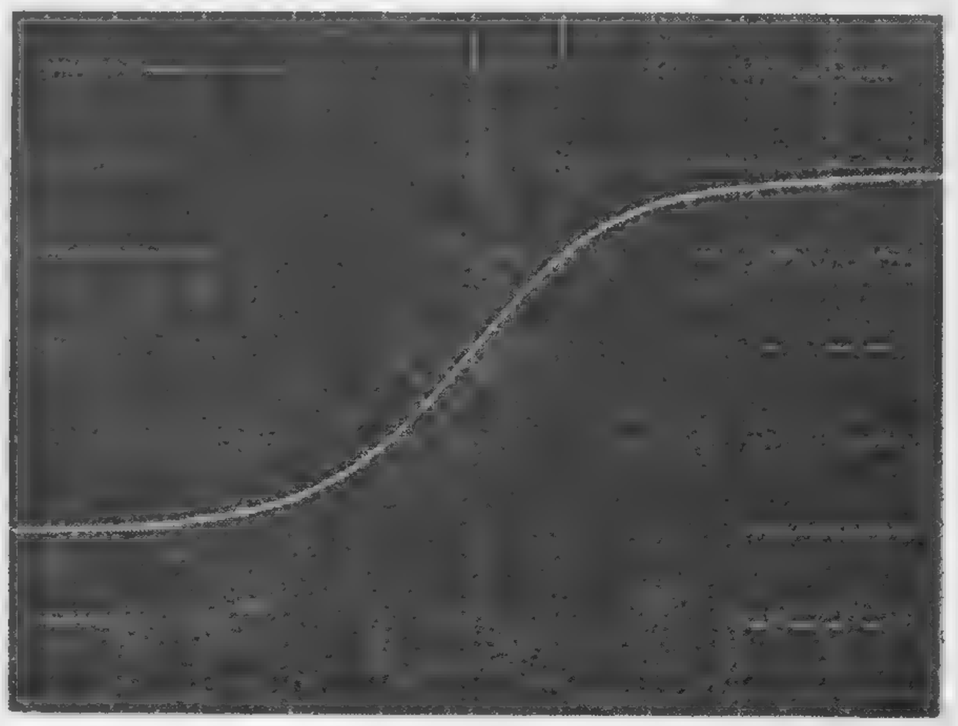


Figure 8—Measured waveform near a shock wave; Figure 6 expanded. (Horizontal—0.5 nanosec/div.; vertical—2 volts/div.)

## SESSION I: New Device Characteristics

### 1.4: A Comparison of the Diffusion-Limited Semiconductor Junction Diode and the Space-Charge-Limited Dielectric Diode

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University of Birmingham

Birmingham, England

THE DIFFUSION-LIMITED SEMICONDUCTOR DIODE and the space-charge-limited dielectric diode are both similar in basic operation. Current occurs in each device by the transit of charge between an input electrode and an output electrode; to achieve large current the input capacitance for stored charge must be large and the transit time of charge must be small. A large input capacitance is more readily achieved in the semiconductor diode, whereas a small transit time is more readily achieved in the dielectric diode. Thus the semiconductor diode is inherently suited to operation at high-current densities as in power rectification and switching systems, whereas the dielectric diode is inherently suited to high-frequency operation as in communications, computing and microwave systems.

Space-charge-limited current has been achieved in the laboratory using insulating crystal plates of pure cadmium sulphide. Deep trapping levels have been effectively eliminated by the mechanism of defect compensation and the basic square-law dependence of current upon voltage has been confirmed experimentally. Materials such as gallium arsenide and aluminium antimonide are more suitable for device development; the data presented in this paper are based on parameters, characteristic of electrons in gallium arsenide.

Compensated crystals used for the fabrication of dielectric diodes contain ionized donor centers which act as shallow electron traps. If present in sufficient density these can affect the frequency characteristics of a space-charge-limited device. Calculations show that trapping affects mainly the low-frequency characteristics and that at high frequencies the diode acts almost as if trap-free. In any event, however, trap densities and depths in a practical device are sufficiently low so that the effects of trapping are negligible.

To achieve high-frequency operation the electrode spacing must be made small. The reciprocal transit time is a measure of operating bandwidths and on this basis it is evident that the dielectric diode offers approximately an order of magnitude increase in bandwidth over the semiconductor diode at the same electrode spacing.

In the semiconductor diode the junction width increases by space-charge widening into the lower conductivity *P*-region; at high reverse voltages the depletion layer reaches completely across the device. In the dielectric diode on the other hand, which operates at much lower current density, the electrode spacing increases by space-charge widening into the *N*-region which is comparable in conductivity with the *P*-region of the semiconductor diode. Thus, much larger reverse voltages can be withstood before breakdown field strength is reached. In this case the electrode spacing can be made very small to achieve very high-frequency operation without significantly reducing reverse electric strength.

The forward characteristics of the semiconductor diode are very sensitive to temperature changes; this is because of the exponential dependence on temperature of the injected minority carrier density. In the dielectric diode, however, the injected carrier density is space-charge-limited and is almost independent of temperature. Thus the dielectric diode is not affected very much by temperature changes and can operate over a wide temperature range.

The semiconductor diode is a noisy, temperature-sensitive device. At low frequencies large fluctuations in current are caused by variations in the number of carriers in the conduction levels of the device; at high frequencies this noise mechanism becomes negligible and shot noise is predominant. Current fluctuations in the dielectric diode should be very much smaller. Variations in stored charge are virtually eliminated by space-charge-reduction and variations in transit time caused by the thermal velocity distribution of the carriers should be much smaller even than in the vacuum diode.

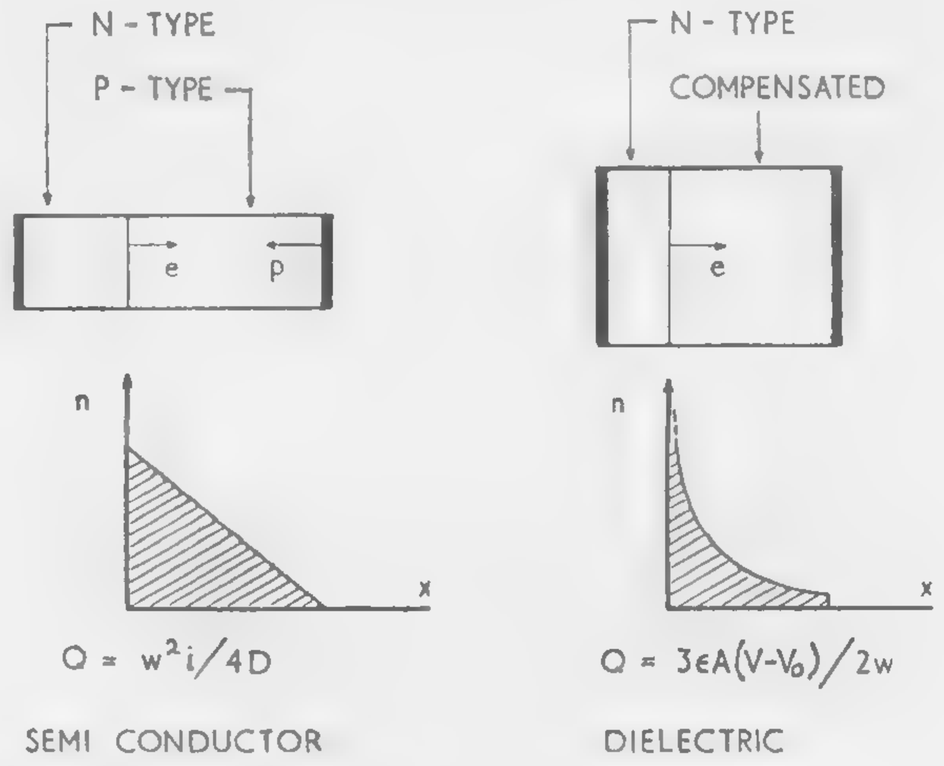



**Figure 1—Forward operation. In the semiconductor diode, the output (collector) electrode injects majority carriers to maintain electrical neutrality; in the dielectric diode it is a blocking electrode and electrical neutrality is not maintained.**

| QUANTITY | SEMI CONDUCTOR DIODE | DIELECTRIC DIODE |
|---|---|---|
| CURRENT | $i = \frac{eDN_0A}{w} \exp\left(\frac{eV-W}{kT}\right)$ | $i = \frac{9\epsilon\mu A}{8w^3}\left(V-V_0\right)^2$ |
| INPUT CAPACITANCE | $C = \frac{ew^2 i}{2kTD}$ | $C = \frac{3\epsilon A}{2w}$ |
| TRANSIT TIME | $t_r = \frac{w^2}{4D}$ | $t_r = \frac{4w^2}{3\mu(V-V_0)}$ |
| RECTIFICATION RATIO (APPROX) | $R \sim \exp\left(\frac{W}{kT}\right)$ | $R \sim \exp\left(\frac{eV_0}{kT}\right)$ |
| IN EACH CASE CURRENT EQUALS RATIO OF STORED CHARGE TO TRANSIT TIME | | |

**Figure 2—Basic formulas for idealized devices: $W$ = difference between energy band systems in N and P-regions. $V_0$ = difference between work functions of cathode and anode.**

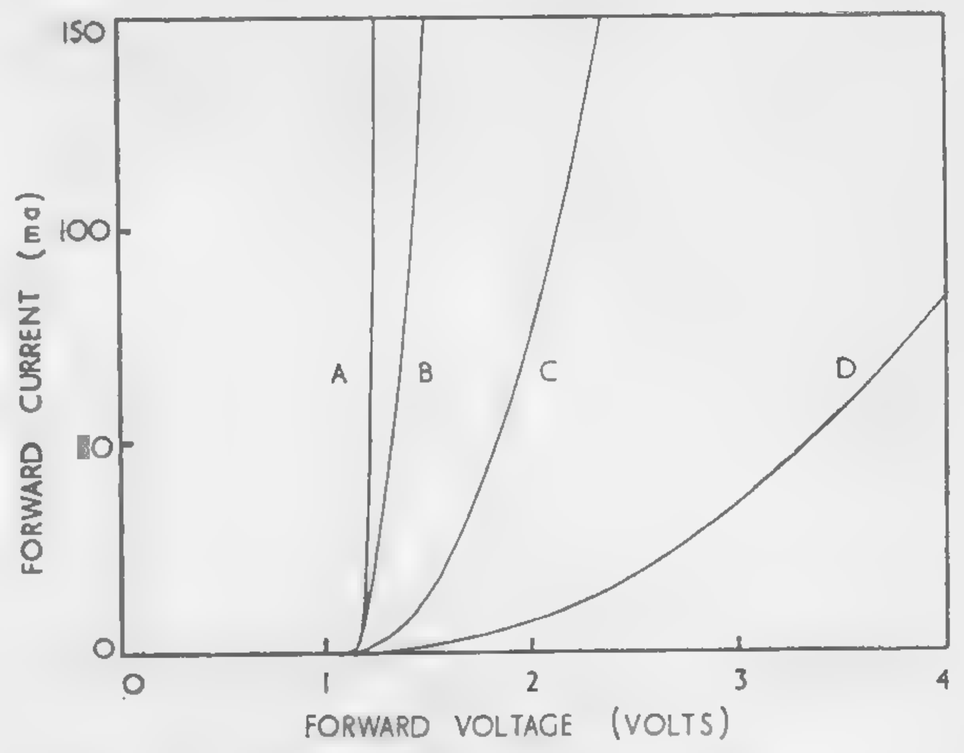



**Figure 3—Typical forward characteristics; electrode spacing 1 micron. Semiconductor diode: *(A)*—electrode area 10 microns square, C = 76 *pf* at 100 ma. Dielectric diode: *(B)*—electrode area 100 microns square, *C* = 1.5 *pf*. *(C)*—electrode area 30 microns square, *C* = 0.15 *pf*; *(D)*—electrode area 10 microns square, *C* = 0.015 *pf*.**

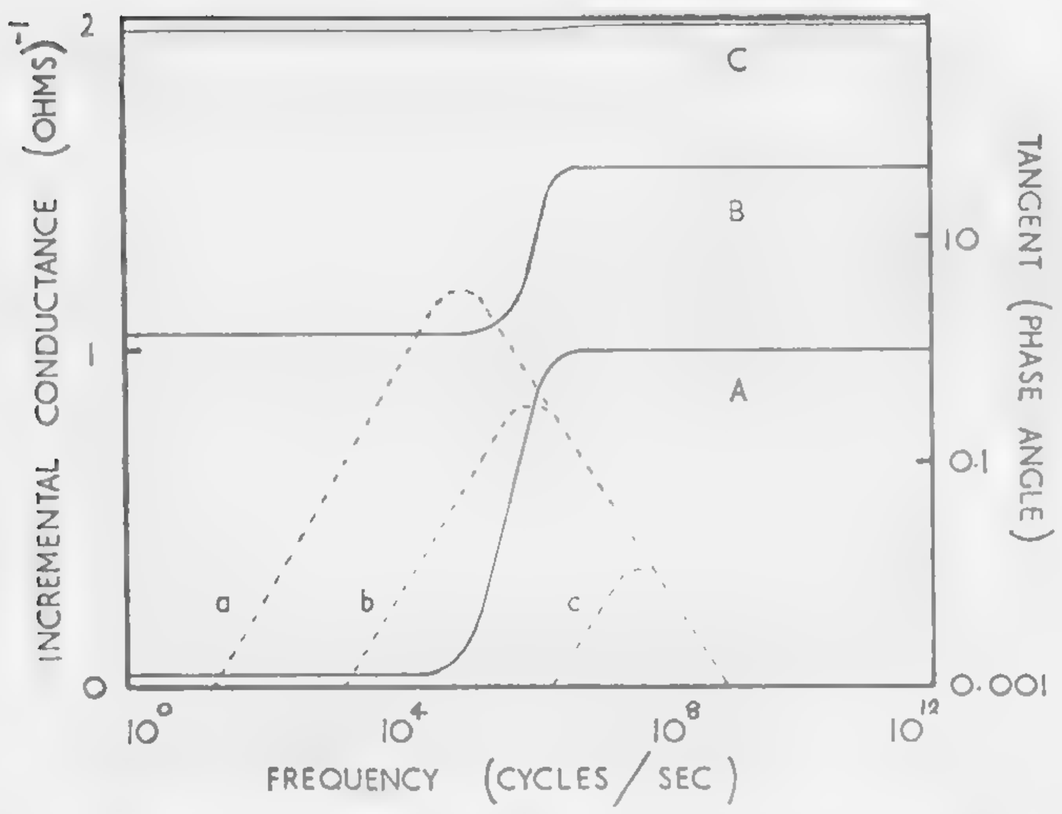



**Figure 4—Frequency dependence of incremental conductance (curves *A, B, C*) and phase lead of current (curves *a, b, c*) caused by trapping: Electrode spacing 1 micron; electrode area 100 microns square; trap density $10^{22}$ $m^{-3}$. *(A, a)*—trap depth O-3*ev*; *(B, b)*—trap depth O-2*ev*; *(C, c)*—trap depth O-1*ev*.**

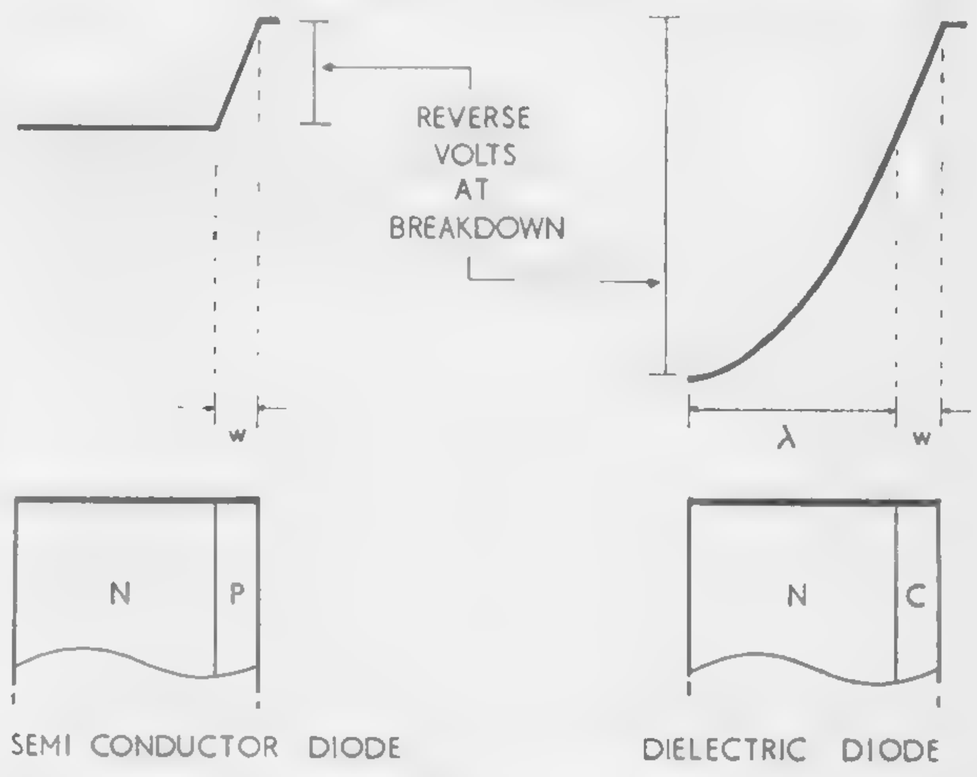



**Figure 5—Reverse operation. In the semiconductor diode a high reverse voltage is applied uniformly across the small electrode spacing *w*. In the dielectric diode the reverse voltage is applied across the increased spacing ($\lambda + w$).**

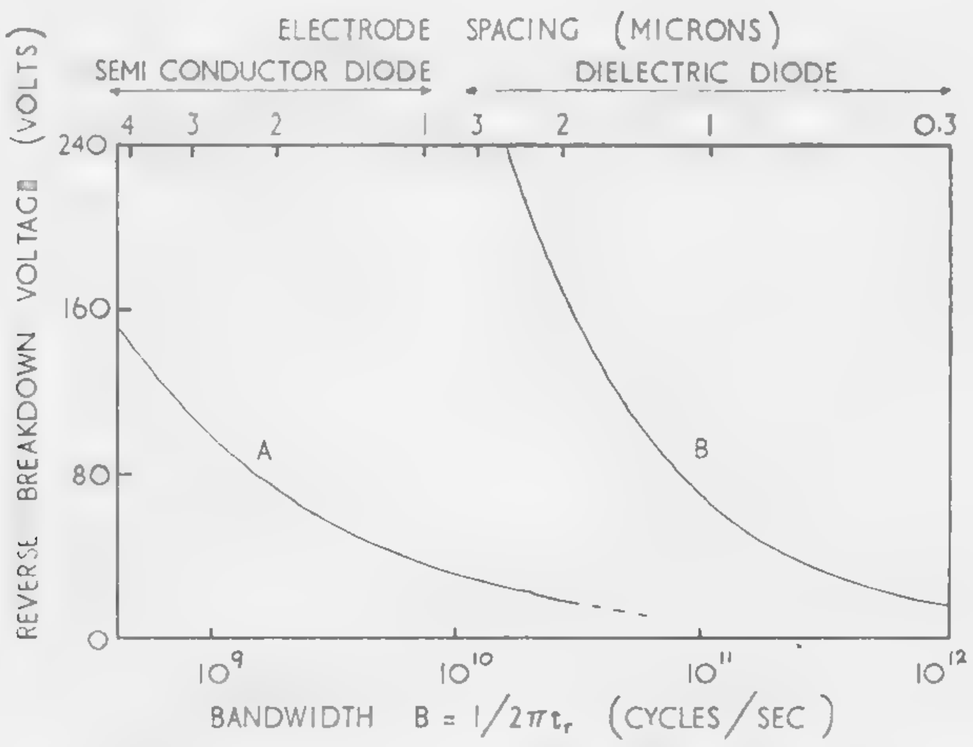



**Figure 6—Relation between operating bandwidth and reverse electric strength. *(A)*—semiconductor diode; *(B)*—dielectric diode.**

## SESSION I: New Device Characteristics

### 1.5: Superconducting Tunneling Devices

I. Gaever

Research Lab., General Electric Company

Schenectady, N. Y.

THE IDEAL CAPACITOR shown in Figure 1 can consist of two parallel metal plates separated by a $10^{-4}$ *cm* wide vacuum region. No steady state current would be observable in such an arrangement. However, if the separation distance between the two plates could be reduced to, say, $10^{-7}$ *cm* or 10Å, a rather large *dc* would flow in the circuit. The explanation for this phenomena is the quantum mechanical tunnel effect, which allows the electrons to flow across the vacuum region, even though classically this is energetically impossible. The general behavior of such a conduction mechanism is understood[1].

The main features are that for small fields the tunnel current is proportional to the voltage, gradually changing to a *Fowler-Nordheim*[2] (cold emission) relation at higher voltages. The tunnel current is a strong function of the separation distance between the metal plates, decreasing exponentially with this separation. An energy diagram of the capacitor-like arrangement is shown in Figure 2, where for comparison both thermionic emission current and tunnel current is shown.

It is difficult to separate two metals by such a narrow vacuum region, but easy to separate them by an aluminum-oxide film of small thickness as illustrated in Figure 3. First a strip of aluminum is evaporated onto a clean glass plate (microscope slide). The surface of this aluminum strip is then oxidized. Finally a metal is vapor-deposited across the first strip, resulting in a sandwich of the aluminum oxide between the two metals, thus forming a capacitor-like arrangement. It has been shown that the current across such a narrow aluminum oxide layer is mainly due to tunneling[3].

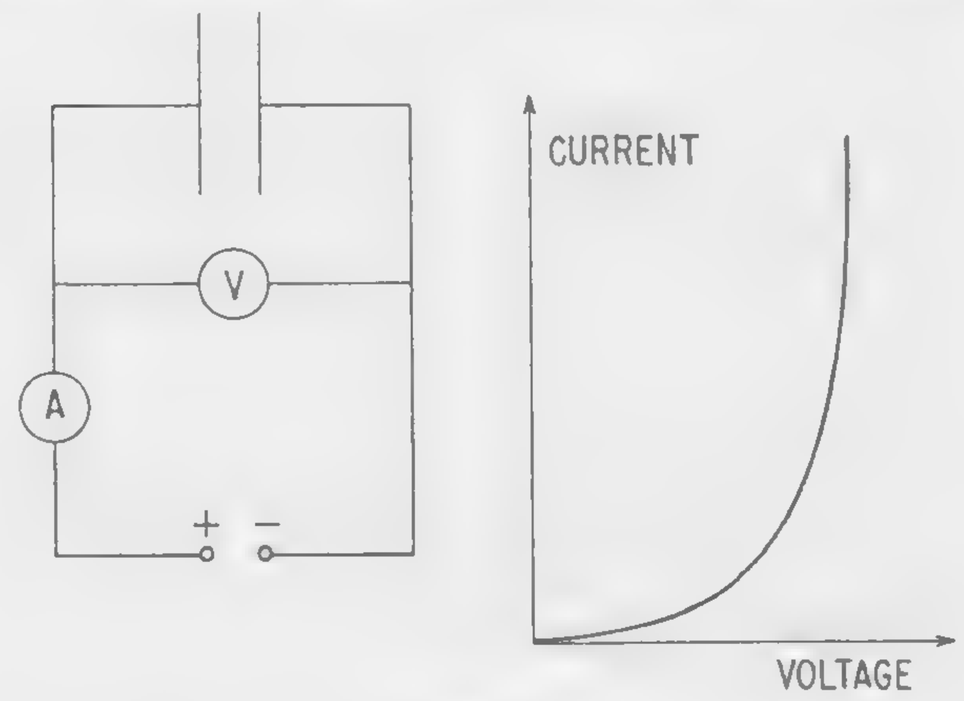
If one of the two metals forming the sandwich is made superconducting, the current-voltage characteristics for low electric fields changes from a linear to a non-linear behavior[4]; Figure 4. The reason for this drastic change is that a forbidden energy range centered at the *Fermi* energy appears in the electron density of states when a superconductor goes from its normal to its superconducting state. This non-linear current-voltage behavior can be changed by subjecting the metal-oxide-metal sandwich to a magnetic field, also illustrated in Figure 4. The current-voltage characteristic is independent of polarity. If a coil is wound around the capacitor-like arrangement, as shown schematically in Figure 5, the tunnel current flowing between the two metals can be modulated by passing a current through the coil. Thus the device has all the features necessary to make a triode or related devices such as switches.

If both metals forming the sandwich are made superconducting, a negative-resistance region appears in the voltage-current characteristics[5,6] as shown in Figure 6. Again the voltage-current characteristic is independent of polarity. The negative resistance is closely related to the energy gaps and to the rapidly-varying density of states in the two superconductors. A superconductor thus shows a superficial resemblance with an intrinsic semiconductor, and quantitatively the negative resistance region may be understood based upon such a model; Figure 7. The value of the negative resistance is a function of the operating temperature as well as the applied magnetic field, as shown in Figure 8.

It should be noted that the current through the samples can be varied within wide limits by varying the thickness of the oxide layer. Resistances measured when both metals are normal ranges from $10^{-4}$ ohms $cm^2$ to $10^{6}$ ohms $cm^2$. The voltage at which the negative resistance occurs, and further, the negative resistance region itself depends upon what combination of superconductors is used. It will usually be in the millivolt range, and the figures shown are typical.

*Credits*

To *J. C. Fisher* and *C. P. Bean*, for their interest and encouragement and to *K. Megerle* and *P. E. Lawrence*, for helping with some of the experiments, sincerest thanks.

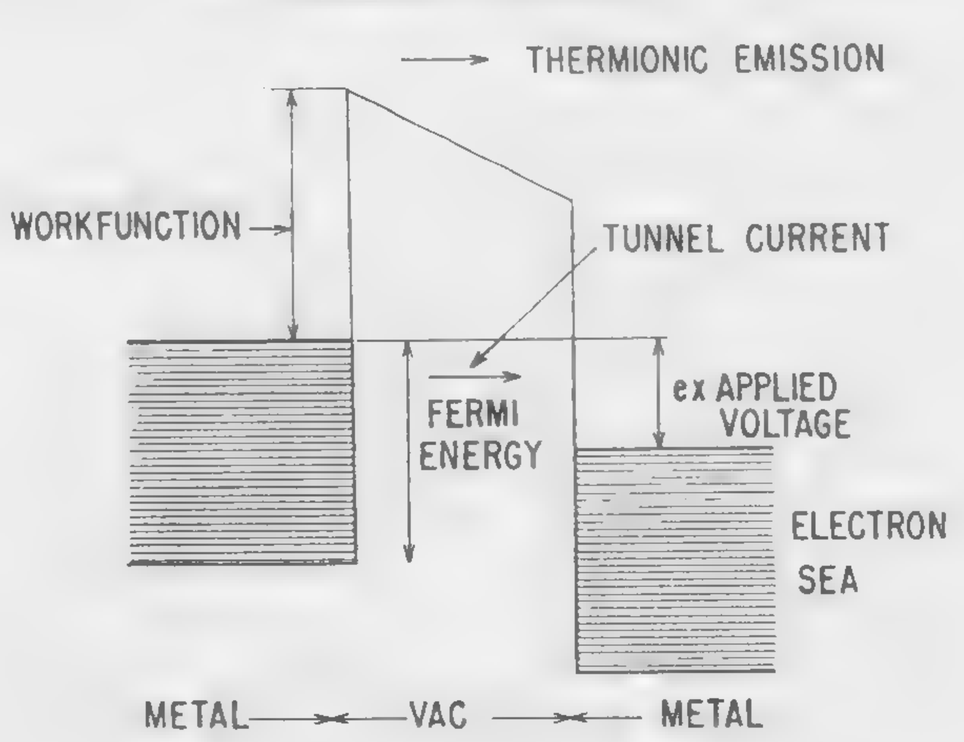



*(Above)*

**Figure 1—If the separation distance between the capacitor plates is less than approximately 100 *Å*, *dc* will flow in the circuit. Typical current-voltage characteristic is shown to the right.**

*(Below)*

**Figure 2—An energy diagram of the capacitor arrangement of Figure 1. Since the current flow is nearly independent of temperature, thermionic emission is ruled out.**




[1] Holm, R., *J. Appl. Phys.*, 22, 569; 1951.
[2] Nordheim, L., *Physik. Z.*, 30, 177; 1929.
[3] Fisher, J. C. and Giaever, I., submitted to *J. Appl. Phys.*
[4] Giaever, I., *Phys. Rev. Letters*, 5, 147; 1960.
[5] Giaever, I., *Phys. Rev. Letters*, 5, 464; 1960.
[6] Nicol, F., Shapiro, S., Smith, P. H., *Phys. Rev. Letters*, 5, 461; 1960.

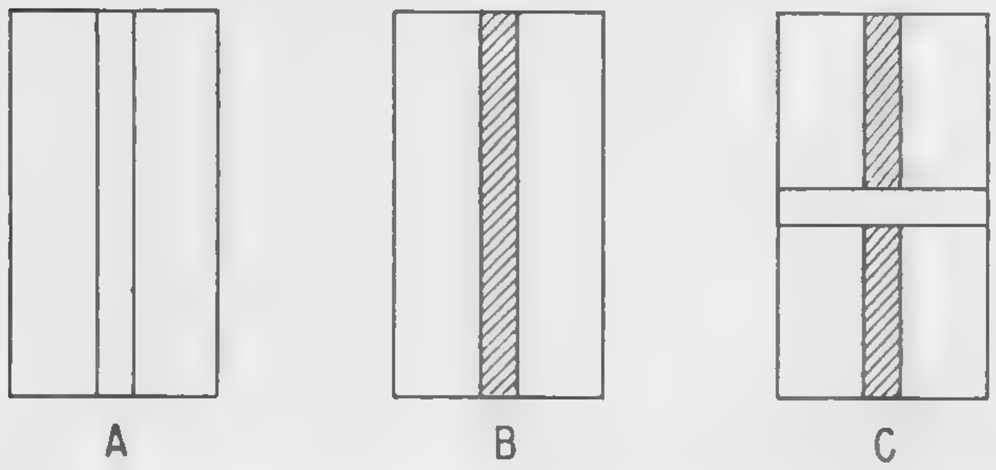



Figure 3—Preparation of the capacitor like-arrangement: *(a)*—Glass slide with the evaporated aluminum strip; *(b)*—surface of the aluminum strip has been oxidized; *(c)*—another metal has been evaporated across the aluminum oxide forming a metal-oxide-metal sandwich.

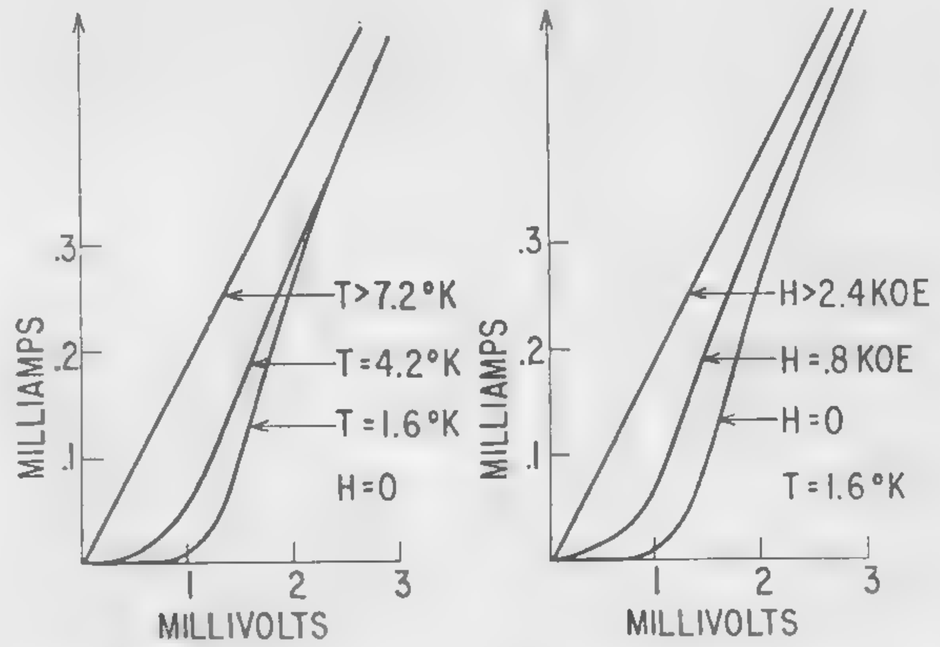



Figure 4—Current-voltage characteristic of an aluminum-aluminum oxide-lead sandwich, as a function of temperature and magnetic field.

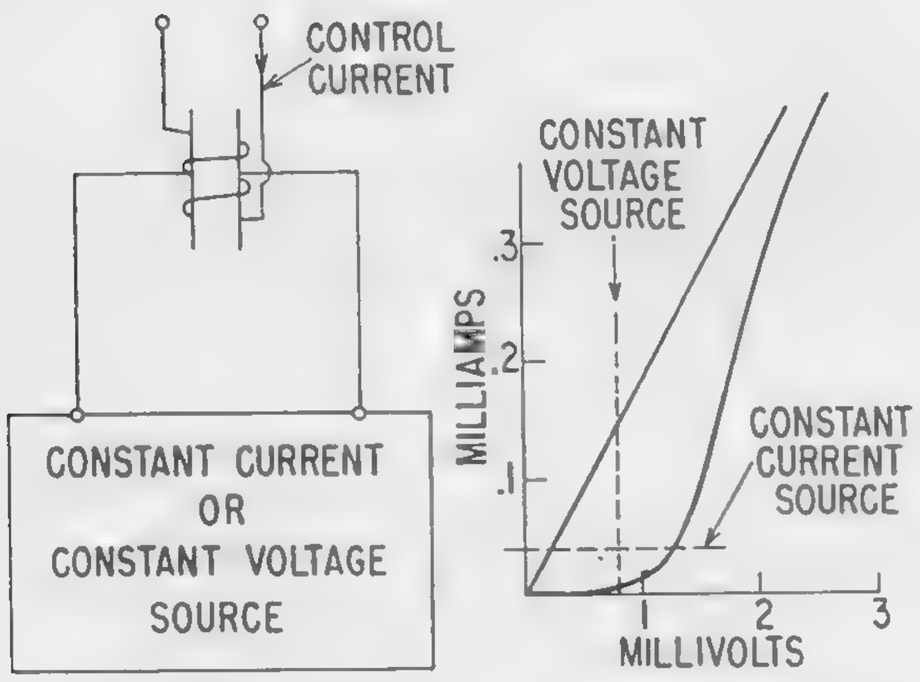



Figure 5—Illustration of principle of a metal-insulator-metal sandwich operated as an active element.

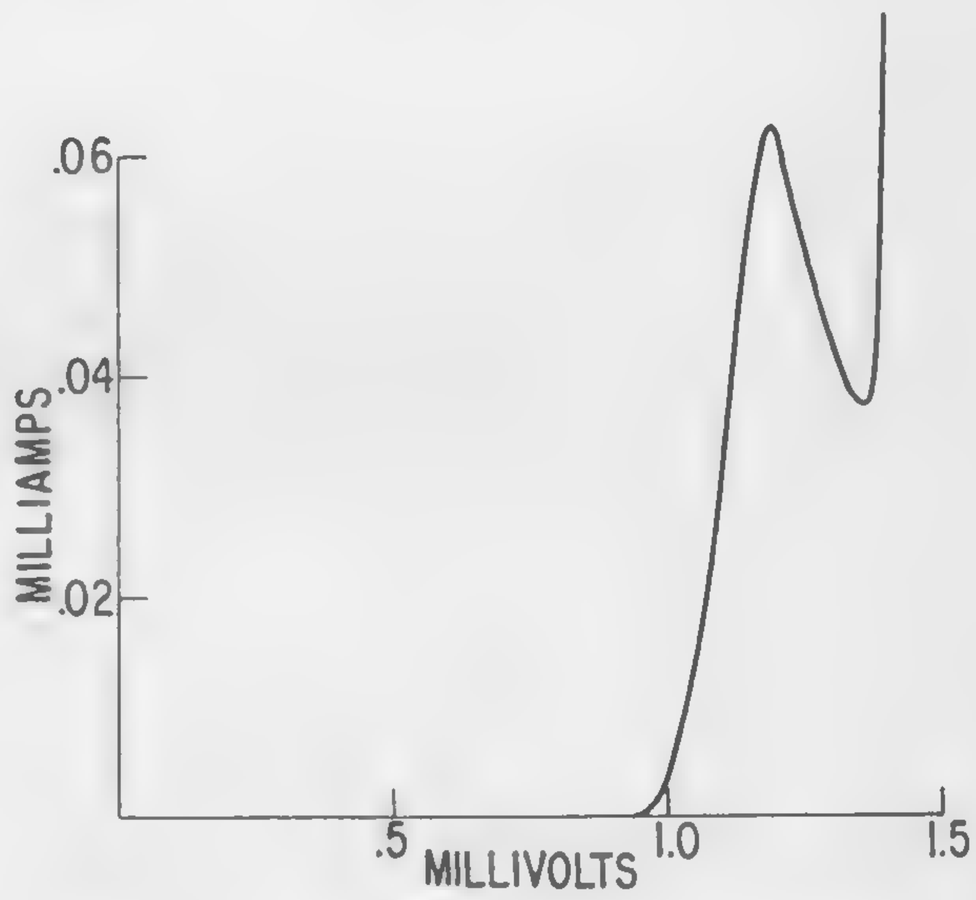



Figure 6—Negative resistance obtainable with a superconductor-insulator-superconductor sandwich. The example shown is an *Al-Al₂O₃-Pb* sandwich at approximately 1°*K*.

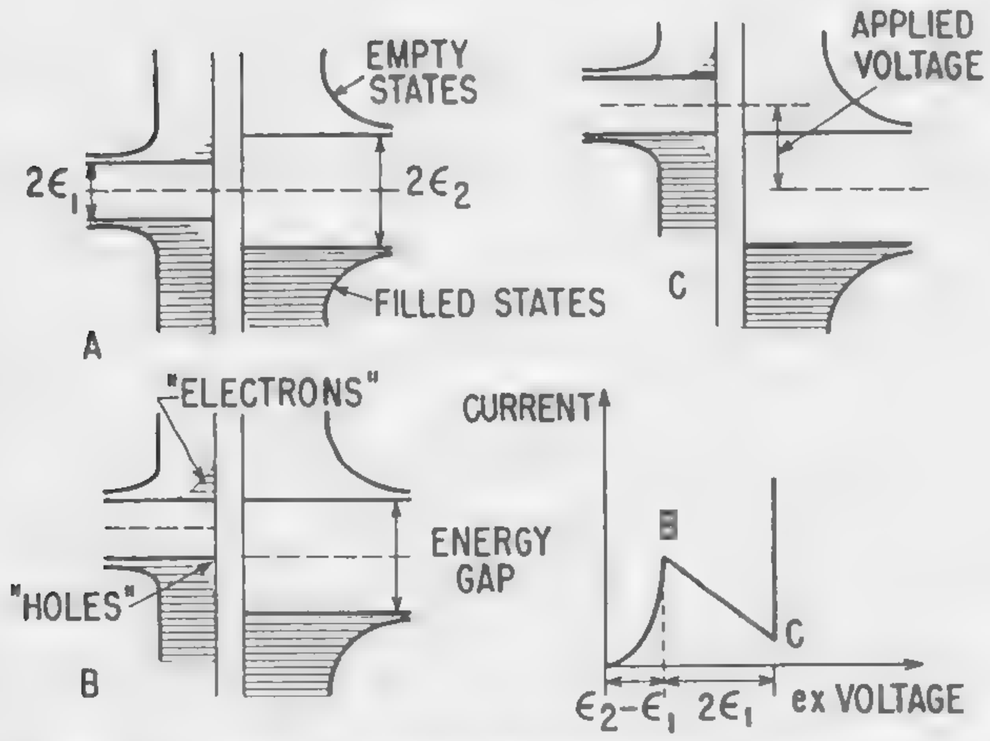



Figure 7—Energy diagram showing the energy gaps and density of states in two dissimilar superconductors separated by an insulating layer. The negative resistance region is associated with the rapid change in the electronic density of states near the energy gaps.

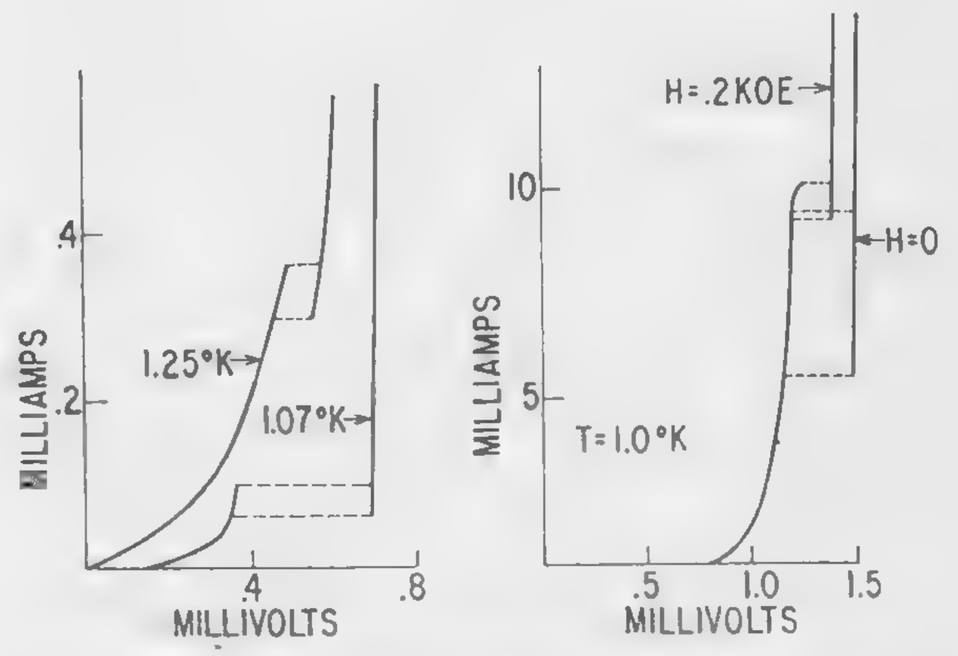



Figure 8—Effect of temperature and applied magnetic field on the negative resistance for two different sandwich types. At left an *Al-Al₂O₃-In* sandwich; at right an *Al-Al₂O₃-Pb sandwich.*

## SESSION II: Microwave Amplifiers

Chairman: E. W. Sard
Airborne Instruments Laboratory, Melville, N. Y.

### 2.1: The Characteristics of Esaki Diodes at Microwave Frequencies*

H. Fukui
Sony Corporation
Tokyo, Japan

THE MOST REMARKABLE FEATURE of the *Esaki* diode is its extremely high limiting frequency of the negative conductance region.

A small-signal equivalent circuit for the *Esaki* diode is shown in Figure 1. The admittance at the terminals *a-a'* represents the total admittance of the circuit observed at the input terminals. The admittance to the right of the terminals *c-c'* represents the *p n* junction admittance. Values of $g_t$, $C_b$, $g_d$ and $C_d$ are all dependent on the bias voltage. There is a negative region of $g_t$ along the forward voltage direction. For a small bias voltage $g_d$ and $C_d$ can usually be neglected.

At frequencies of 0.3 to 4.6 *kMc* admittance has been measured by means of the standing-wave method; Figure 2. The *Esaki* diode was terminated by a purely resistive load to avoid oscillations in the negative conductance region. A small brass block was mounted in place of the diode to determine the minimum standing-wave voltage point and to obtain a reference point. The *Esaki* diode was then actually mounted and the admittance was measured by keeping the input level within 1$\mu w$. From the measured *swr* and the voltage minimum point, the admittance at the reference point can be computed and thus the admittance of the *Esaki* diode itself. The *swr* in the negative conductance region can be expressed by negative values of the *swr*.

In Figure 4, showing the measured admittance of an *Esaki* diode, dotted lines correspond to the negative conductance region. It will be seen that at 4.6 *kMc*, a negative conductance is still observed between the terminals *a-a'*.

(A)—$C_S$: A number of burned Esaki diodes were measured and the most probable value was estimated to be 0.85 *pf*.

(B)—$R_S$ and $L_S$: Evaluation may be done by biasing the diode such that $g_t$ becomes sufficiently large; results are shown in Figure 5. It will be seen that $R_S = 2.5 + 0.5\sqrt{F\ (kMc)}$ ohms and $L_S = 0.21\ m\mu H$.

(C)—$g_t + g_d$ and $C_b + C_d$: Junction admittance is given in Figure 6; values are essentially frequency independent.

(D)—$C_b$ and $C_d$: Relation between $1/(C_b + C_d)^2$ and the bias voltage is plotted in *a* of Figure 7. Capacitance in the linear region is due to $C_b$. In the diffusion-current region, this relation deviates from the straight line due to an additive capacitance $C_d$. $C_b$ satisfies the well-known barrier capacitance formula for a step junction. Thus, we have $C_o = 1.4\ pf$ and $V_t = 0.86\ v$, which agree well with the calculated results for a *Ge p n* junction with $p = n = 4 \times 10^{19}\ cm^{-3}$. As for $C_d$, Figure 7*b* agrees well with the result calculated from the diffusion capacitance formula in the high bias region.

(E)—Comparison of calculated and observed results: In Figure 8, it will be noted that both results agree well. Therefore one finds that the equivalent circuit outlined can express the characteristics of an *Esaki* diode sufficiently accurate from low frequencies up to the microwave region.

### *Figure of Merit of an Esaki diode*

The mechanism responsible to the negative conductance is a very fast phenomenon due to quantum mechanical tunneling. But because of the junction capacitance, there results a time constant of $(C_b/g_t)$, which limits the response time of an *Esaki* diode. Therefore the value of $(C_b/g_t)_{min}$ is the primary important figure of merit in microwave frequencies. Thus, one finds that $(C_b/g_t)_{min}$ is about $1.3 \times 10^{-10}$ second. This value corresponds, according to an approximate calculation, to the *Ge p n* junction.

$(C_b/g_t)$ is a time constant determined only by the junction. However, the overall time constant of an *Esaki* diode is affected by $R_S$ and $L_S$. Consequently, the resistive cutoff and the self-resonant frequencies, which are obtained from the equivalent circuit, are 5.6 and 8.7 *kMc*, respectively.

* To be presented by: **M. Uenohara**, Bell Telephone Laboratories, Inc. Murray Hill, N. J.

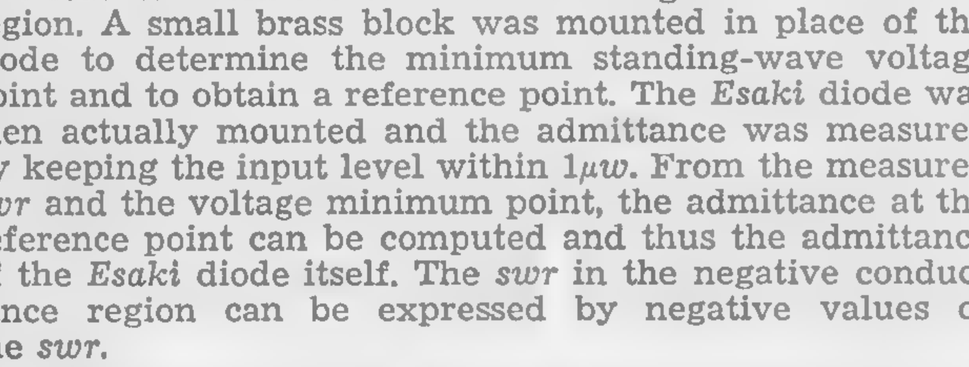



**Figure 1—A small-signal equivalent circuit where $g_t$ represents the tunnel conductance; $C_b$, the barrier capacitance; $g_d$ and $C_d$, the diffusion conductance and capacitance; $R_s$, the bulk resistance, and $L_s$ and $C_s$, the capsule inductance and capacitance.**

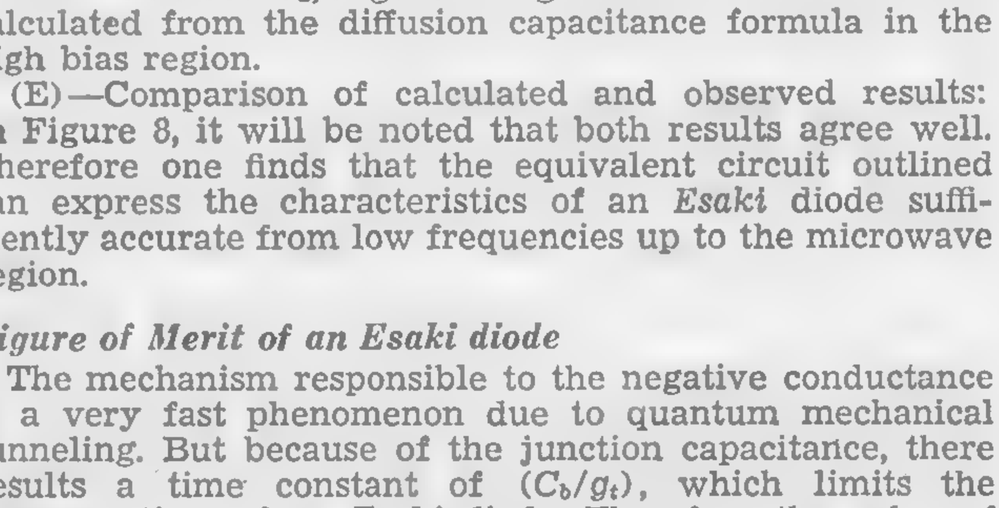



**Figure 2—Block diagram of the measuring circuit. The characteristic impedance of the coaxial system is 50 ohms. The *Esaki* diode measured has an $I_p$ of 2 *ma*. For larger $I_p$, the use of a lower impedance line or matching transformers may be necessary.**

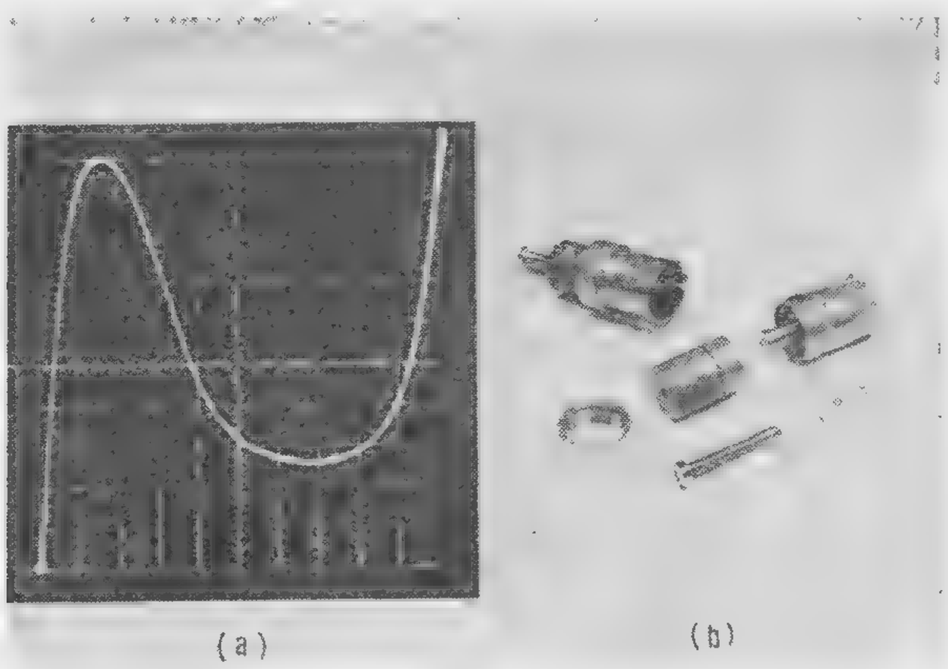



Figure 3—*(a) I-V* characteristic curve of a *Ge Esaki* diode used in this measurement. Horizontal—50 *mv/div.*, vertical—0.2 *ma/div. (b)* The mount[2] of an *Esaki* diode.

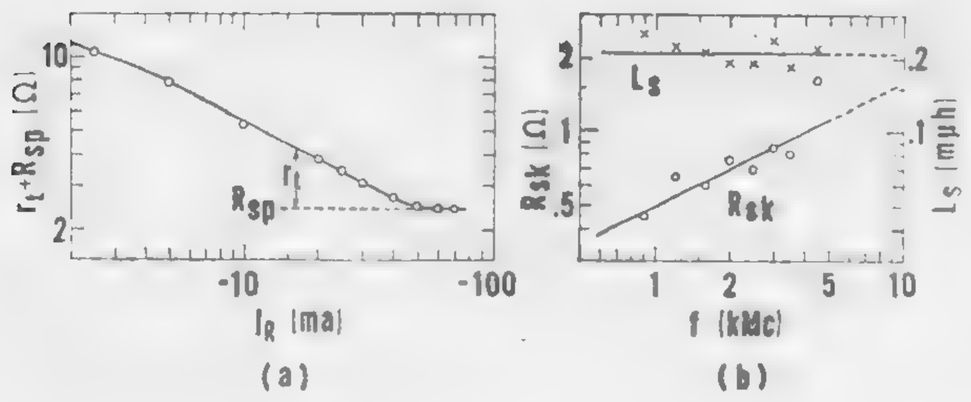



Figure 5—*(a)* Reverse characteristics of an *Esaki* diode at lower frequencies. $R_{sp}$ represents the spreading resistance. *(b)* Frequency characteristics of $L_s$ and $R_{sk}$, the skin effect resistance; $R_s$ consists of $R_{sp}$ and $R_{sk}$.

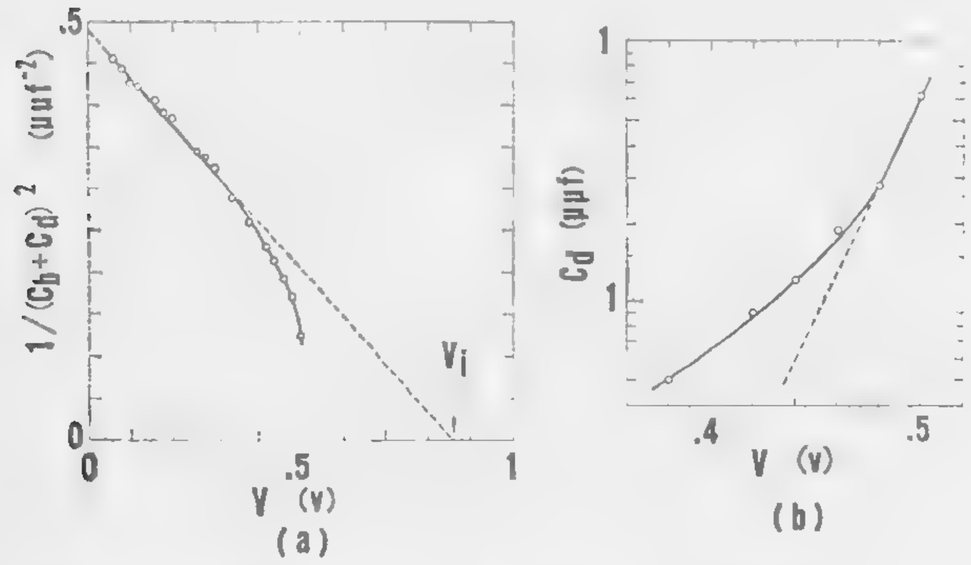



Figure 7—Separation of the barrier capacitance and the diffusion capacitance from the junction capacitance: *(a)* Relation between $1/(C_b + C_d)^2$ and bias voltage; *(b)* diffusion capacitance versus bias voltage.

[1] Sony IT1103.
[2] Modified General Radio coaxial connector 874-B.

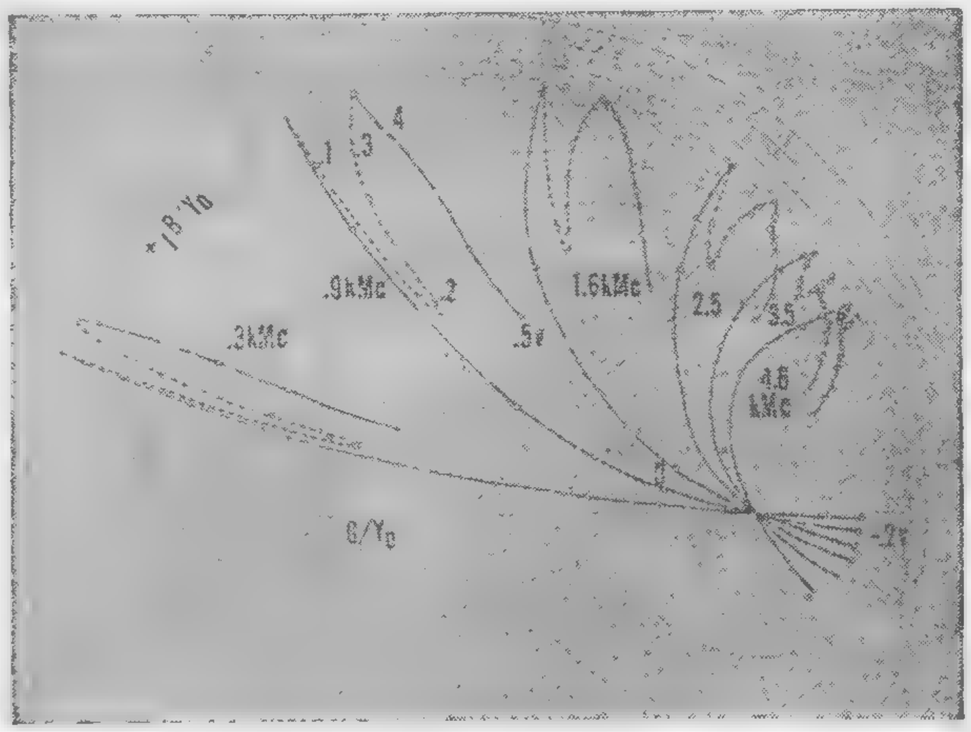



Figure 4—Measured admittance of an *Esaki* diode[1] versus bias voltage for various frequencies. The admittance corresponds to that between the terminals *a-a'* of the equivalent circuit shown in Figure 1.

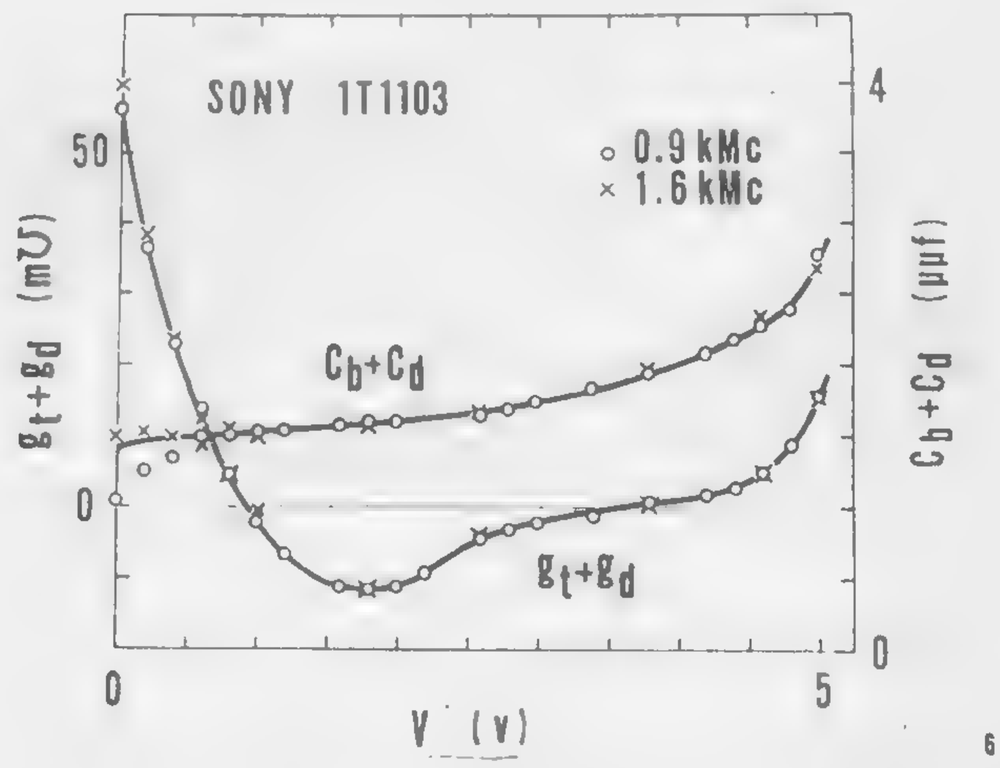



Figure 6—Junction conductance, $g_t + g_d$, and capacitance, $C_b + C_d$, versus bias voltage, computed from the observed values at 0.9 and 1.6 *kMc*. The results are essentially frequency independent.

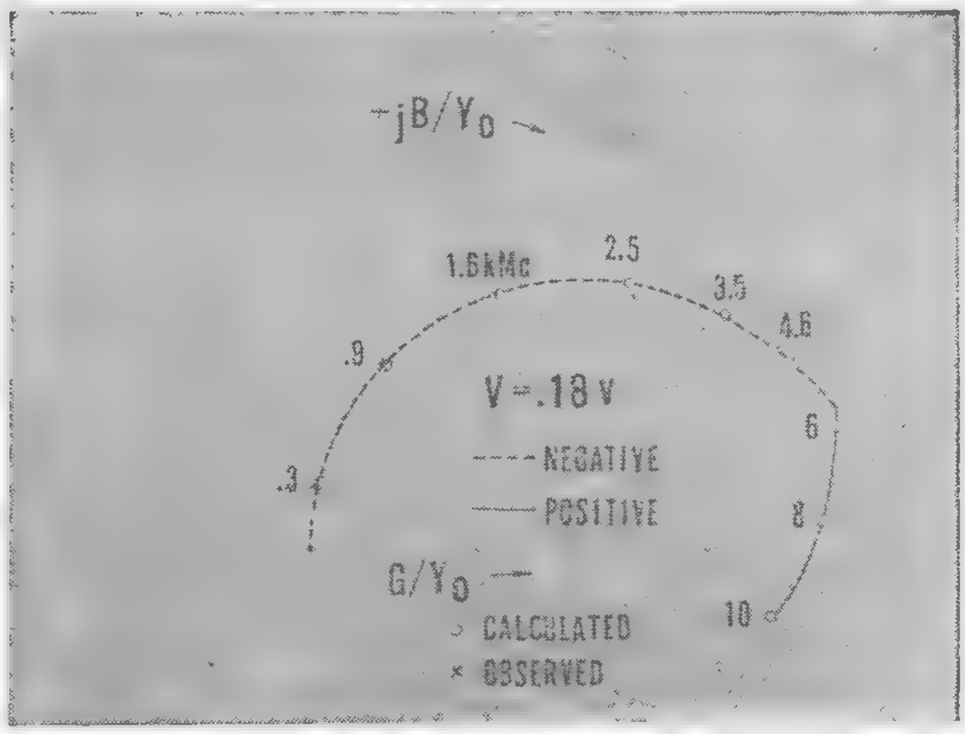



Figure 8—Comparison of calculated and observed admittance. Bias voltage is set at the maximum negative conductance.

## SESSION II: Microwave Amplifiers

### 2.2: Some X-Band Microwave Esaki-Diode Circuits

R. Trambarulo

Bell Telephone Laboratories, Inc.

Holmdel, N. J.

DURING THE PAST YEAR the *Esaki* diode has become firmly established as a microwave element. Several investigators have reported oscillators operating at X band with germanium diodes[1,2]. Gallium-arsenide units have oscillated with fundamental frequencies as high as 103 *kMc*[3]. Amplifiers have been operated up to 26 *kMc*[4,5]. The high-frequency limit of usefulness appears to be dictated by the junction capacity rather than by transit time of the electrons.

An equivalent circuit of a small-diameter *Esaki* junction appears in Figure 1. Any inductance associated with the mounting is not included, but may be considered a part of the associated microwave structure. The circuit elements depend upon voltage and may be taken either as incremental or as average values depending upon the degree of voltage excitation of the diode.

### *Circuits*

A simple microwave transmission-line equivalent circuit of an *Esaki*-diode oscillator or amplifier is shown in Figure 2. At resonance $\omega C' + Im\ (Y) = O$. When $G' > Re(Y)$, oscillations grow until the average value of $G'$ equals $Re(Y)$. It is seen from Figure 3 that oscillations can take place at more than one frequency. This multimoding has been observed experimentally. If circuit parameters are altered so that $G' < Re(Y)$, the circuit becomes a reflection amplifier. An experimental conical transmission line cavity of Figure 4 has been operated both as an amplifier and as an oscillator. This structure has several advantages for experimental circuits: (1) The diode mounting is a part of the transmission line so that diode lead inductances are reduced; (2) the dominant mode in conical transmission line has no cutoff frequency which simplifies circuit analysis; (3) the load conductance may be varied by rotating the plane of the loop. The main disadvantage is the lack of frequency tuning. Amplifiers differ from oscillators only in loop size and diode impedance range.

### *Diodes*

Both germanium and gallium-arsenide diodes have been operated in these circuits at *X* band. Diodes were integral parts of the cavities. After the cavities had been assembled, small area junctions were formed electrically. Only extremely heavily doped semiconductors giving *RC* products lower than $10^{-10}$ seconds were used.

### *Oscillators*

With certain simplifying assumptions the *Van der Pol* differential equation describes approximately the behavior of an *Esaki*-diode microwave oscillator. From it one finds that the power output should be a parabolic function of bias voltage, and that the maximum power output is

$$\frac{3}{16}\ (V_{valley}-V_{peak})\ (I_{peak}-I_{valley}).$$

These predictions are in approximate agreement with experiment, as seen in Figure 5. Gallium-arsenide diodes allow larger voltage swings than germanium units of the same impedance and are capable of higher power output. As high as half of a milliwatt has been obtained from a arsenide alloyed junction diode oscillating at 7.5 *kMc*.

### *Amplifiers*

In the reflection-type amplifier of Figure 6, the input and output signals are separated by a circulator. The gain is adjusted by rotation of the coupling loop. Stable gains in excess of 35 db have been obtained. At gain of 20 db, bandwidths are about 20 to 30 *Mc*. Measured noise figures at 11 *kMc* are typically 11.5 db for gallinum-arsenide units and about 7 db for germanium diodes.

---

[1] Hall, R. N., "Tunnel Diodes," *IRE Transactions on Electron Devices*, p. 1-9; January, 1960.

[2] Nelson, D. E., and Sterzer, F., "Tunnel-Diode Microwave Oscillators with Milliwatt Power Outputs," *IRE Wescon Convention Record*, Part I, p. 68-73; 1960.

[3] Burrus, C. A., "Millimeter Wave Esaki Diode Oscillators," *Proc. IRE;* in press.

[4] Yariv, A., Cook, J. S., and Butzien, P. E., "Operation of an Esaki Diode Microwave Amplifier," *Proc. IRE*, p. 1155; June, 1960.

[5] Trambarulo, R., "Esaki Diode Amplifiers at 7, 11, and 27 kMc," *Proc. IRE;* in press.

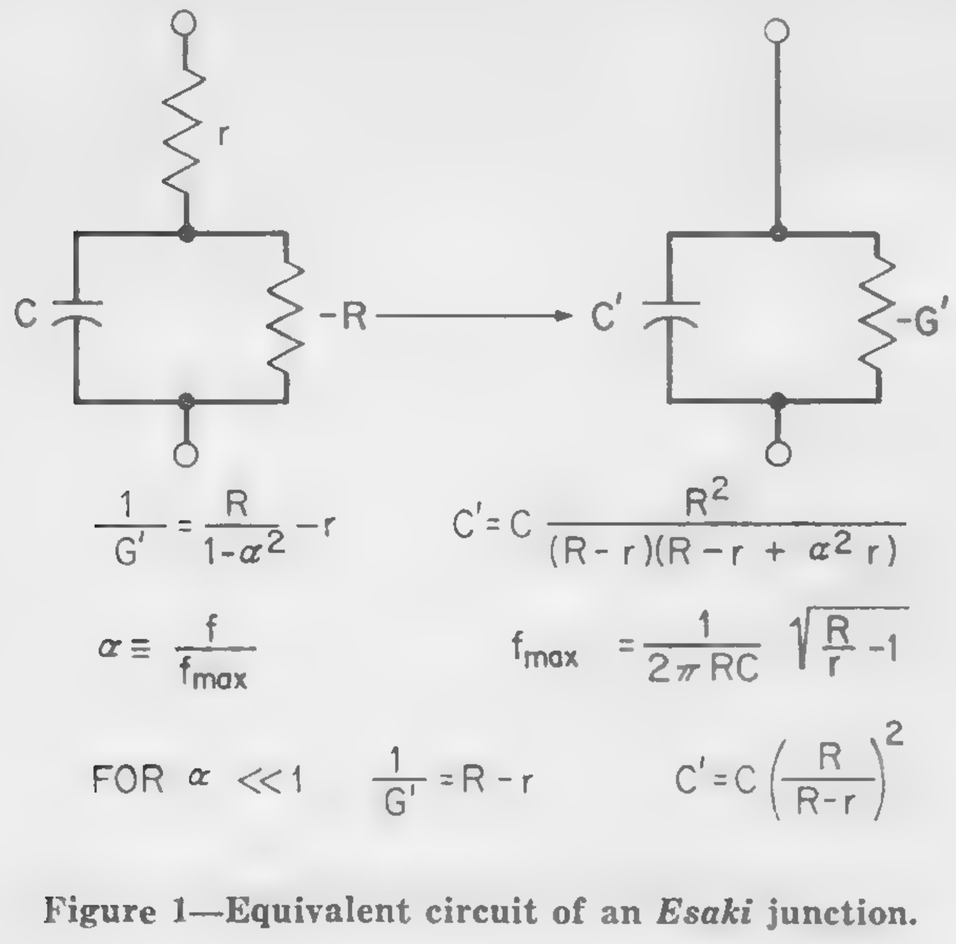



**Figure 1—Equivalent circuit of an *Esaki* junction.**

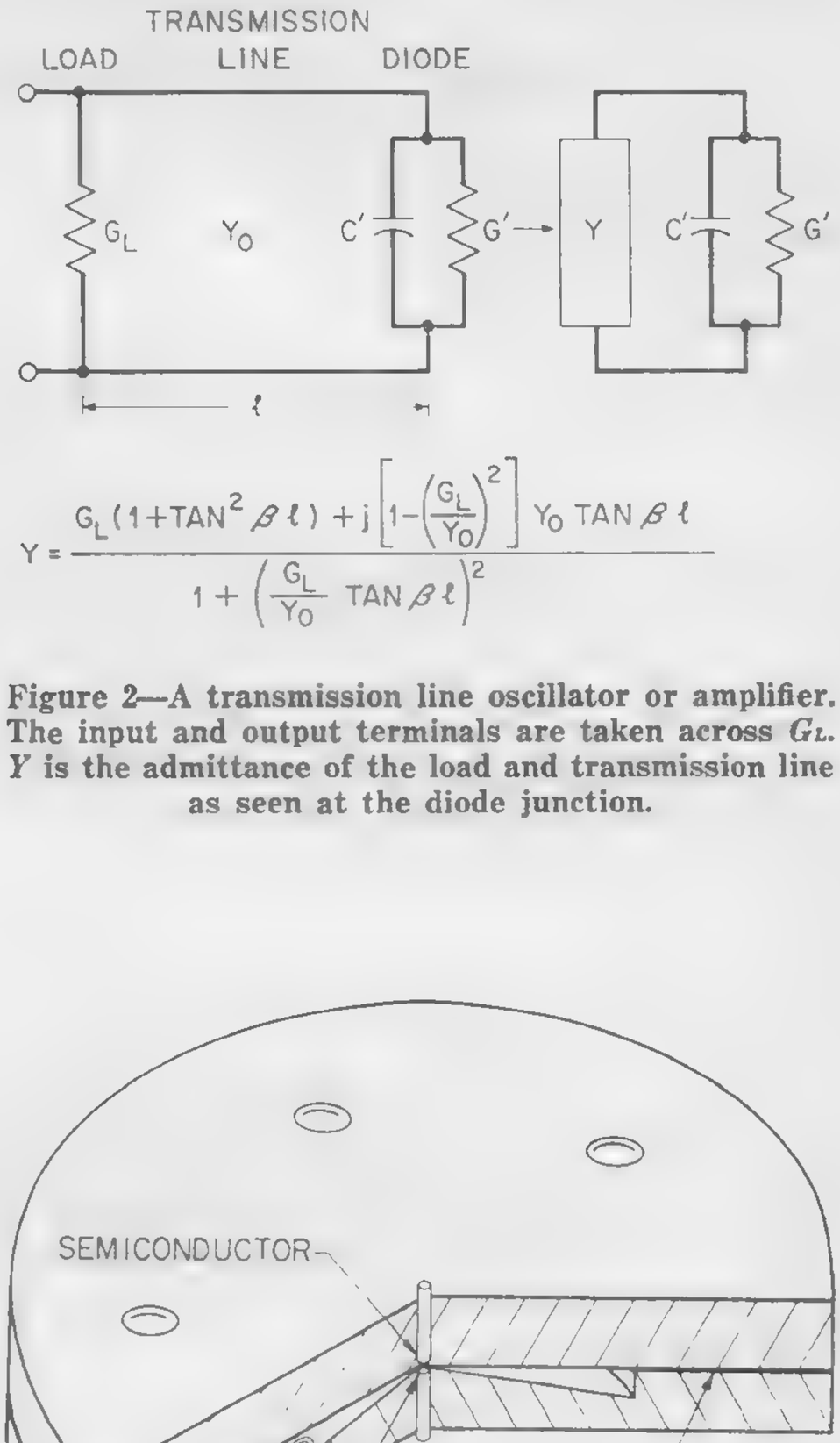



**Figure 2—A transmission line oscillator or amplifier. The input and output terminals are taken across $G_L$. $Y$ is the admittance of the load and transmission line as seen at the diode junction.**

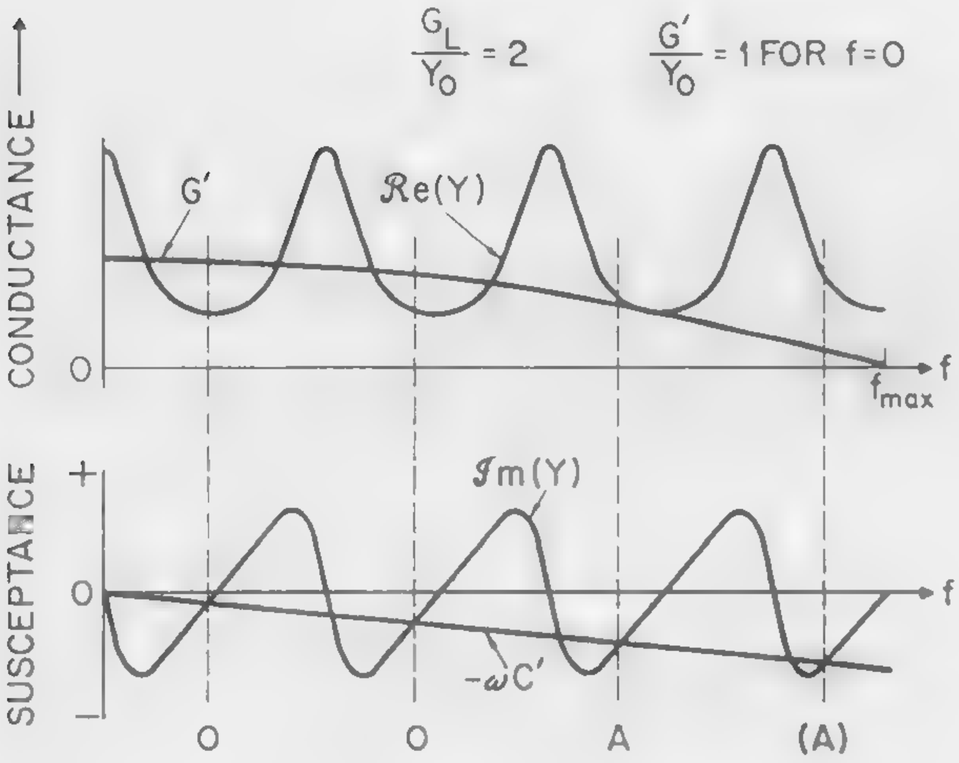



**Figure 3—A plot of the real and imaginary parts of $Y$ (Figure 2) and of the diode admittance as a function of frequency. At susceptance crossings marked *O*, oscillations can occur. Amplification can take place in bands centered near *A* if oscillations at *O* are quenched.**




**Figure 4—A practical *Esaki*-diode circuit. The circuit will operate either as an oscillator or amplifier in *X* band for a cavity diameter of 0.5-inch with either *GaAs* or *Ge* diodes having peak currents of about 1 *ma*.**

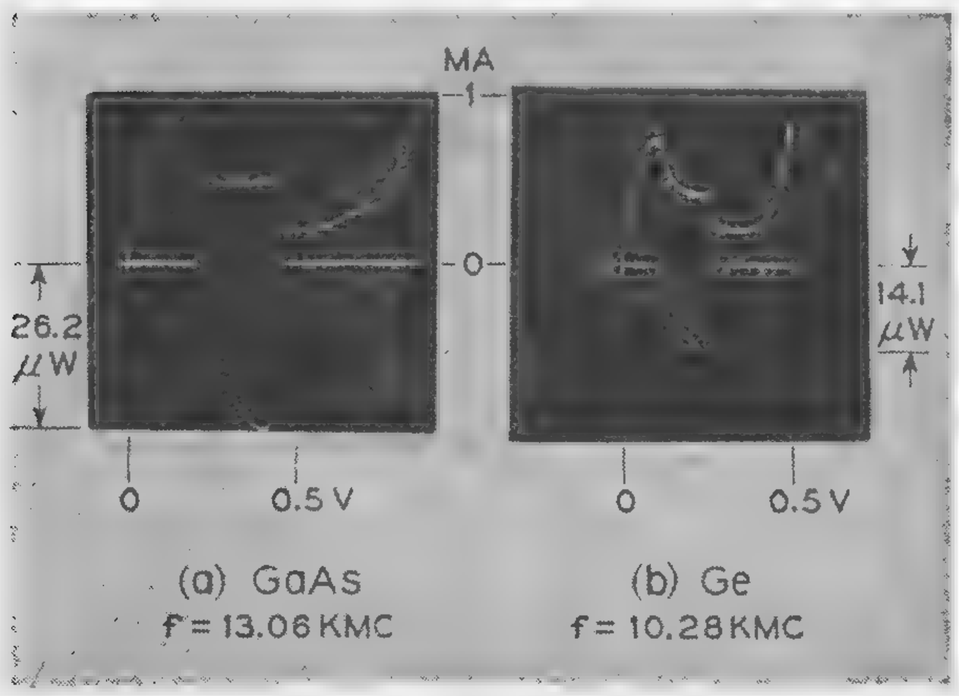



**Figure 5 — Current-voltage characteristics (upper traces) and detected power output (lower traces) of *Esaki*-diode oscillators.**


AT RESONANCE

$$F - 1 = \left(1 - \frac{1}{g}\right)\left[\frac{G'}{G'-G_1}\,\frac{1}{1-\alpha^2}\left(\frac{qI_0R}{2kT_0} + \frac{T_d}{T_0}\,\alpha^2\right) + \frac{G_1}{G'-G_1}\right]$$

$g$ = POWER GAIN

$\alpha = \frac{f}{f_{max}}$ $\quad T_d$ = JUNCTION TEMPERATURE

**Figure 6—Circuit arrangement for an amplifier with the input and output separated with a circulator. At resonance, an expression for the excess noise figure is given. Circuit losses are represented by $G_1$.**

## SESSION II: Microwave Amplifiers

### 2.3: Parametric Oscillation and Amplification Using Esaki Diodes

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Research and Development Center, Japan Defense Agency

Tokyo, Japan

EFFICIENT PARAMETRIC OSCILLATION and amplification is possible by applying appropriate *dc* bias voltage to *Esaki* diodes which operates the diode in the positive resistance region below the peak point or above the valley point of current. By superimposing an *ac* excitation voltage the diodes can be made to alternate between the positive and negative resistance regions. The element receives energy during the half-cycle of positive resistance and delivers energy during the half-cycle of negative resistance. Accordingly, when *Esaki* diodes are operated in the manner described, the existence of subharmonics and the phenomenon of parametric oscillation are observed.

A parametron circuit can be constructed with a circuitry identical to that of semiconductor barrier capacitance parametron[1], and the method of amplification is similar to that of variable reactance amplifier. The *Down* Converter[2] is quite similar to the one herein described in its operation.

Parametric oscillation and amplification are generally possible by means of any circuit elements of dynatron characteristics, including discharge characteristics through gas. A parallel tuned circuit having an angular frequency of $\omega$ is shown in Figure 1*(A)*. In *(B)* is shown the oscillation domain given by (4) in Figure 2. A parametron circuit, which does not always necessitate self or *dc* bias voltage is illustrated in Figure 3.

With an excitation frequency of 24 *Mc* an oscillation of 12 *Mc*, with its *O* and $\pi$ phases were observed.

Figure 4 shows the variation in the characteristics for various values of *RC* time constant.

The *Esaki*-diode parametron, because of its flat oscillation characteristics and its great value of modulation factor in the parameter term, is a promising element for microwave computing devices.

The subharmonic $fo/2$, its even multiples $2f_o/2$, $4f_o/2$ . . . and its odd multiples $3f_o/2$, $5f_o/2$ . . . were observed with the parametron circuit shown in Figure 3. For example, the loss in downward frequency conversion, to $f_o/7$ was about 40 *db*.

Higher harmonics up to $20/f_o$ were easily observed, when the exciting power of the fundamental frequency $f_o$ (0.5 ~ 5 *Mc* was applied to the circuit with a series tuning unit. The frequency conversion loss was, in this case, about 20 *db* at $6/f_o$ and about 45 *db* at $20/f_o$.

In both cases of conversions, the loss observed includes input and output coupling. The net loss in the conversion itself is, therefore, less than the value cited. The waveform of the voltage and current through the diode were expanded into *Fourier* series to evaluate the power in the higher harmonic components. The ratio in power distribution showed good agreement with the losses observed in the frequency conversion.

An equivalent circuit of a parametric amplifier of the variable conductance type appears in Figure 5; derived power gain and noise figure is shown in Figure 6.

Figure 7 shows the computation of power gain of a variable-impedance parametric amplifier. The gain and the bandwidth of amplifier and down converter were over 20 db and 200-300 *kc* in the *hf* band. The characteristics in the *vhf* band, i.e., gain versus excitation power, are given in Figure 8. The amplification phenomenon, which has no idling circuit is somewhat similar to a super-regenerative amplifier. Steep rise in gain was observed with increasing excitation power, when the regenerative amplification $fs \rightarrow fi \ldots fs$ was provided by an idling circuit. A gain of 20 *db* and a bandwidth of 8 *Mc* were observed with an *L-band* amplifier of the reflection type. Amplification was also observed at 4 *Gc* with reflection and travelling-wave types, exciting frequency being 7 *Gc*.

Amplification by excitation, however, requires a driving oscillator for practical applications. It seems more advantageous to employ a *dc*-biased diode in its negative resistance region. Down converter would be preferred as a low noise preamplifier in the microwave region.

The authors express their thanks to Professors Watanabe and Nishizawa for their helpful suggestions.

[1] Kiyasu Z., and others, "Parametric Excitation using Barrier-Capacitance of Semiconductor," *J. of the Inst. of Electrical Communciation Engineers of Japan*, p. 162; Feb., 1957.

[2] Chang, K. K. N., "Low Noise Tunnel-Diode Down Converter Having Conversion Gain." *Proc. I.R.E.*, p. 854; May, 1960.

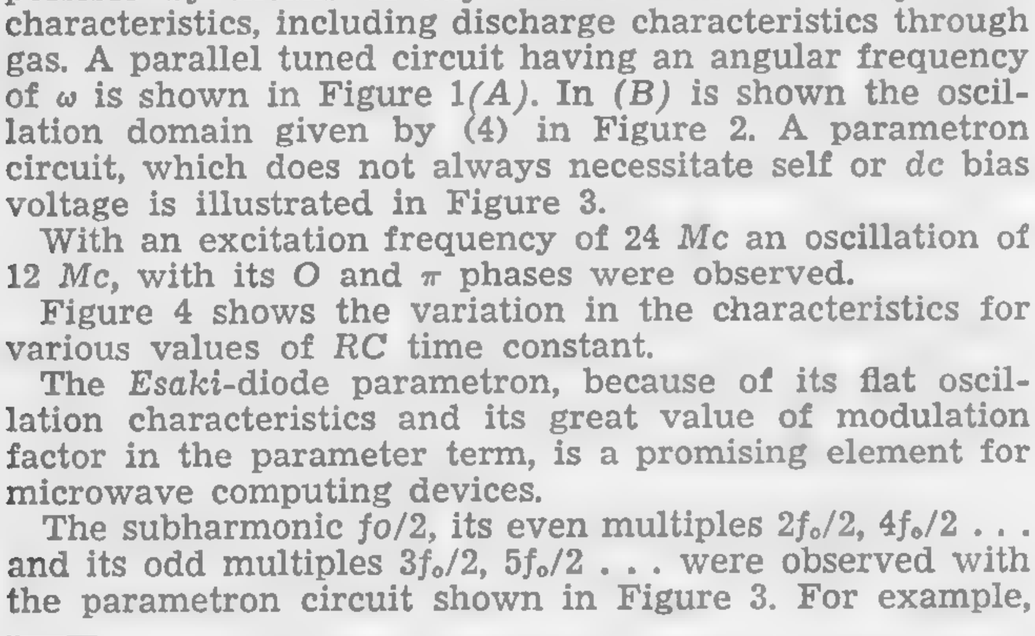



**Figure 1—*(a)* Equivalent circuit of parametron; *(b)* parametric oscillation domain (hatched area).**

$$\int \frac{v}{L}dt + vG + \frac{d}{dt}(Cv) = 0 \qquad (1)$$

$$v = v_0 e^{\lambda t}\sin(\omega t - \theta) \qquad (2)$$

$$\left(\frac{\omega\gamma G_0}{2C}\right)^2 = \left(\omega^2 - \frac{1}{LC}\right)^2 + \left(2\lambda\omega + \frac{G_0\omega}{C}\right)^2$$

$$\lambda = \pm\frac{G_0}{4C}(\gamma \mp 2) \qquad (3)$$

$$\gamma = 2\Gamma$$

$$\Gamma = \frac{1}{G_0^2}\left(\omega C - \frac{1}{\omega L}\right)^2 + 1 \qquad (4)$$

**Figure 2—When the exciting angular frequency is 2 ω, equation *(3)* holds in the case of resonance, as seen from equations *(1)* and *(2)*, with the assumption of $\lambda \ll \omega$ and disregarding the terms of over 3 ω.**

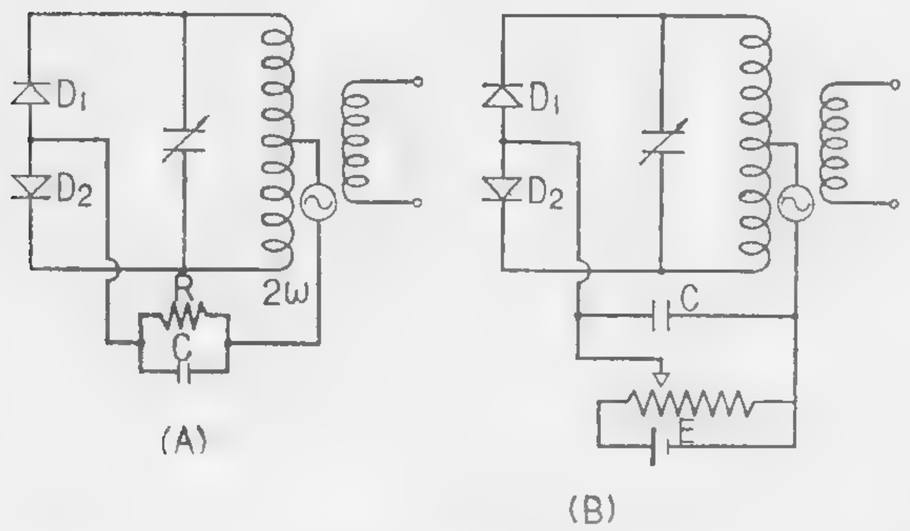



**Figure 3—Parametron circuit, *(a)* Self-biased; *(b)* *dc*—biased.**

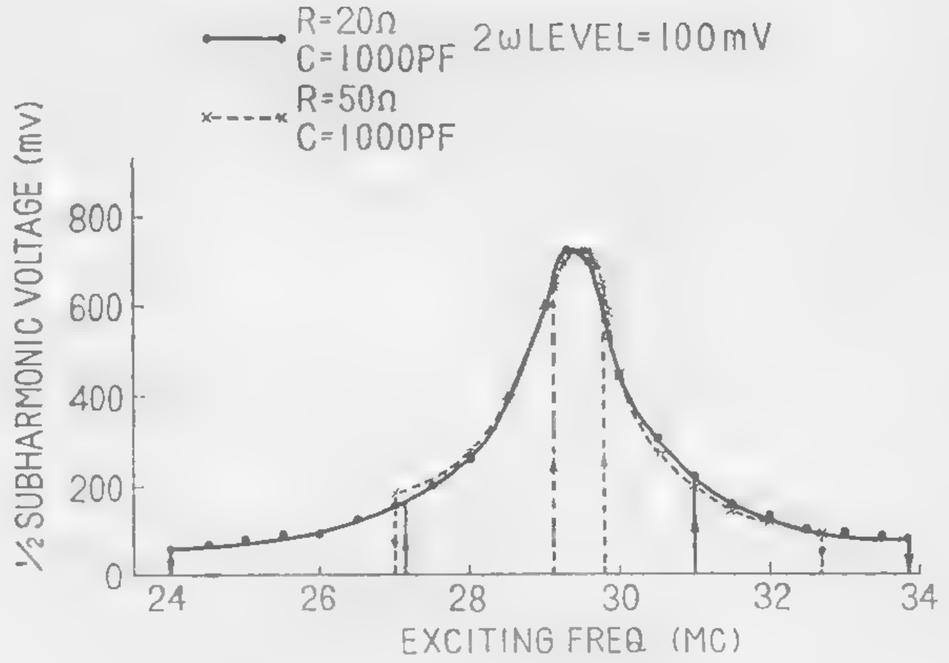



**Figure 4—Parametric oscillation characteristics which differ from the conventional parametron of *L* and *C* type. The domain of oscillation extends symmetrically, with rises and falls on both sides of the center frequency.**

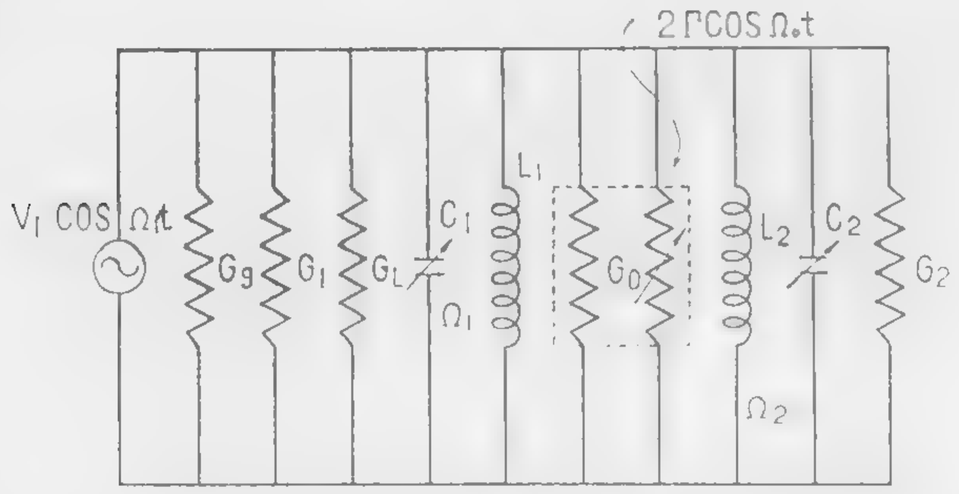



**Figure 5—Equivalent circuit of a variable conductance parametric amplifier. Excitation, signal and idling angular frequencies are $\Omega_0$, $\Omega_1$, and $\Omega_2$, respectively.**

$$G = G_0(1 + 2\Gamma\cos\Omega_0 t), \quad \Omega_0 = \Omega_1 + \Omega_2$$

$$G(\Omega_1) = G_0\left(1 - \frac{\Gamma^2 G_0}{G_{T2}}\right), \quad G(\Omega_2) = G_0\left(1 - \frac{\Gamma^2 G_0}{G_{T1}}\right)$$

$$\text{GAIN} = \frac{4 G_g G_L}{G_{T1}^2\{1 - G'\}^2}, \quad G' = \frac{(\Gamma G_0)^2}{G_{T1} G_{T2}}$$

$$G_{T1} = G_1 + G_g + G_L + G_0, \quad G_{T2} = G_0 + G_2$$

$$F = 1 + \frac{G_1}{G_g} + \frac{G_e}{G_g} + \frac{G_L}{G_g} + \frac{G' G_{T1}}{G_g}\left(1 + \frac{G_e}{G_{T2}}\right), \; G_e = \frac{e I_D}{2kT}$$

**Figure 6—Evaluation of power gain and noise figure on the basis of equivalent circuit of Figure 5. The expressions $G(\Omega_1)$ and $G(\Omega_2)$ show that they are both negative, when $\Gamma$ is greater than unity.**

$$\begin{bmatrix} i_1 \\ i_2^* \end{bmatrix} = \begin{bmatrix} g_0 + j\omega_1 C_0 & g_3 + j\omega_1 C_3 \\ g_3 - j\omega_2 C_3 & g_0 - j\omega_2 C_0 \end{bmatrix} \begin{bmatrix} V_1 - i_1 R_S \\ V_2^* - i_2^* R_S \end{bmatrix}$$

$$\text{GAIN} \approx \frac{4 G_g G_L}{G_{T1}^2\left[1 + \dfrac{G_{T1} R_S\{(\alpha+\beta)^2 + \gamma^2\} - (\alpha+\beta)}{\{G_{T1} R_S(\alpha+\beta) - 1\}^2 + (\gamma G_{T1} R_S)^2}\right]^2}$$

$$= \frac{4 G_g G_L}{G_{T1}^2\{1 - (\alpha+\beta)\}^2} \quad \text{WHEN } R_S = 0$$

$$\alpha = \frac{g_3^2}{G_{T1} G_{T2}}, \quad \beta = \frac{\omega_1 \omega_2 C_3^2}{G_{T1} G_{T2}}, \quad \gamma = \frac{g_3 C_3(\omega_1 - \omega_2)}{G_{T1} G_{T2}}$$

**Figure 7—Evaluation of power gain of a variable impedance parametric amplifier; $\alpha$ and $\beta$ are negative resistance terms associated to the variable conductance and capacitance, respectively, while $\gamma$ refers to both.**

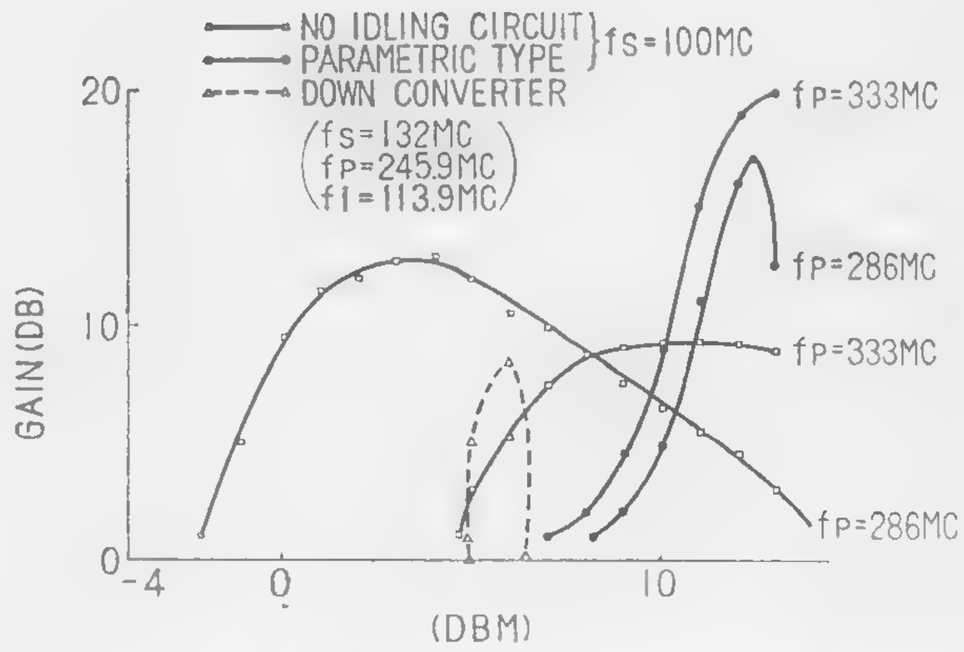



**Figure 8—The gain of the amplifier with and without the idling circuit versus exciting or pumping power, and its characteristic of down converter.**

## SESSION II: Microwave Amplifiers

### 2.4: High-Frequency and High-Power Operation of Tunnel Diodes*

C. S. Kim and J. B. Hopkins

Electronics Lab., General Electric Company

Syracuse, N. Y.

Representing a tunnel diode by the equivalent circuit of Figure 1, the cutoff frequency $f_c$ and the self-resonance frequency $f_r$ are given by[1]

$$f_c = 1/2\pi \quad g/C \quad \sqrt{1/R_S\, g - 1} \text{ and}$$
$$f_r = 1/2\pi \quad \sqrt{1/LC - g^2/C^2}$$

The voltage characteristics of a tunnel diode are determined by the energy level of the junction material and hence are essentially fixed for a particular material. To increase the output power, it is necessary to increase the diode current, i.e., the junction area. Assuming $g$ and $C$ are proportional and $R_S$ is inversely proportional to the junction area, $f_c$ is independent of the junction area. On the other hand, $f_r^2$ is approximately inversely proportional to the junction area, if it is assumed that the inductance $L$ is constant.

To maximize $f_r$, the smallest possible internal series inductance $L_i$ must be obtained. $L_i$ is limited by the lead inductance of the device. Therefore, to oscillate at frequencies above the self-resonance frequency, it is necessary to insert a capacitance[2] $C'$ (or negative inductance $L'$) in series with $L_i$. The oscillation frequency $f_r'$ ($\omega_r'^2 = \omega_r^2 + 1/L_i - L'$; $L_i - L' > 0$) can then be extended beyond $f_r$. The maximum oscillation frequency is ultimately limited by $f_c$.

When the oscillation frequency is made smaller than $f_c$, the output power increases as shown in Figure 2. The oscillation here is considered to be sinusoidal or almost sinusoidal. The power and frequency are normalized to the factor $gR$ and $\omega C/g$, respectively. The power delivered by the negative conductance element divides between $R_2$ and $R_L$. The power delivered to $R_S$ is represented by the horizontal line $B$, and the power delivered to the load $g(R\text{-}R_S)$ is the difference between curves $A$ and $B$. The intersection, $P$, is the cutoff frequency where the output power becomes zero.

At microwave frequencies, the capacitance (or negative inductance) element becomes frequency dependent and oscillation will not only take place at $f_r'$, but also at other frequencies. The negative inductance may be obtained by means of a short-circuited transmission line with length $l$ within the range $\lambda/4 < l < \lambda/2$ at the desired oscillation frequency. However, at a lower frequency $f''$, the line behaves as an inductance which satisfies another resonance condition, and oscillation can occur simultaneously at two frequencies. This undesirable oscillation at a lower frequency generally becomes the dominant mode, and it can even produce high harmonics. The lower frequency oscillation reduces the magnitude of the average negative conductance of the diode. This reduces the power output at the desired frequency. It is therefore desirable to suppress undesired oscillation.

Figures 3 and 4 show two possible strip-line circuit configurations that will suppress these oscillations. In Figure 3, a resistance $R_1$ is placed a distance $\lambda/4$ from the short circuited end of the transmission line, where it does not have an appreciable effect at the desired frequency. However, at other frequencies, especially at lower frequncies, $R_1$ will be effective in damping out the undesired oscillations. Figure 4 shows another possible configuration. If $R_1$ is a *dc* resistance, $R_1$ must be smaller than $1/g$. Of course, $R_1$ and $R_2$ are not restricted to be *dc* resistances and could be *ac* impedances with a proper *dc* value.

A cavity-type radial transmission line configuration corresponding to Figure 3 is shown in Figure 5. The cavity reactance facing the diode is shown as a function of $kr$ in Figure 6. In Figure 7, the reactance curves, as a function of frequency, which could provide lower frequency oscillations, are plotted for given values of $C$. The reactance presented to the input of the diode by the cavity is also shown. The intersections represent possible undesired low frequency oscillations. These oscillations are damped out by $R_1$ and the impedance termination in Figure 5. A single diode can be replaced by a ring-shaped diode or several spot diodes in a ring configuration to improve its performance.

* Work supported by Bushps Contract Nobsy—81320

[1] Nelson, D. E., and Sterzer, F., "Tunnel-Diode Microwave Oscillators with Milliwatt Power Outputs," *IRE WESCON Convention Record Part* 1, p. 68; 1960.

[2] Kim, C. S., "Circuit Application of Tunnel Diodes" R59ELS111, *G.E. Internal Publication*, p. 35-38; Dec. 1959. Independent work from RCA is published in *reference* 1.

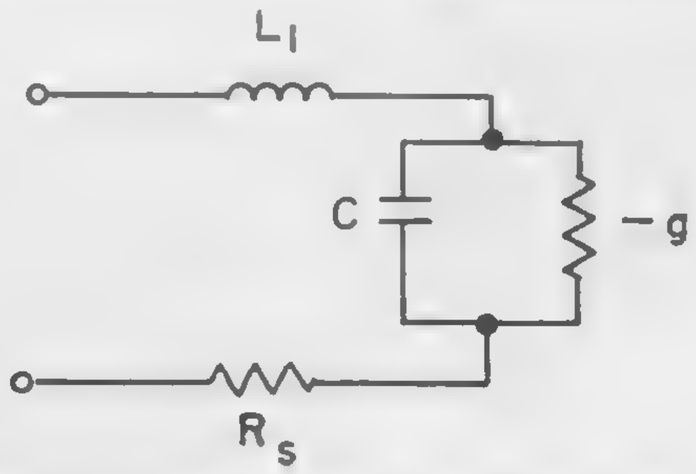



**Figure 1—Tunnel diode equivalent circuit.**

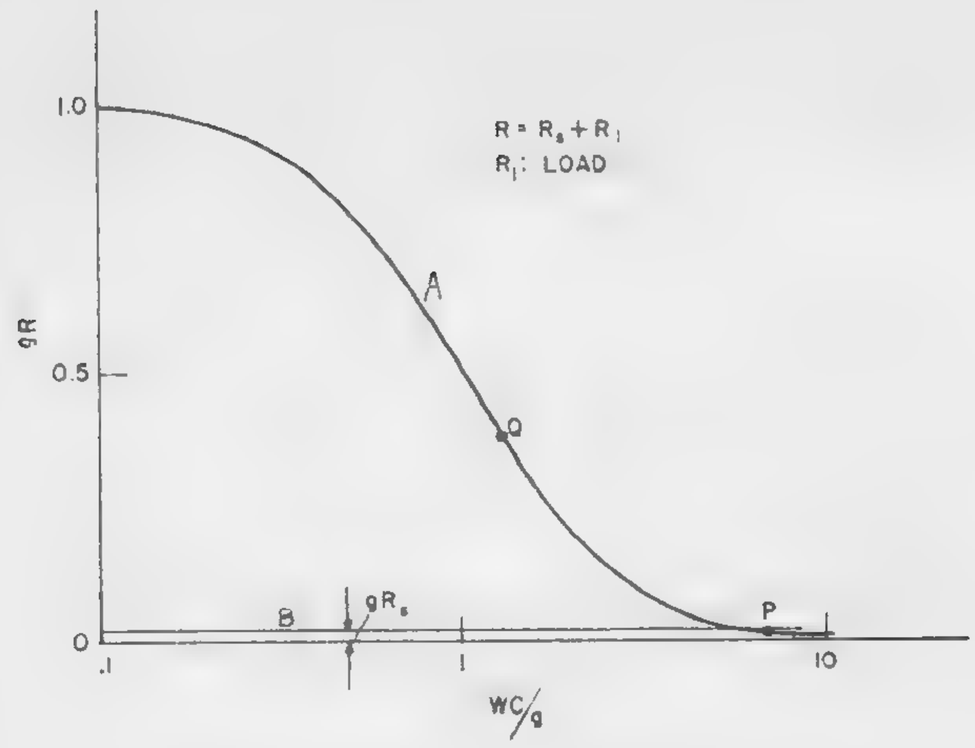
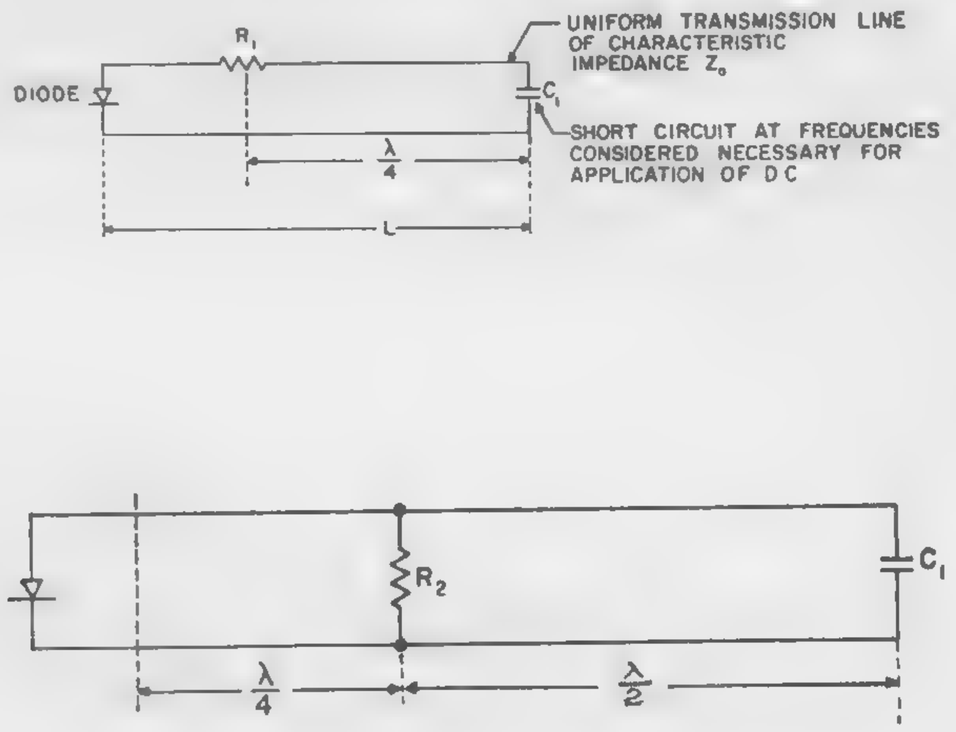



**Figure 2—Plot for $gR$ versus $WC/g$.**




**Figures 3 and 4—Circuits to suppress lower frequencies.**

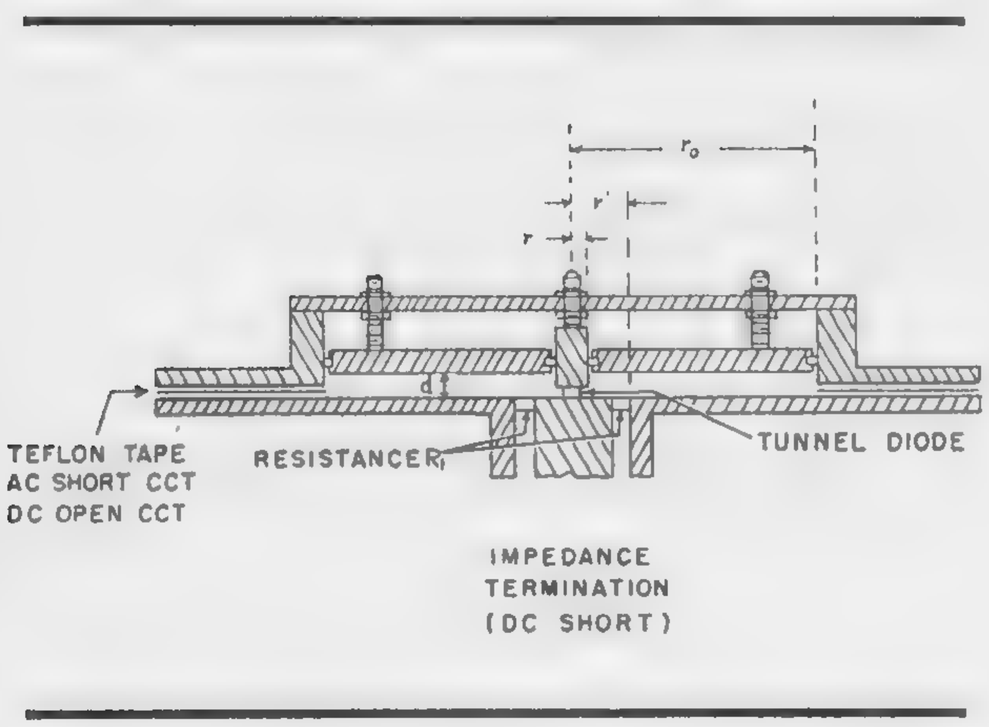



**Figure 5—Radial transmission line cavity.**

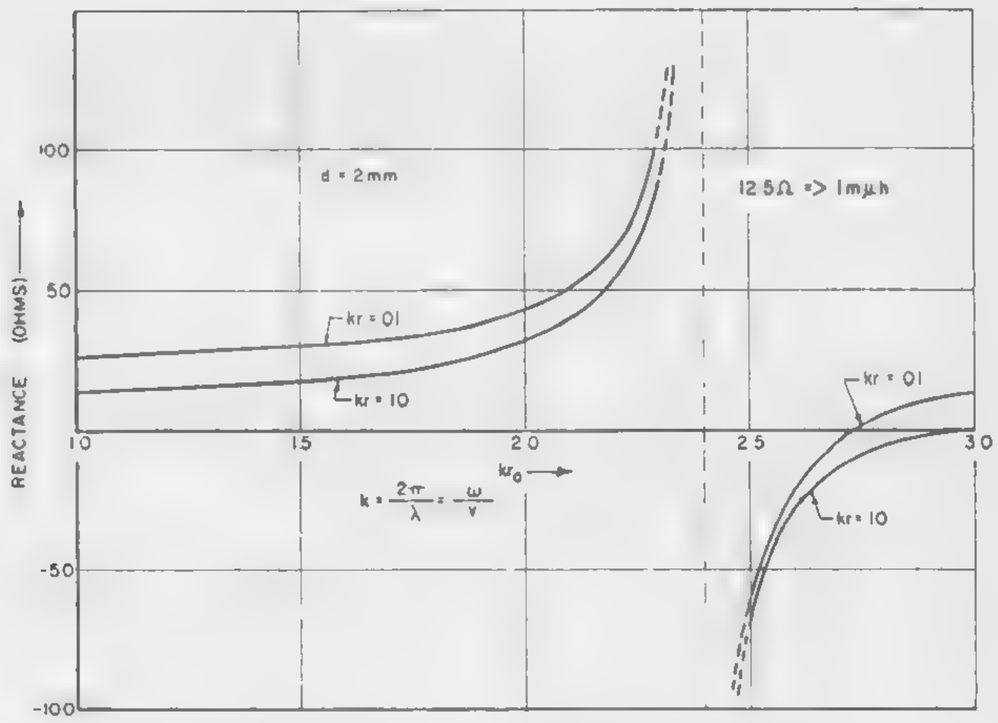



**Figure 6—Reactance at input versus $kr_o$.**

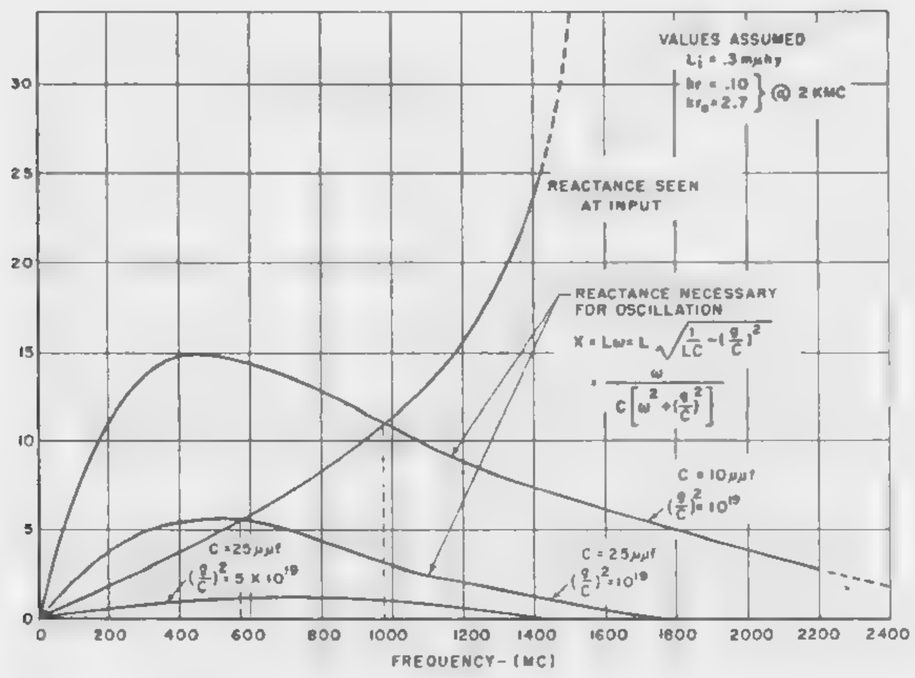



**Figure 7—Reactance at input versus frequency reactance necessary for oscillation versus frequency.**

## SESSION II: Microwave Amplifiers

### 2.5: Waveguide Parametric Amplifiers

B. C. De Loach Jr.

Bell Telephone Laboratories, Inc.

Holmdel, N. J.

TWO ESSENTIALLY DIFFERENT METHODS of placing a diode contained in a *Sharpless* type cartridge (Figure 1) in a waveguide circuit have been employed. In one of these, cylindrical rods essentially form extensions of the diode end caps and make connections with the waveguide walls. In the other, the waveguide height is reduced until it is the same height as the quartz window (.050-inch) of the diode, and the end caps thus are absorbed as part of the waveguide walls. The frequency sensitivity of these two basic structures is remarkably different.

#### *The Extended Rod Structure*

If a .050-inch length section is removed from a ⅛-inch rod attached to the center of the broad faces of a .400-inch x .900-inch *i.d.* *X*-band waveguide one obtains the frequency response shown in Figure 2, provided one edge of the resulting gap is .050-inch distant from the plane of the broad face of the waveguide. If one now drills .080-inch diameter holes to a depth of .050-inch in the faces of two ⅛-inch rods and inserts different diode components, the effect on the resonant frequency of the transmission characteristic of Figure 2 will appear as in Figure 3; the effect of placing the components at different distances from the broad walls is also included here.

#### *Reduced Height Waveguide Structure*

In the other structure, which in *X*-band guide would correspond to a .050-inch x .900-inch waveguide, we have in the absence of the crystal an ordinary waveguide whose frequency response is well known.

Although one may have an intuitive feeling as to the appropriate choice between these two circuits for utilization in a parametric amplifier the decision is not an obvious one. This choice is a function of many variables and in practice depends upon the job the amplifier is required to do.

#### *Experimental Results*

Two experimental degenerate amplifiers typifying the two circuit extremes will be discussed.

The first type is shown in Figure 4. This amplifier has produced typically 80 to 100 *Mc* bandwidth centered at 11.55 *kMc* with 10-*db* gain and 3.2 to 4-*db* double-sideband noise figures. This operation required from 100 to 200 *mw* of pump power. A modified circuit, as shown in Figure 5, reduced the power required from 30 to 100 *mw*, while providing essentially the same performance characteristics. Special diodes in this modified circuit have produced 10-*db* gain with 21 *Mc* bandwidth and a 3.2-*db* double-sideband noise figure with only 1.5 *mw* of pump power. Circulator or one port operation has always been used with this amplifier.

The second type of amplifier is presented in Figure 6. This amplifier employs a so-called *dam* cavity to provide the major signal tuning element. This amplifier has provided 1,020-*Mc* bandwidth with a 1-db ripple centered at 11.4 *kMc* with 14.2-*db* gain and a 3.1-*db* double-sideband noise figure and is operated as a two-port or transmission device. One port or circulator operation can also be used. Pump power requirements at present range from 100 to 200 *mw*, but should be considerably reduced by further circuit modifications.

A 30-*kMc* amplifier is shown in Figure 7. Subharmonic oscillations were obtained with as little as 28 *mw* of pump power.

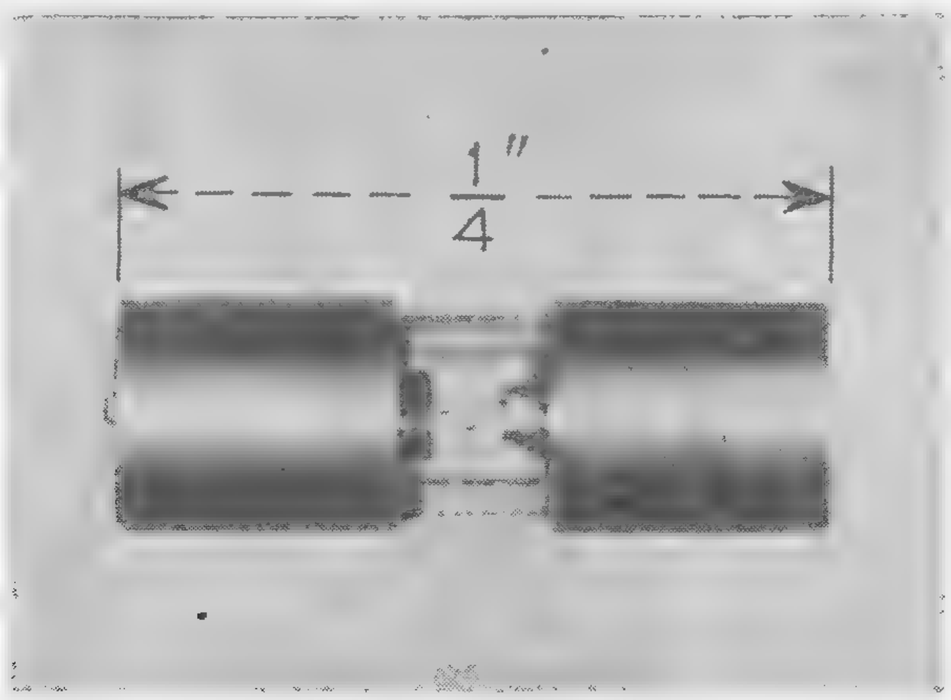



**Figure 1—Photograph of crystal cartridge.**

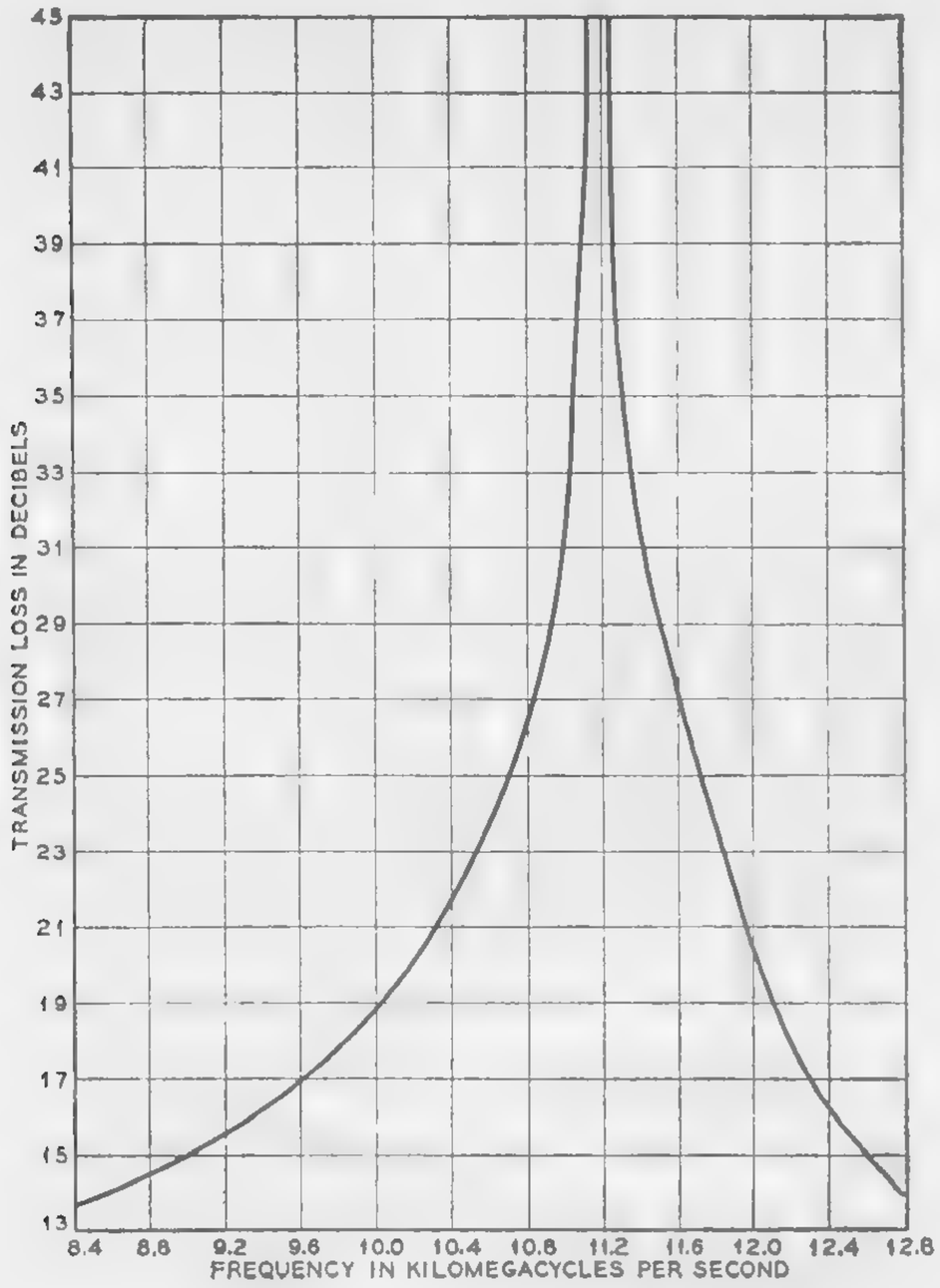



**Figure 2—Transmission characteristic of a resonant post structure.**

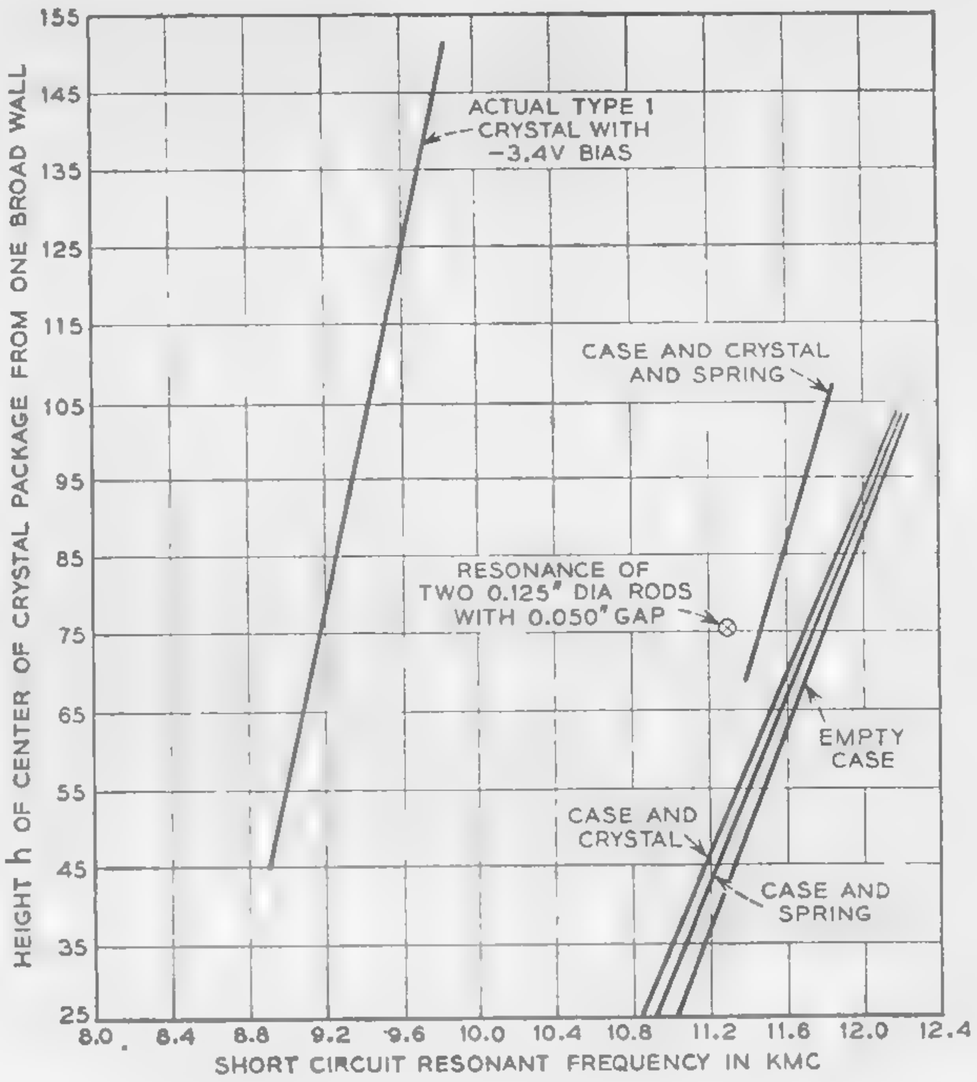



**Figure 3—Effects of different variables on the resonant frequency of the extended rod structure.**

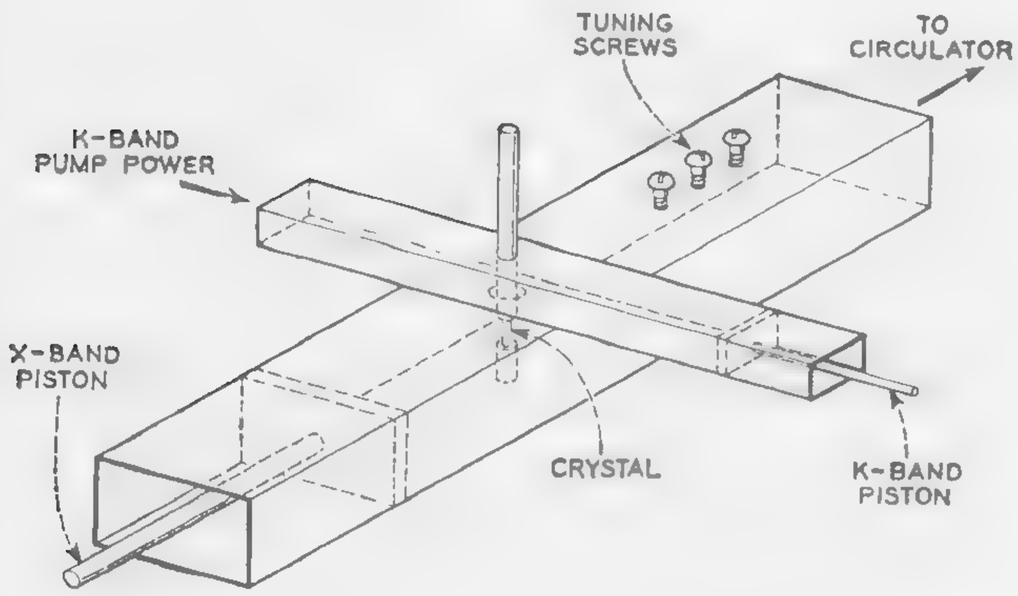
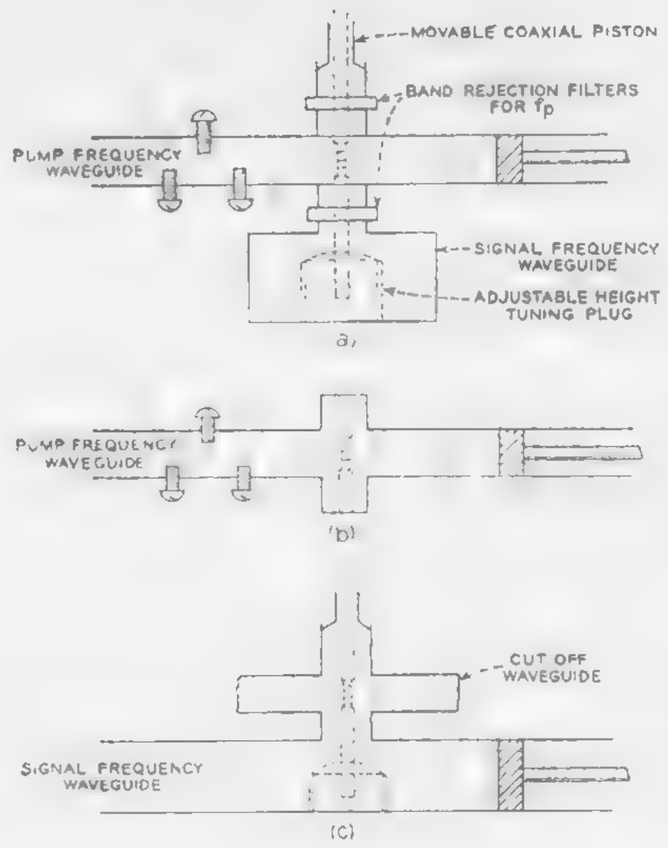



**Figure 4—Experimental amplifier employing the extended rod structure.**




**Figures 5a, b, c—A special low pump power amplifier employing a modification of the extended rod structure is illustrated in *(a)*; pump-frequency equivalent circuit is shown in *(b)*, while *(c)* presents the signal (and idler) frequency equivalent circuit.**

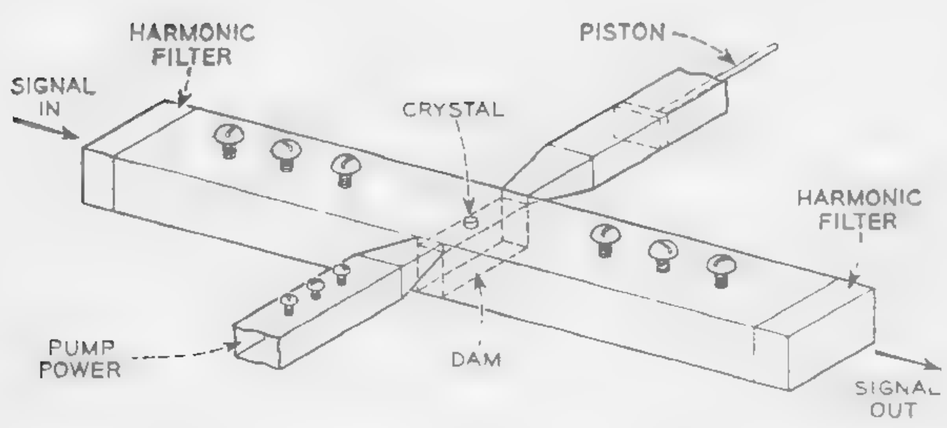



**Figure 6—Experimental amplifier employing the reduced height waveguide structure.**

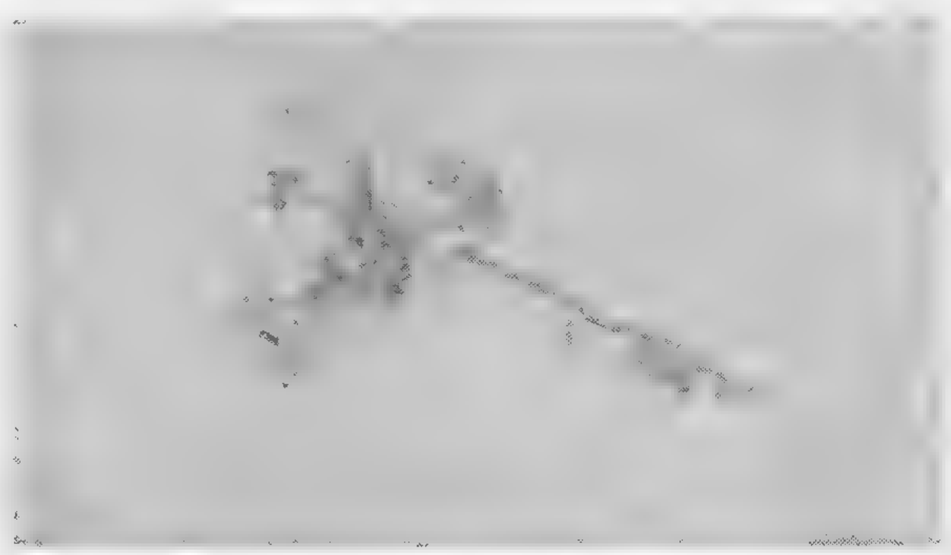


**Figure 7—A 30-*kMc* amplifier.**

# WEDNESDAY, FEBRUARY 15, 1961 IRVINE AUDITORIUM (UNIVERSITY OF PENNSYLVANIA) . . . 1:45-2:45 P.M.

## Formal Opening of Conference

### Introductory Comments

Chairman of Conference—**T. R. Finch**, Bell Telephone Laboratories, Inc.

### Welcoming Remarks

**G. P. Harnwell**, President, University of Pennsylvania

### 1960 Conference Awards

Chairman, 1960 Conference—**A. P. Stern**, Electronics Laboratory, General Electric Company

### Invited Address

**J. G. Linvill**, Stanford Electronics Laboratories, Stanford University

**How Can Solid-State Electronics Mature Without Losing Its Youth?**

## SESSION III: Logic I

Chairman: J. J. Suran
Electronics Laboratory, General Electric Co., Syracuse, N. Y.

### 3.1: Parametron and Esaki Diode Progress in Japan

E. Goto
University of Tokyo
Tokyo, Japan

VARIOUS NEW CIRCUITS for *Esaki* diode logic have been proposed. *Oshima* and *Amano*[2] improved the diode-pair logic[1] so as to facilitate negation; Figure 1. They provided a separate power transformer for each diode pair so that the power circuits may have no common ground. Negation is made simply by reversing the polarity of coupling and the number of diodes are reduced to half of that required in the symmetric scheme[1].

*Komamiya*[3] proposed a hard oscillator scheme; Figure 2. Connecting a suitable *L, C, R*-circuit to an *Esaki* diode, an oscillator, which is not self-starting but triggerable by pulse or other oscillators, is formed. The oscillators are used both for memory cells and logical elements, and are specially suited for asynchronous logic. Transformers and wave guides can be used for coupling purpose because of the absence of *dc* component.

*Takahashi*[4] is developing an *Esaki* diode matrix memory for a very high speed computer*; Figure 3. The binary cell of the memory consists of an *Esaki* diode and a resistor, a buffer diode being used for each cell to reduce the attenuation of the read out signal.

*Yamamoto*[5] and *Fushimi*[6] have developed a subharmonic oscillator (Figure 4), where oscillation is generated by negative conductance and the frequency and phase is locked into ½ subharmonic. This scheme is called the *Esaki*-diode parametron by some authors since the same logical principle and almost the same circuitry as that of parametrons can be applied to it.

At our laboratory, a transformer coupled *dc*-free logic scheme is being studied[7]; Figure 5 and 6. The basic element consists of an *Esaki* diode pair, but transformers are used for coupling the pairs. Generally in *dc* coupled systems, the ratio of the control current $I_c$ to the output current $I_o$ of an *Esaki*-diode element is less than $1/N$, where $N$ is the number of logical branches. Using coupling transformer, the input and output impedances can be matched and the ratio can be improved as $1/N$. For instance, in a circuit having $N=9$ logical branches, the control current $I_c$ can be made three times larger than that in *dc*-coupled systems, which may result in three times less stringent tolerance for circuit parameters. Further, assuming that the buildup of signals is exponential, the square root in the ratio implies the possibility of doubling the clock frequency. Moreover, large freedom in negating signals, insulation from common ground currents, impedance-matching facility to transmission lines and delay lines are considered to be the other important advantages of the transformer coupling. The disadvantage of transformers, however, consists in the inability to transmit *dc* component. In our system, all of the signals are supposesd to take a form as shown in Figure 6. namely, every effective signal $x, y, z, \ldots$ is followed by its negative so as to eliminate the *dc* component. Free signals *(dc)* are obtained by suitable logical design, called *dc free logic*, rather than by special hardware. While in the *dc fl*, the information rate is half the clock rate, the information rate would be the same and the delay time for combinatorial operations would be halved compared with the *dc* coupled system.

Magnetic thin film parametrons have also been developed. Oshima[8] has replaced ferrite cores with vacuum-evaporated permalloy films and subharmonic oscillation has been obtained at 30 *Mc*. At our laboratory, parametrons using copper wires electroplated with permalloy have operated successfully at 6 *Mc* pump[9]; Figures 7 and 8. The mass production of uniform thin magnetic films has been the main problem of the yield of these parametrons.

---

* ETL Mark 6.

[1] Goto, E., et al, "Esaki Diode High Speed Logic," *Trans. I.R.E. on Electronic Computers*, p. 25; March, 1960.

[2] Oshima, S., and Amano, K., "Floating Power System for Esaki Diode Pair Logic," *Record of Meeting of PGEC of Inst. of Communication Engineers of Japan;* May, 1960.

[3] Komamiya, Y., "Asynchronous Logic by Esaki Diode Hard Oscillator," *PGEC of ICEJ;* Aug., 1960.

[4] Takahashi, S., "High Speed Esaki Diode Memory," *PGEC of ICEJ;* Aug., 1960.

[5] Yamamoto, T., "Parametric Excitation by Esaki Diodes," *PGEC of ICEJ;* Aug., 1960.

[6] Fushimi, K., "Esaki Diode Parametron," *PGEC of ICEJ;* Aug., 1960.

[7] Takahasi, H., Goto, E., and Ishida, H., "DC Free Logic for Esaki Diode," *PGEC of ICEJ;* Dec., 1960.

[8] Oshima, S., et al, "Evaporated Film Parametron," *Convention Record of ICEJ;* Aug., 1960.

[9] Goto, E., et al, "Electro-Plated Film Parametron" *PGEC of ICEJ;* May, 1960.

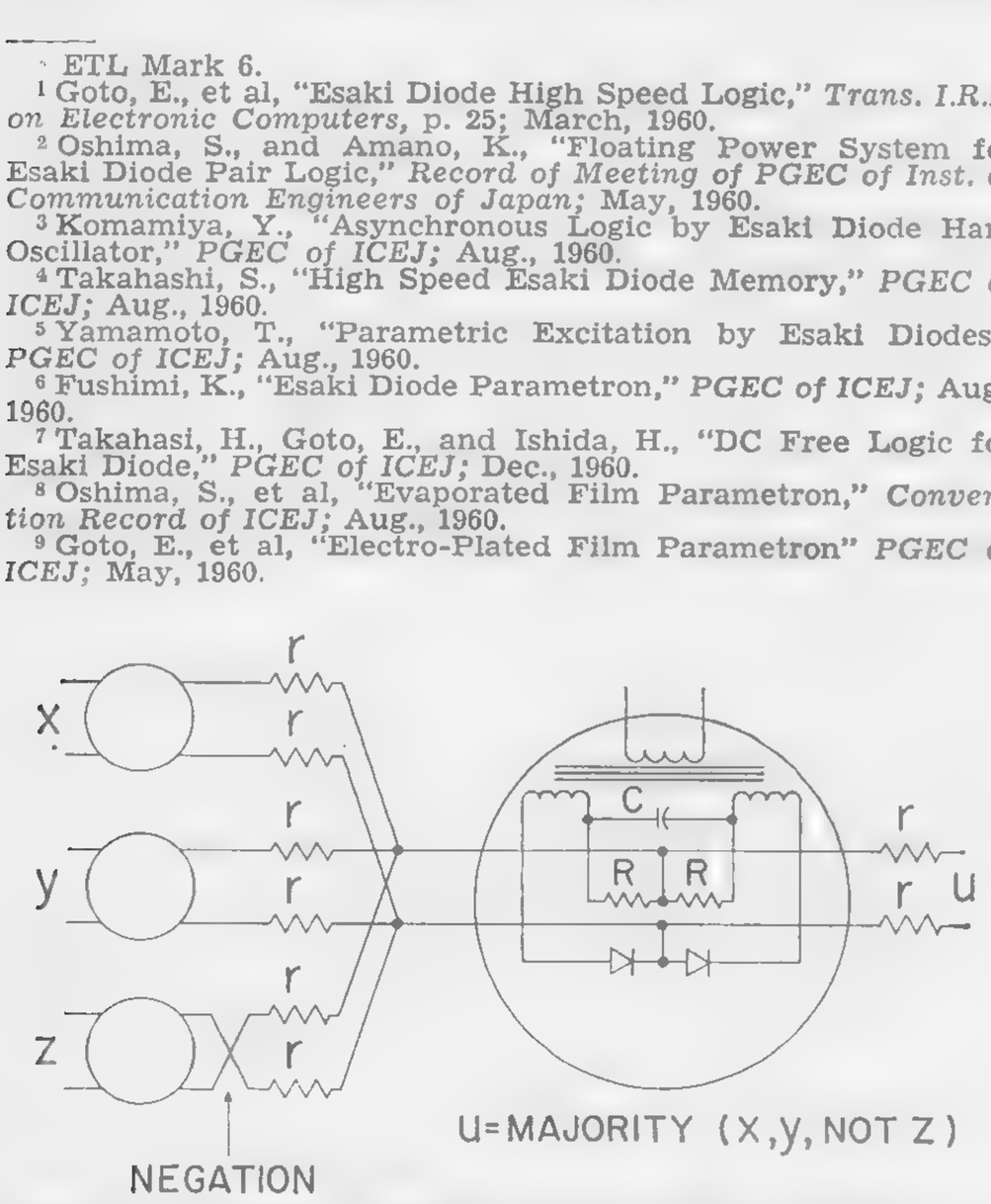



Figure 1—*Oshima's* floating power supply system for *Esaki* diode logic. A *dc* autobias is generated at the *RC* network. Left circles denote the same circuit as in the right.

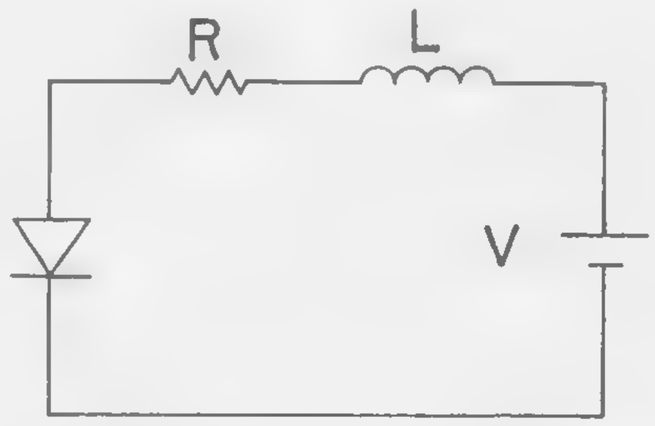



Figure 2—The simplest form of *Komamiya's* hard oscillator. Suitable values of *L, R,* and *V* give self-sustained but not self-starting oscillation.

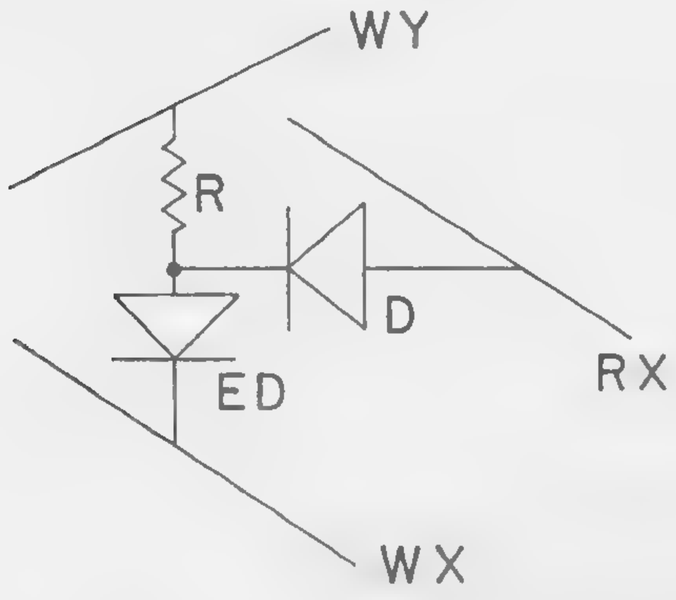



Figure 3—A memory cell of *Takahashi's Esaki*-diode matrix; *WX*, *WY* coincidence writing. Word arrangement nondestructive readout by sending a read pulse to *WY* and sensing at *RX*.

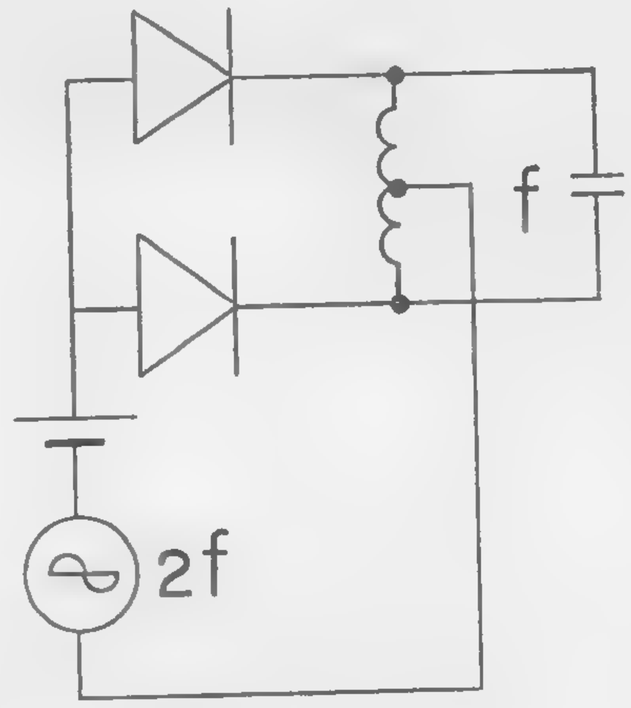



Figure 4—A ½ subharmonic oscillator of *Yamamoto* and *Fushimi*. Oscillation of frequency *f* is maintained by negative conductance and the phase is locked in by the nonlinearity of the diodes.

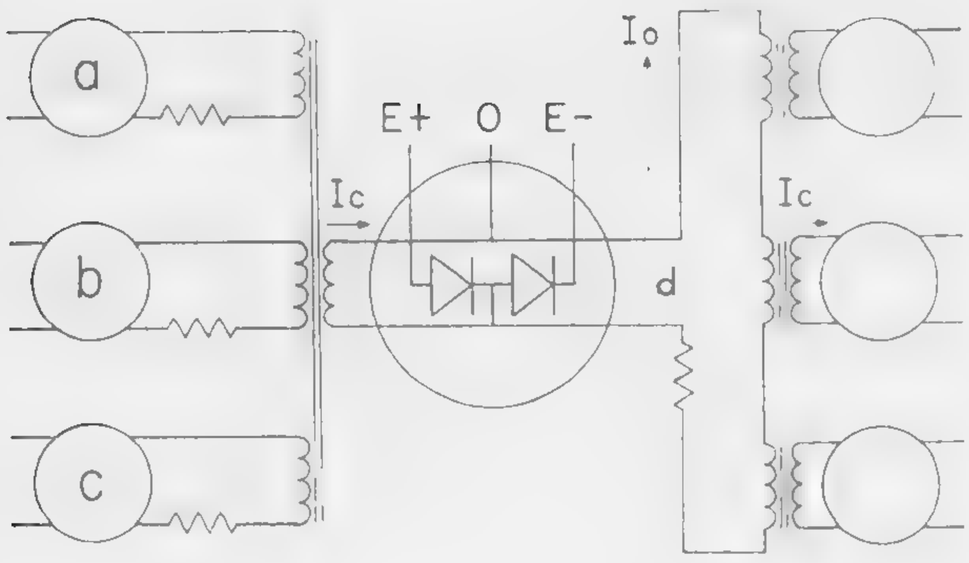



Figure 5—Transformer coupled *Esaki* diode pair logic. Circles in the left and right denote the same circuit as in the middle.

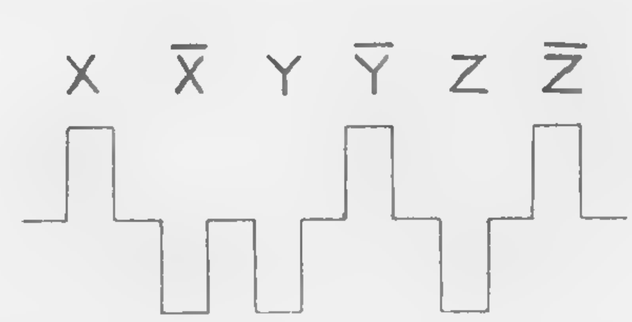



Figure 6—Waveform of signals in the *dc free logic*. Every effective digit *x*, *y*, *z*, . . . is immediately followed by its negative.

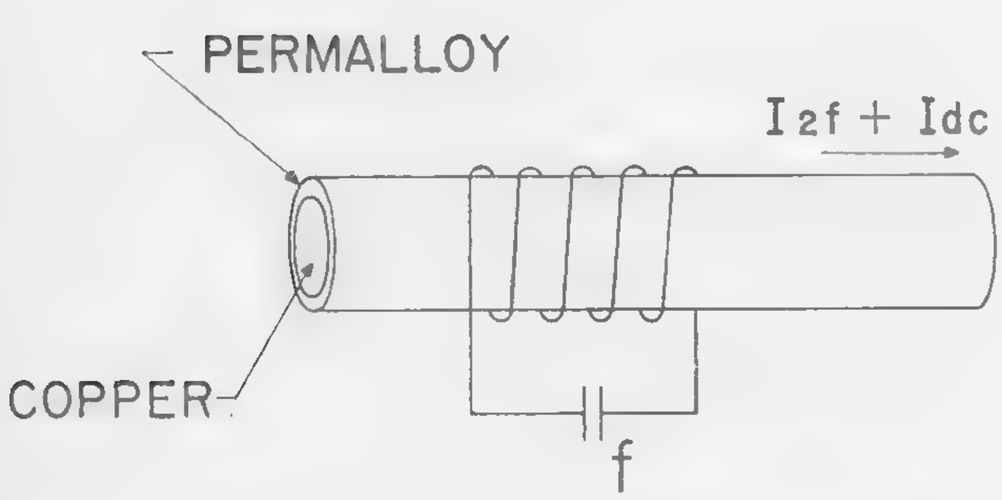



Figure 7—Magnetic thin film parametron using permalloy-plated copper wire. The pumping current is passed through the copper wire.

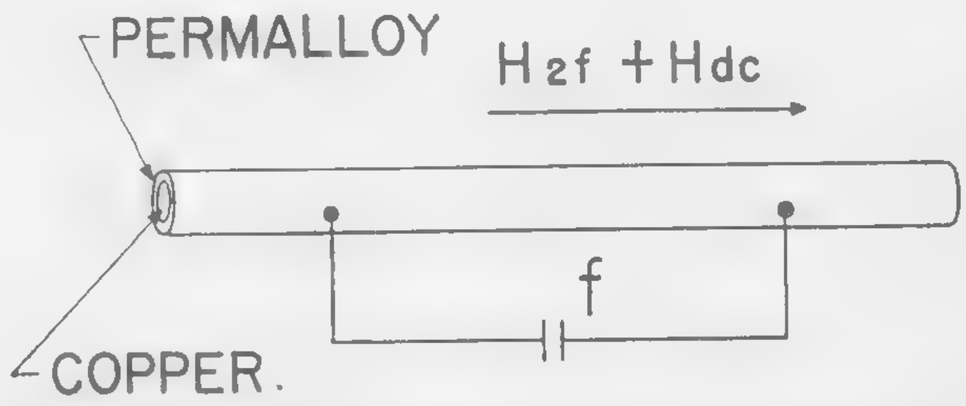



Figure 8—Magnetic thin film parametron using very fine copper wire plated with permalloy. The oscillation current passes through the wire which is placed in pumping magnetic field.

## SESSION III: Logic I

### 3.2: The Neuristor*

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Stanford Research Institute

Menlo Park, Calif.

NEURISTOR, derived from *neuron*, is a term assigned to a class of structures that exhibits attenuationless *signal* propagation, as in the attenuationless propagation of the *chemical* burning zone along a simple fuse, or the attenuationless propagation of the *ionic discharge* along the axon of a nerve fiber. Totally distributed, *one-dimensional electronic* lines, exhibiting such a propagation mode, can also be realized[1].

Attenuationless propagation represents no violation of energy conservation since, as the signal propagates, energy flows *transversely* into the line. A *line* consists essentially of a distributed, triggerable active element arranged so that when any portion of line is triggered, some or all of the locally available energy is converted into a form suitable for triggering the neighboring section of line. Thus, in a chemical fuse, if the temperature at any point passes threshold the resulting combustion generates a local temperature rise sufficient to activate the adjacent section of line. Although a fuse is a one-time device, the axon *heals* after each discharge and can be used an indefinite number of times. In conformity with the terminology of neurophysiologists, the period of healing, or recovery, is referred to as the *refractory period.*

It has been shown previously that digital computer systems of arbitrary complexity can be synthesized with networks made exclusively of lines exhibiting a *finite* refractory period[1]. To exhibit a finite refractory period, each section of line must be able to recover from its active or discharge condition. There seem to be two possibilities here. In a *rechargeable* fuse, recovery implies energy restoration after burning, the cessation of which is due to the depletion of available energy. In an axon, discharge does not cease because of energy depletion, but rather because of *inactivation* of the membrane[2]. In either case, however, that portion of line is refractive during recovery. Thus, there is a minimum spacing between pulses traveling one behind the other. Even more important, however, because of the refractory period, oppositely directed pulses are destroyed upon *collision*, since at the instant of collision the line is refractive on both sides of the collision point.

There appear to be two fundamental methods of interconnection of lines in order to form neuristor networks. In a *T*-junction, connected portions of two or more lines become simultaneously activated, or triggered, as in a knitted bundle of fuses, so that as a discharge zone (i.e., signal) arrives at the junction on any line, a corresponding signal is generated on each of the other connecting lines. In an *R*-junction, connected portions exhibit mutual refractoriness, but not mutual triggering. Thus, where two side-by-side lines are *R*-interconnected, a single pulse on either line may pass the junction without initiating a pulse on the coupled line, but two pulses (one on each line) colliding on the junction are destroyed, since again both lines are mutually refractive on both sides of the collision point, and neither pulse can pass. This provides a powerful logical inhibition function, and together with the *fan-out* capability of the *T*-junction, provides full capability for digital logic synthesis.

Although primary interest is with totally distributed electronic lines, the basic line technique and methods of interconnection are demonstrated here in terms of the simple relay lines[3] of Figures 1, 2, 3 and 4. Some examples of logic synthesis are indicated in Figures 5, 6 and 7. No distributed lines have as yet been constructed, although there seems to be little question that such lines are physically realizable.

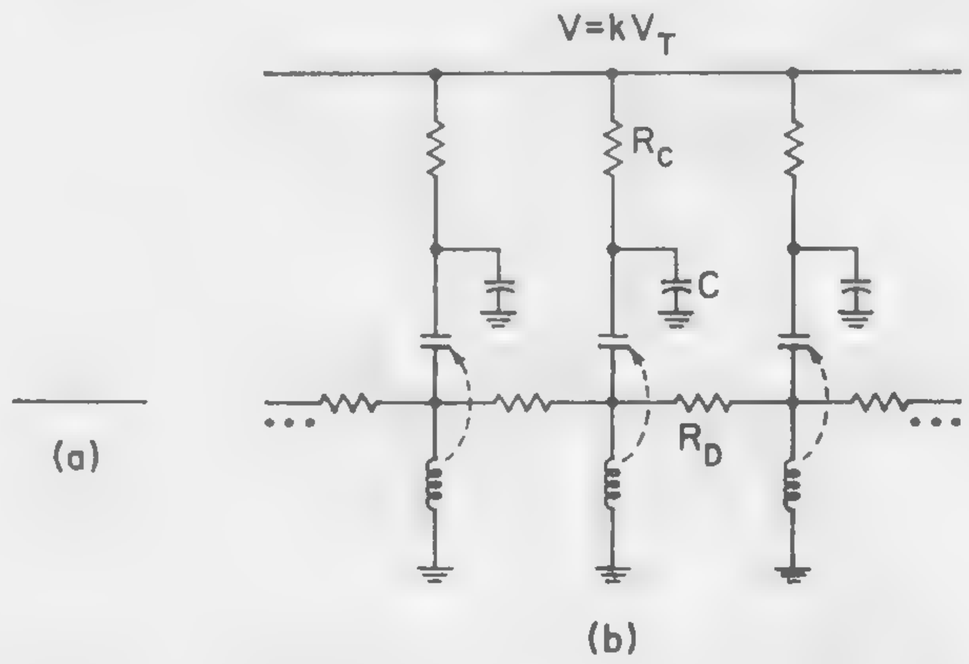



**Figure 1—*(a)* Symbol for basic neuristor line; *(b)* relay neuristor line. $V = kV_T$, where $V_T$ is relay energizing level, and $k>>1$ - - e.g., $k = 10$. Whenever a node voltage reaches level $V_T$, the corresponding relay closes, applying $kV_T$ to the node, and thereby sustaining the propagation.**

* Work on this project was supported by Contract Nonr-3212(00), Office of Naval Research, and Contract AF 33(616)-7567, Wright Air Development Division.

[1] Crane, H. D., "Neuristor Studies," *Tech. Report* 1506-2, *Solid-State Electronics Laboratory,* Stanford University; July 11, 1960.

[2] Crane, H. D., "The Axon as a Neuristor; An Analysis of Nerve Transmission," *Interim Report* 1, *Project* 3286, *Contract Nonr*-3212(00), Stanford Research Institute; November, 1960. Also issued as *Tech. Note* 1, *SRI Project* 3351, *Contract AF* 33(616)-7567.

[3] Crane, H. D., Rosengreen, A., "Experimental Results from Relay Neuristor Lines," *Interim Report* 2, *Project* 3286, *Contract Nonr*-3212(00), Stanford Research Institute; January, 1961. Also issued as *Tech. Note* 2, *SRI Project* 3351, *Contract AF* 33(616)-7567.

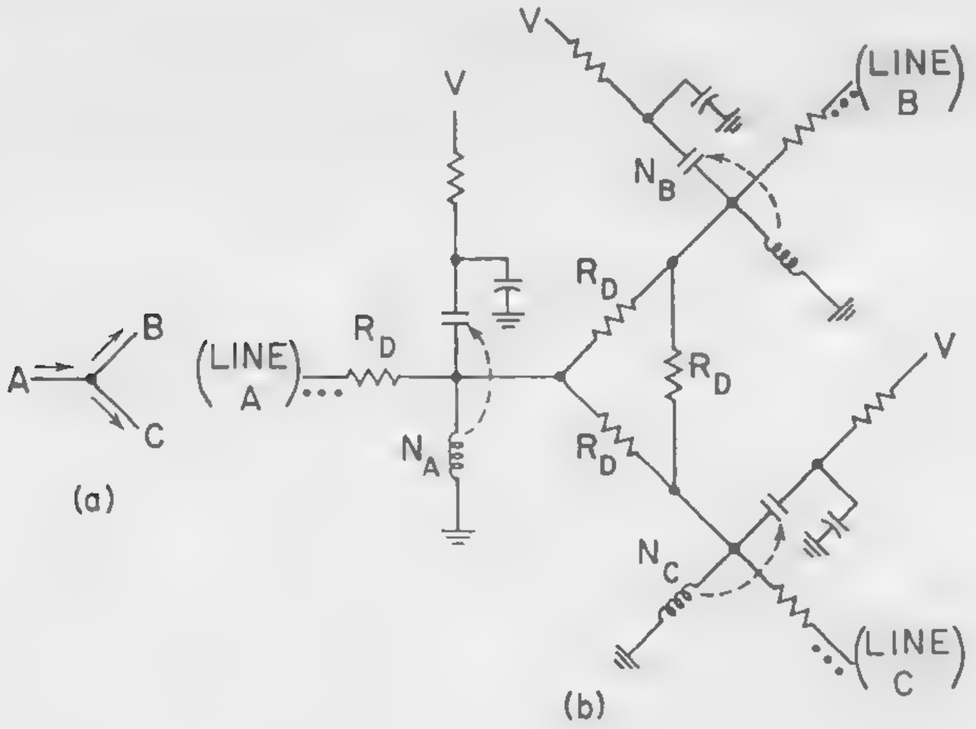



**Figure 2—*(a)*—Symbol for *T*-junction of three branches. A pulse arriving at the junction on any line results in the generation of a pulse on each other connected line. *(b)* The *T*-junction of relay lines.**

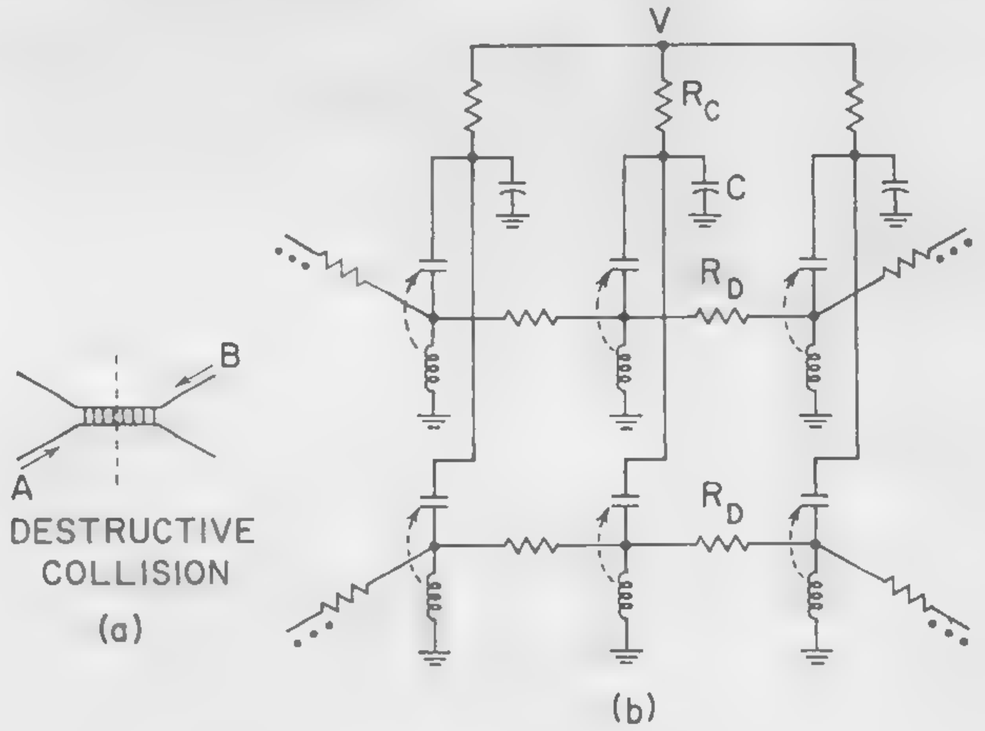



**Figure 3—*(a)* Symbol for *R*-junction. A single pulse passes the junction unimpeded (and without triggering a pulse on the other line), but two pulses colliding on the junction are both annihilated. *(b)* The *R*-junction of relay lines.**

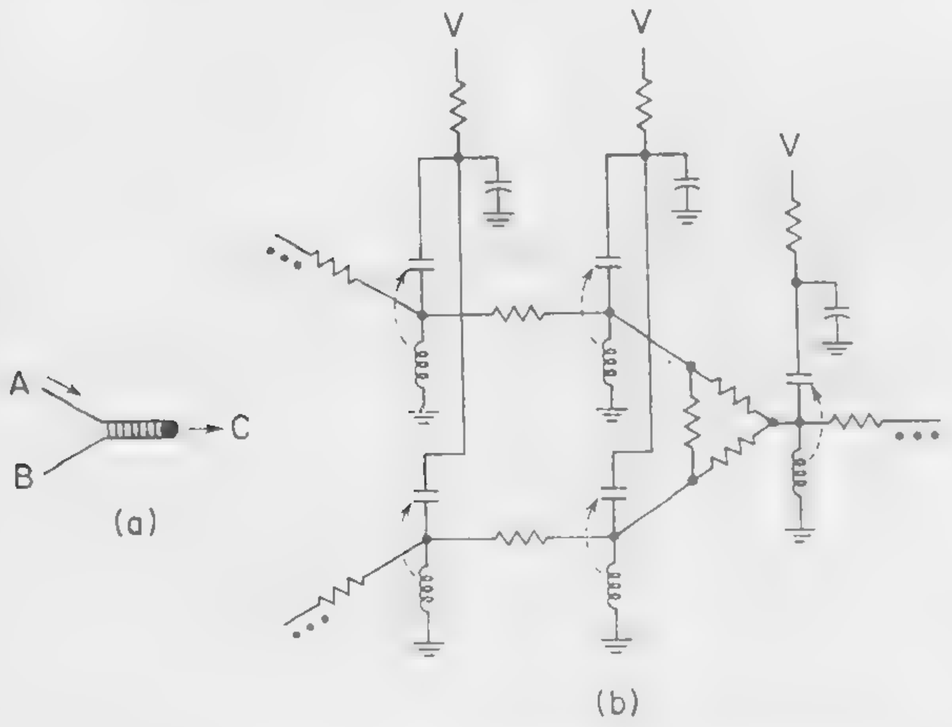



**Figure 4—*(a)* Symbol for *T-R* junction. Pulse on line *A* (or *B)* propagates along *C*, but not back along line *B* (or *A)*, since the initiating pulse cannot travel through its own refractory zone. *(b)* The *T-R* junction of relay lines.**


**Figure 5—A pulse initiated on the *storage* ring propagates indefinitely. Pulse entry via *T-R* junction. Binary state of stored variable defined as $X = 1$ for circulating pulse, and $X = 0$ for no pulse. For $X = 1$, a pulse train appears on output.**

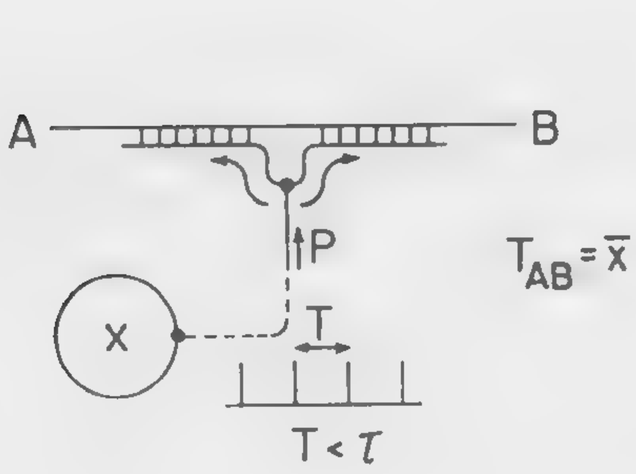



**Figure 6—Basic gating arrangement. Single pulse, *P*, inactivates line *AB* for time $\tau$, during which time any pulse from *A* (or *B)* would be annihilated. By pulse-train excitation ($T < \tau$), line *AB* is permanently inactivated for X = 1, but free for use for $X = 0$.**

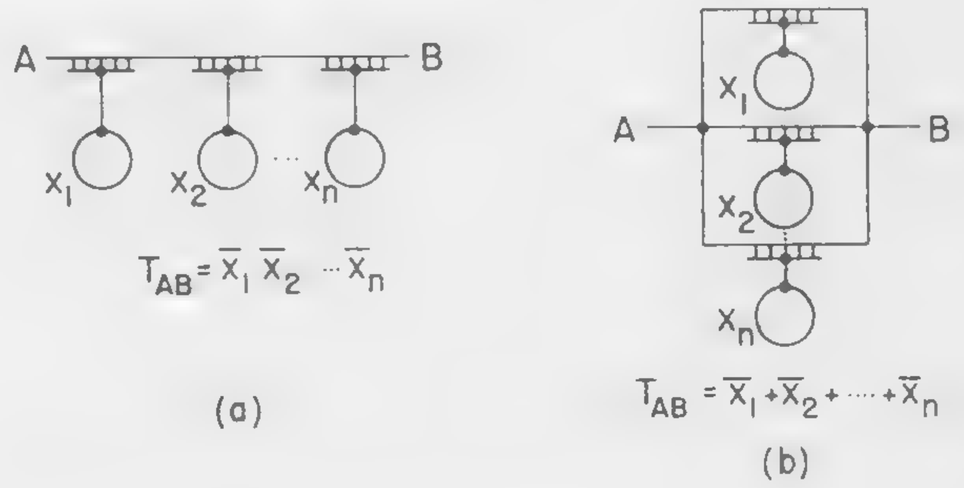



**Figure 7—Simple logic arrangements. *(a)* AND gate. Pulse from *A* (or *B)* reaches *B* (or *A)* only if $X_1 = X_2 = \ldots = X_n = 0$; *(b)* OR gate. *Single* pulse reaches *B* (or *A*) only if at least one control variable is zero.**

## SESSION III: Logic I

### 3.3: Gain and Geometrical Considerations in Planar Optoelectronic Circuits

**T. E. Bray**

Electronics Lab., General Electric Company

Syracuse, N. Y.

INTEREST IN OPTOELECTRONIC CIRCUITS is stimulated by several factors; *(a)* extreme compactness, *(b)* present capability for fabrication in large arrays, *(c)* potential low cost, *(d)* low power consumption, *(e) inherent state indication, (f)* electrical isolation available, and *(g)* capacity for large *gain* or high *fan-in* and *fan-out* in logic circuits. These factors are related to the fact that optoelectronic networks are basically composed of only two materials—*electroluminescent* to produce radiation electrically and *photoconductive* for radiation control of electrical power; no other components such as inductance, capacitance, resistance or active elements are needed. Applications of this technology are limited to those in which the relatively slow change of state with present materials (approximately .01 to 2 seconds) is not objectionable.

This paper will propose definitions for various *gains* of interest and consider the geometry of the optoelectronic elements. Consideration of many possible optoelectronic structures is eliminated by confining attention to the structures of Figure 1. Such structures are of basic interest since they allow very accurate control of both the *PC* and *EL* element properties. A photograph of typical *PC* electrode structures is shown in Figure 2.

The formulation will involve the following assumptions, each of which is normally a good approximation in the majority of present materials and circuits. The *EL* material is assumed capacitive (a loss term is included only for calculation of power gain) with negligible nonlinearity below an applied field $E_{EL\,max}$. Similarly, the *PC* material is considered purely resistive. The current is independent of *PC* thickness and showing no electrical nonlinearity below an applied field $E_{PC\,max}$ providing a power dissipation per unit area of $P_{max}$ is not exceeded. Pure sinusoidal excitation is assumed. A table of parameters is given in Figure 3.

In analyzing optoelectronic networks from a circuit viewpoint, factors such as the nonlinear voltage dependence of *EL* brightness, spectral shifts in *EL* radiative output with change in excitation frequency, the relative spectral characteristics of *EL* and *PC* and nonlinear dependence of *PC* resistivity on brightness cause difficulty. However, if one is able to find a relation between *EL* excitation voltage and *PC* resistivity, the foregoing factors do not appear explicitly. This relation, termed by the author *transluminance* (by analogy with *transconductance*), may be written

$$\rho\,\square = f\,(V_{EL}, \omega) \qquad (1)$$

where a sinusoidal *EL* exciting voltage of frequency $\omega$ and rms value $V_{EL}$ is assumed. A simple, but quite accurate empirical expression for *transluminance* is shown in Figure 4, together with experimental data.

The circuit of Figure 5 is used in defining voltage and current gain. These may be written:

Steady state voltage gain $G_V = V_2/V_1$
Incremental voltage gain $G\Delta_V = \Delta V_2/\Delta V_1$
Steady state current gain $G_I = I_2/I_1$
Incremental current gain $G\Delta_I = \Delta I_2/\Delta I_1$

For applications where a signal is to be amplified, the $\Delta$ gain would probably be useful. In switching circuits either definition may be useful, depending upon whether memory is involved (where steady state gain is important) or whether relative signal level only is important. The voltage gains, on a unit area basis, are given by Equations (1) and (2) of Figure 6. Current gains, as defined here, are given by Equations (3) and (4).

Small signal power gain may be calculated by assuming the input *EL* element impedance contains a real part and that the load can dissipate energy and is matched to the controlling *PC* resistance. The equivalent circuit is shown in Figure 7, together with an equation for optimum matched power gain using the transluminance of Figure 4.

To fabricate optoelectronic circuits which show maximum utilization of volume, the interdigital *PC* electrode structure must be examined. From a general viewpoint, considering the limitation of electric field ($E_{PC\,max}$) it is desirable to utilize the rectangular structure shown in Figure 8*A*. If one minimizes the area occupied by such a structure, given the electrode width and gap dimensions as well as *folding ratio*, it is found that the relation between the number of *half-cycles* of *PC* electrode ($Nf$) is related to the folding ratio, $N_O$, by the equation of Figure 8*B*.

The foregoing relations, useful in themselves, may be combined to yield gain-geometric tradeoff ratios which are of use as general criteria in the design of optoelectronic circuitry.

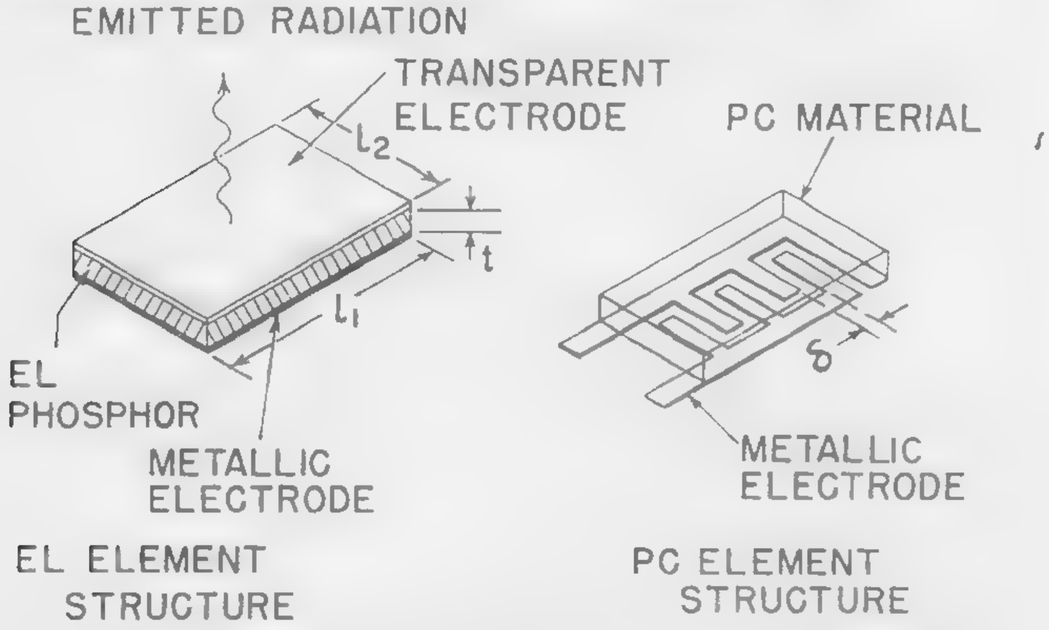



**Figure 1—Optoelectronic structures used in analysis, PC elements considered have coplanar (and normally interdigital) electrodes with a thin *PC* layer overlay. Electrode gap is $\delta$.**

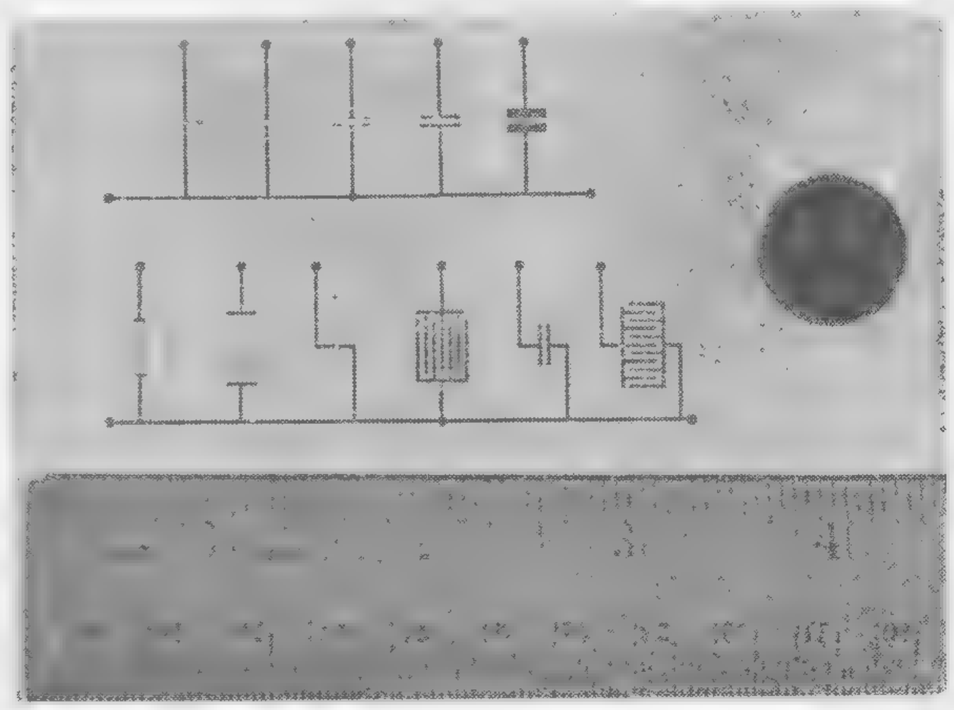


**Figure 2—Photograph of *PC* electrode structure. The substrate is 10 mil glass. The interdigital electrodes each have the same *folding ratio*.**

$\mathcal{E}_{EL\,MAX}$ – THE MAXIMUM ALLOWED VALUE OF THE AVERAGE ELECTRIC FIELD WITHIN THE EL PHOSPHOR

$\mathcal{E}_{PC\,MAX}$ – THE MAXIMUM ALLOWED VALUE OF THE AVERAGE ELECTRIC FIELD IN THE PC

$P_{MAX}$ – THE MAXIMUM ALLOWABLE POWER DISSIPATION PER UNIT AREA IN THE PC

$C_A$ – CAPACITANCE OF EL MATERIAL PER UNIT AREA

$\rho_\square$ – RESISTIVITY OF PC MATERIAL PER SQUARE

**Figure 3—Material parameters and definitions.**

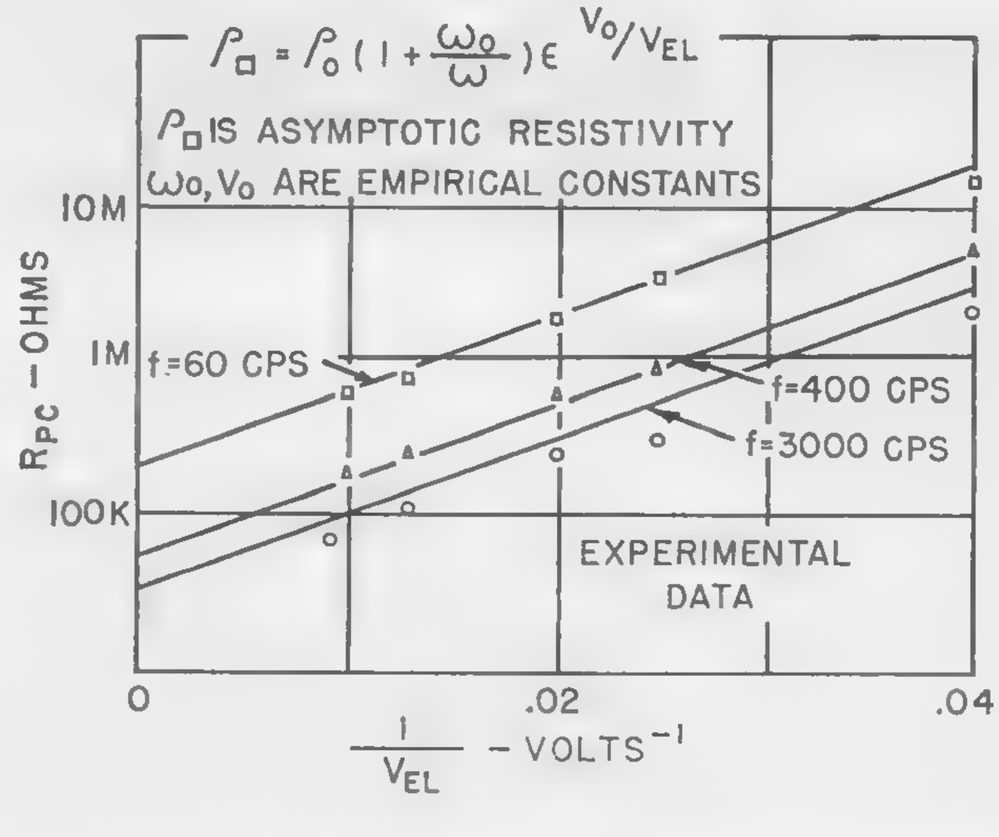



**Figure 4—An empirical transluminance relation and fitting of relation to experimental data.**

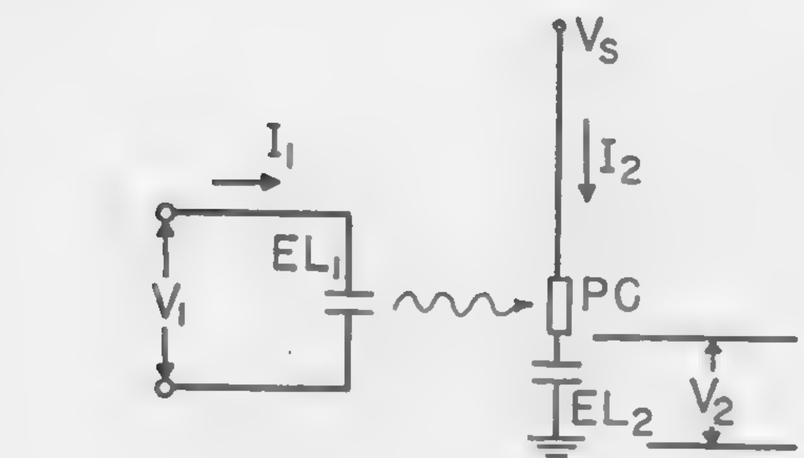



**Figure 5—Proposed circuit for use in defining voltage and current gains. The overall gain of a series of interconnected circuits of this type may be obtained forming the product of the individual gains.**

STEADY STATE VOLTAGE GAIN:

(1) $G_V = \dfrac{\mathcal{E}_{PC\,MAX}}{V_1 \left\{ \delta^2 + \left[ \dfrac{\omega\, C_A \rho_\square}{(1+K)\,\delta} \right]^2 \right\}^{1/2}}$

K = RATIO OF PC ELECTRODE WIDTH TO GAP

$\delta$ = pc GAP

INCREMENTAL VOLTAGE GAIN:

(2) $G_{\Delta V} = \dfrac{\Delta V_2}{\Delta V_1} \longrightarrow \dfrac{\partial G_V}{\partial G_{V_1}}$

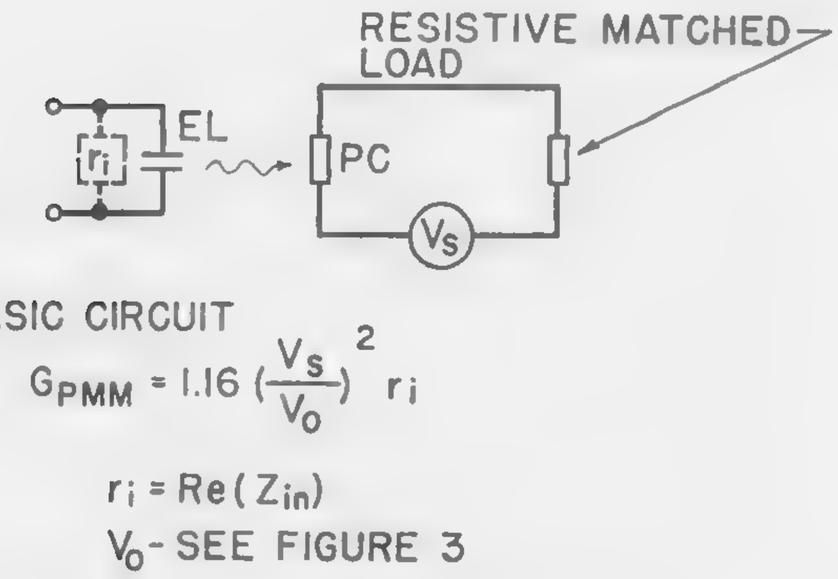
STEADY STATE CURRENT GAIN:

(3) $G_I = Q\,G_V \qquad Q = \dfrac{\text{AREA } EL_2}{\text{AREA } EL_1}$

INCREMENTAL CURRENT GAIN:

(4) $G_{\Delta I} = \dfrac{\Delta I_2}{\Delta I_1} \longrightarrow = Q G_{\Delta V}$

**Figure 6—Voltage and current gain equations normalized to a unit area. Voltage gain is maximized with respect to *PC field*.**




A. BASIC CIRCUIT

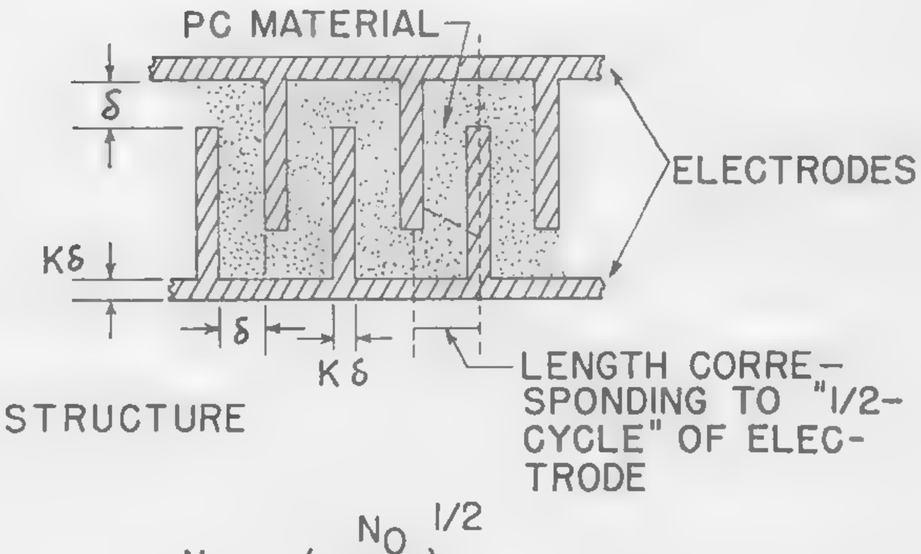
$G_{PMM} = 1.16 \left(\dfrac{V_S}{V_0}\right)^2 r_i$

$r_i = Re(Z_{in})$

$V_0$ – SEE FIGURE 3

B. MAXIMUM MATCHED POWER GAIN

**Figure 7—Small signal optoelectronic power gain. The maximum matched power gain is found by matching the load with *PC* resistance for maximum power transfer, then setting the input and supply voltages optimum values with respect to material parameters.**




A. STRUCTURE

$N_f = \left(\dfrac{N_0}{1+K}\right)^{1/2}$

K$\delta$ = ELECTRODE WIDTH  $\delta$ = ELECTRODE GAP

B. OPTIMUM RELATION

**Figure 8—PC electrode structure and optimization. The optimization is performed with respect to area, assuming $K$, $\delta$ and $N_0$ are fixed by the material properties and circuit requirements. Optimum is relatively broad.**

## SESSION III: Logic I

### 3.4: An EL-PC Device to Implement Flow-Table Logic for Variable Pattern Recognition

**P. R. Low*, J. A. O'Connell‡ and E. J. Skiko**

IBM Corporation

Poughkeepsie, N. Y.

A SEQUENTIAL CIRCUIT IS ONE in which the present output is a function not only of the present inputs, but also the past history of these inputs. *D. A. Huffman*[1] has suggested that a chart, called a flow table, be used to record the sequence of these past input conditions and to define the operation of the desired circuitry. A set of standard manipulations involving this chart has been developed as a means of deriving the proper Boolean expressions. A method which bypasses all these manipulations has been suggested by *P. R. Low* and *G. A. Maley*[2].

This method, termed *flow table logic*, provides a technique for implementing the desired circuitry in a physical configuration directly analogous to the logical flow table configuration (Figure 2), rather than in the standard *AND-OR* form. The advantages of this technique lie in the fact that the circuitry is amenable to batch fabrication, thus emphasizing simplicity and regularity, providing ease of circuit design and attaining an increase in circuit speed.

A pattern is defined as a group of $N$ sequentially scanned $M$-bit words. In this sense pattern recognition is a sequential problem. The concept of flow table logic is directly applicable to the solution of this problem. However, rather than permanently wiring the circuit to recognize only a single pattern, it was desired to provide the facility to change the pattern to be recognized at any time in a simple manner. This required that several changes be made in the standard flow table and that additional circuitry be included.

The pattern recognizer consists of three superimposed optoelectronic matrices, electrically independent but optically coupled:

*(a)* An $N$ $(2^m\text{-}1)$ *EL x-y* panel, any area of which can trigger a geometrically corresponding

*(b)* *EL-PC* storage element in an $N$ $(2^m\text{-}1)$ memory panel, which in turn can selectively gate

*(c)* A $2N \times 2^m$ *EL-PC* flow table matrix.

*Teaching* a unique pattern is a prerequisite to subsequent recognition. *Teaching* is accomplished by serial selection of the appropriate elements in the *x-y* panel, thus transferring the pattern to static storage in the memory panel. The latched areas in the memory panel illuminate corresponding, paired photoconductor gates in the flow table matrix, thus wiring the flow table uniquely.

Each column of the flow table is associated with a different one of the $2^m$ words which could be included in the pattern. Recognition is accomplished by selecting sequentially the columns appropriate to the pattern under consideration. An optical bit will proceed through the flow table. A complete traversal of the flow table can be made only if the columns corresponding to the photoselected gates are selected in proper sequence. Any deviation from the proper sequence causes extinction of the optical bit and signals *non-rcognition.*

Aside from common substrate and structural materials, the entire pattern recognizer is constructed from *EL* and *PC* elements.

The *x-y panel* (Figure 3) performs an input function in the pattern recognizer. It consists of a 4 x 7 array of *EL* areas designed for coincident voltage selection and total suppression of crosstalk through the medium of non-linear resistive *SiC* elements. A schematic showing steps in the fabrication of the *x-y* panel as well as its geometric properties is given in Figure 5. The characteristics of the basic panel have been described elsewhere [3].

The memory panel (Figure 3) provides for static optical storage and selective optical gating of the flow table panel. It consists of a 4 x 7 array of *EL-PC* bistable elements, capable of triggering from the *x-y panel.* The construction details for the memory panel are shown in Figure 6. Photographs of the fully assembled device are shown in Figure 4.

The flow table performs the active logical operations in the pattern recognizer. As seen from a comparison of the schematic (Figure 2) and Figure 7 which shows the structural details, the flow table consists of a basic 8 x 8 *EL-PC* logic array with an interposed 4 x 7 array of *PC* gates in registry with and illuminated by the memory array.

Typically the three panels are operated at 300-350 *v (rms) at* 1000 *cps.* Pattern storage is accomplished by manual switching, or by use of neon-*PC* or relay selection circuits. The *x-y* brightness is about 2-foot-lamberts. Memory triggering sensitivity is 0.020 foot-candle seconds. The memory panel is erased by voltage interruption. The memory brightness is approximateiy 10-20 foot-lamberts.

Pattern recognition in the flow table is accomplished by manual or electrical switching. Neon-*PC* and transistor-driven relay rings have been used. The drive rings can be made to operate continuously or to deliver a single shot to the flow table causing merely a single procession of the optical bit down the panel. The flow table is not grounded and both sides of any selected line are switched simultaneously with slight pulse overlap.

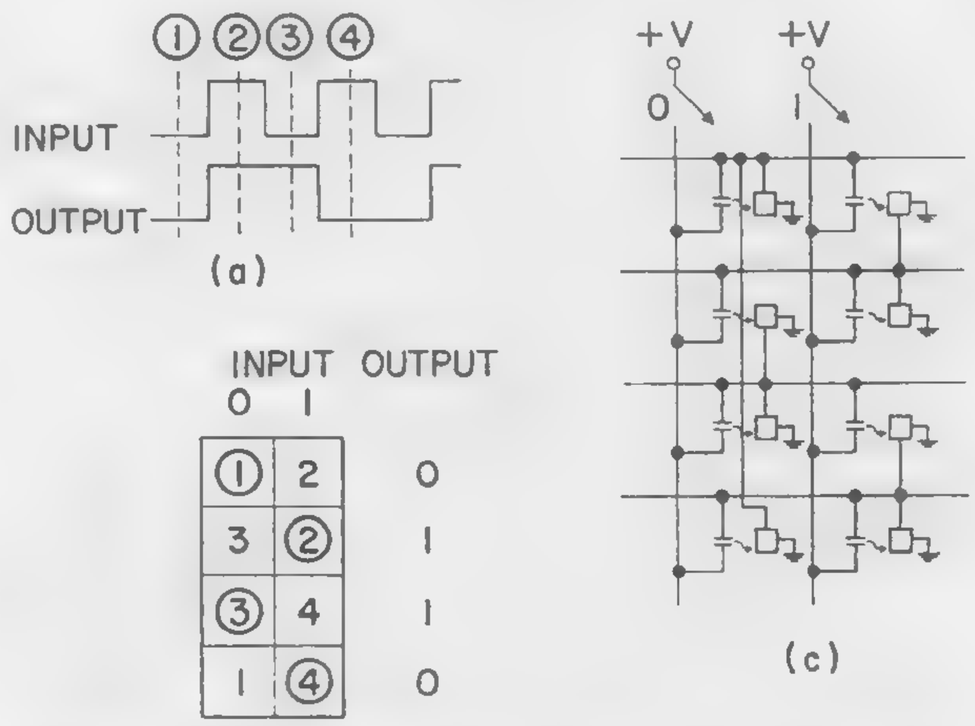



**Figure 1—Example timing chart *(a)*, logical flow table *(b)*, and *EL-PC* flow table *(c).***

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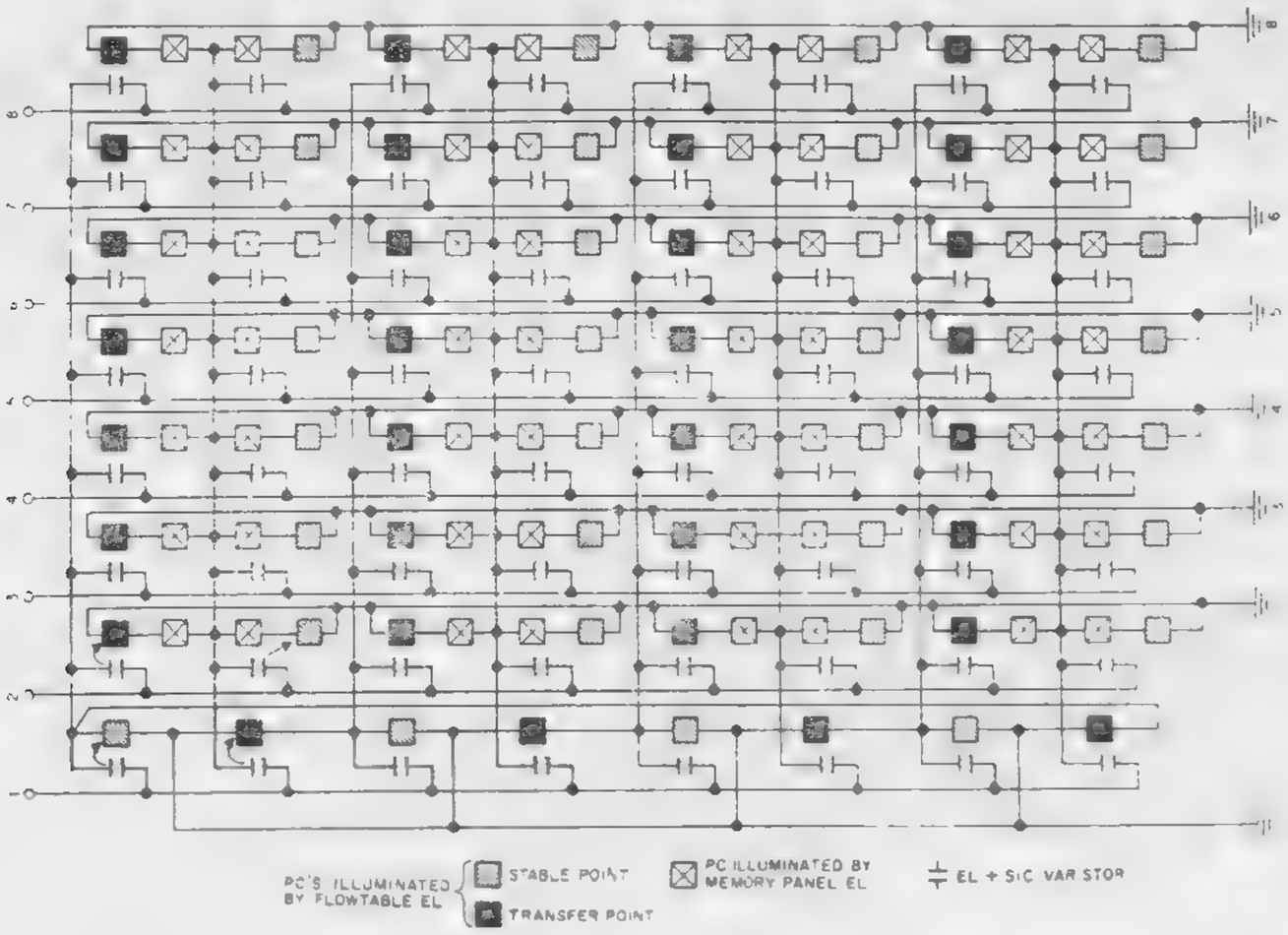
* Now at Stanford University

‡ Now at General Telephone Research Laboratories, Bayside, N. Y.

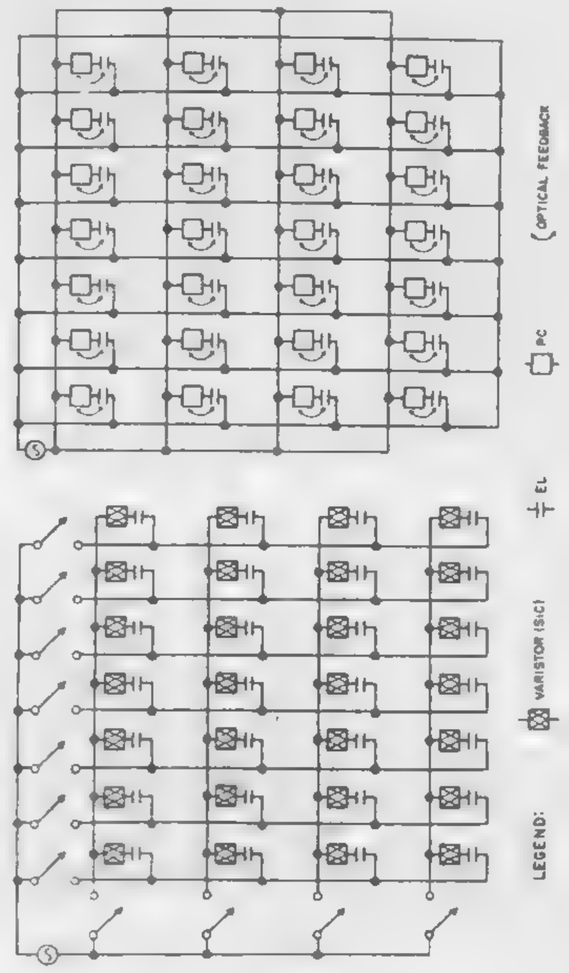
[1] Huffman, D. A., "The Synthesis of Sequential Switching Circuits," (Doctoral Dissertation, Massachusetts Institute of Technology, 1953; *Journal of the Franklin Institute;* March and April, 1954.

[2] Low, P. R., and Maley, G. A., "Flow Table Logic," *Proceedings IRE,* published; January, 1961.

[3] O'Connell, J. A., and Narken, B., "Increasing the Brightness-Voltage Non-linearity of Electroluminescent Devices," *IBM Journal, Research and Development;* October, 1960.




*(Above)*
**Figure 2—Schematic diagram of *EL-PC* flow table panel.**




*(Right)*
**Figure 3—Schematic diagrams of *EL x-y* panel (bottom) and *EL-PC* memory panel (top).**

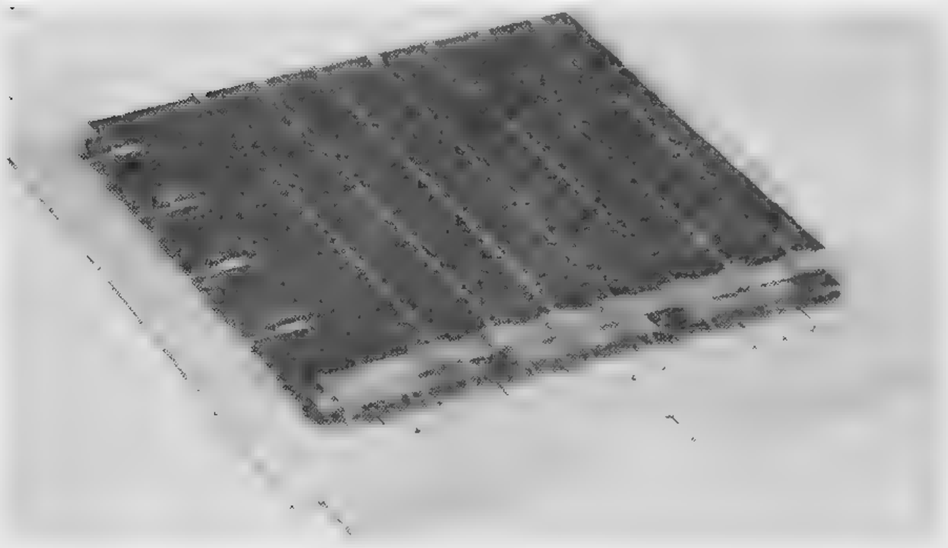


**Figure 4—Assembled pattern recognition device.**

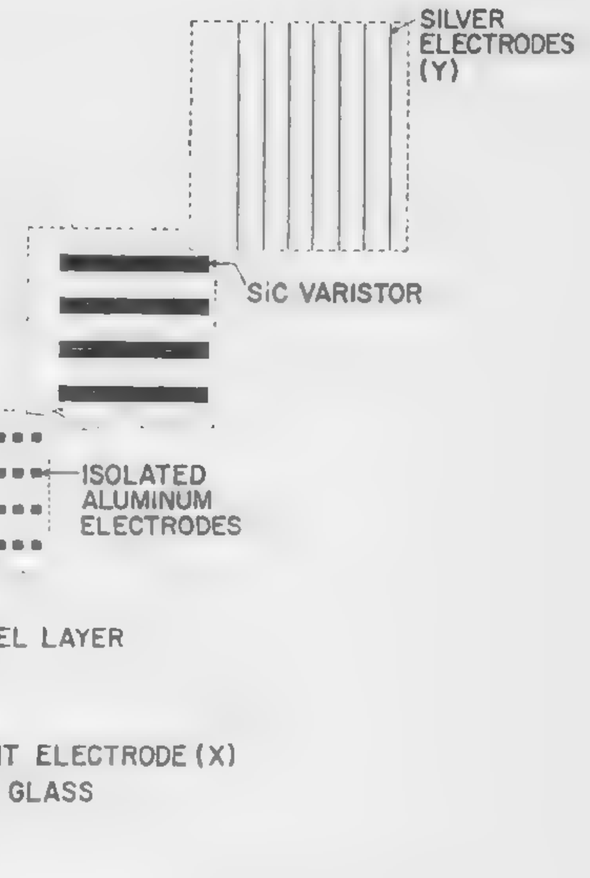



**Figure 5—Steps in construction of *EL x-y* panel.**

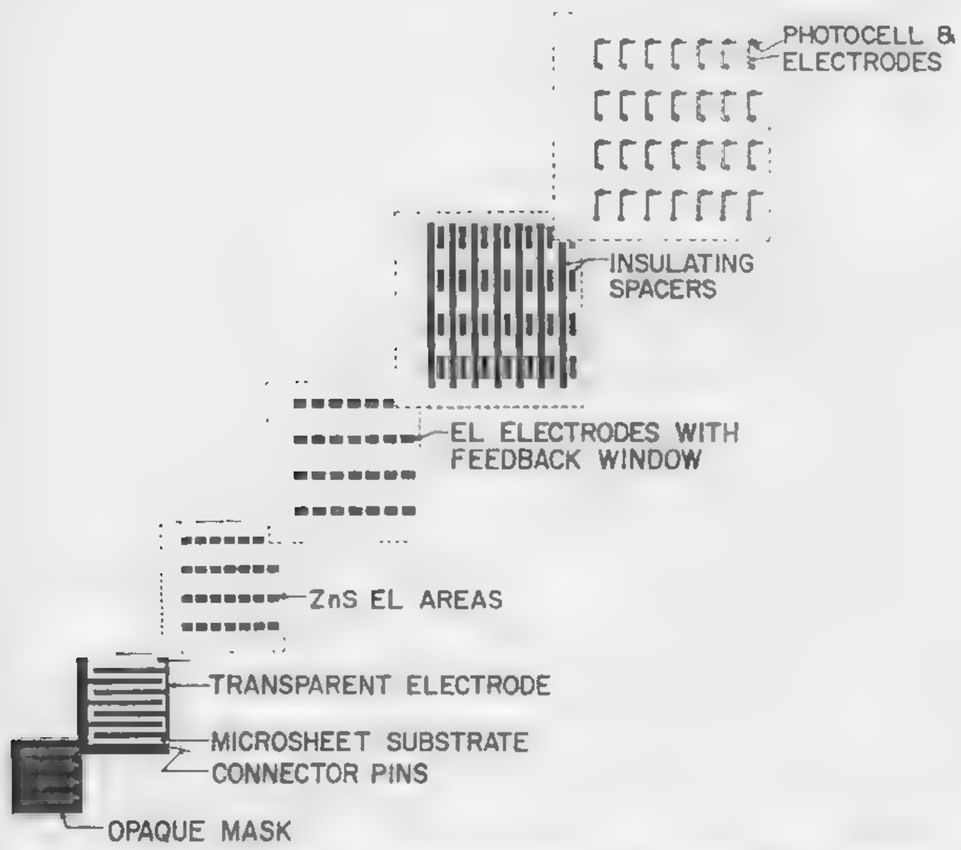



**Figure 6—Steps in construction of *EL-PC* memory panel.**

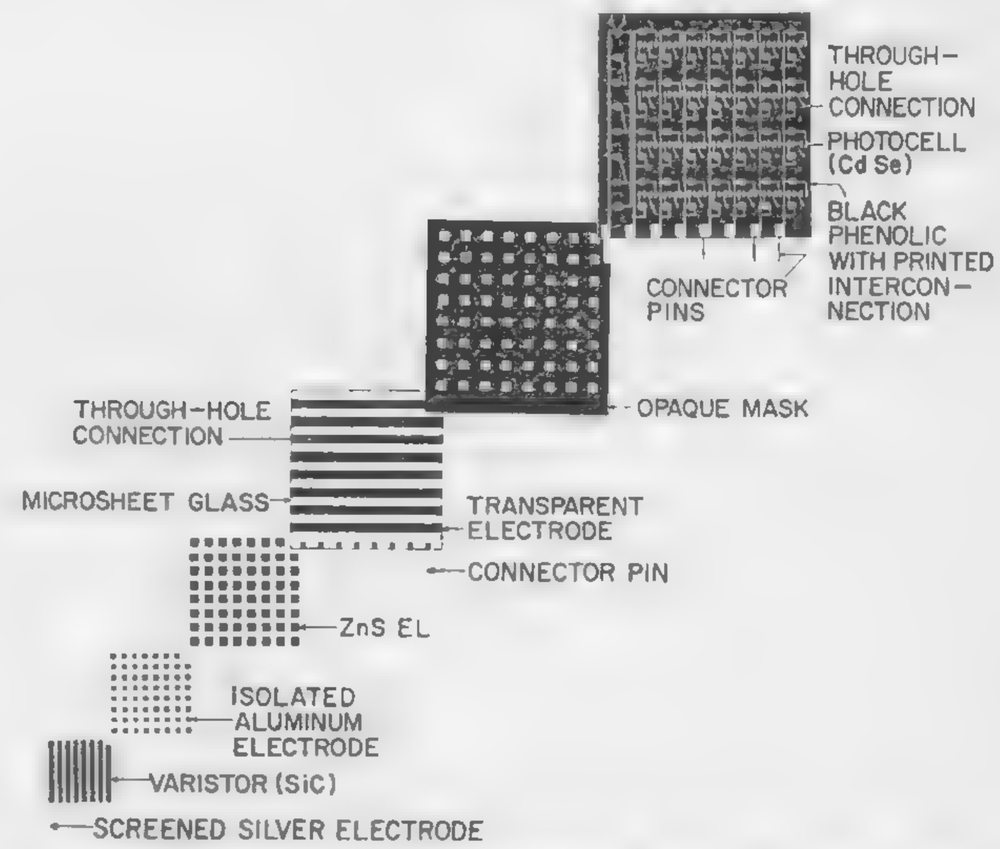



**Figure 7—Steps in construction of *EL-PC* flow table panel.**

## SESSION III: Logic I

### 3.5: Properties of Hydraulic Circuits Using Valves

H. H. Glaettli

IBM Corporation

Zurich, Switzerland

ACCORDING TO THE VOLTAGE MODE in electric circuits, information in hydraulic circuits may be represented by pressure, for instance *ONE* by high pressure, *ZERO* by low pressure.

A simple valve serving as a logic element is shown in Figure 1. Depending upon whether the pressure at the input terminal $Q$ is lower or higher than $m$ (medium pressure), the spool touches the lower or upper stop. Acting as a three-input/one-output device, it connects $X$ with $R$ or $S$. A minor pressure difference at $Q$ may result in a larger change at $X$ (amplification). A signal at $R$ or $S$ degenerates only slightly, due to leakage and flow restrictions.

Due to the fact that no other elements but valves, channels and possibly condensers (pressure *vessels*) appear, the circuits look very simple. Figure 2 shows a circuit that generates the *carry*-signal in a three-input binary adder.

$U$ is advantageously chosen as the *carry*-signal coming from the previous stage, because $V$ or $W$ may change the position of the corresponding spool and would, therefore, lengthen the *carry* propagation time.

The response time is mostly determined by inertia. Its dependence on the size is influenced by the geometry of the places where viscous losses may concentrate. This frequently occurs in the gap between piston and bore. Typical curves for the case where this gap is a constant fraction of the bore diameter are given in Figure 3.

The viscosity $\eta$ acts as a parameter: High viscosities do not allow a decrease of the response time by miniaturization. A finite $\tau$-value is found for vanishing size, but finite viscosity.

Branching also affects the response: The resulting increase depends upon fluid density, viscosity, branching ratio and geometry. Figure 4 represents a simplified case.

The parabola $p$ is a good approximation for small $n$-values, whereas the line $s$ is approached asymptotically for higher $n$. Higher viscosity increases the slope of $s$, but has no effect on $p$.

As far as no cavitation effects are taken into consideration, hydraulic circuits compare with electronic or solid-state counterparts as follows: The valves as active elements are highly nonlinear, and the lines are characterized by a high ratio self inductance (inertia)/capacity (compressibility).

The role of inertia is, therefore, predominant. A three-dimensional design is necessary to keep the signal transfer as well as the power distribution lines as short as possible. As far as molding technique is to be applied, a technique resembling printed circuits may be applied. Figure 5 shows how a binary counter circuit was adapted to this technique.

Each layer contains a complete counterstage. The power distribution lines project vertically through the layers, of which as many as desired may be packed together. Figure 6 shows a 10-stage model worked in a translucent aethoxylin resin.

The maximum counting frequency depends on the number of stages in a similar manner as shown in Figure 4. This is due to a *branching effect* occurring in the power distribution system.

Other manifestations of this effect occur in adders and shift registers. The *carry*-propagation time in adders, for example, again follows the above-cited law, although circuits may be used according to Figure 2, where the *carry*-signal does no work in the adder itself. The work done in circuits or indicators connected to the adder has the same effect: A finite amount of fluid may be displaced in each stage. In shift registers there is a marked dependence of the maximum allowable shift frequency on the information pattern contained; $n$ then has to be taken as the number of changes occurring per shift pulse.

These peculiarities, including cavitation effects, are far from rendering valve logic impractical; the fact that system planning cannot occur analogously with electronic models is, to a great extent, the consequence of these circumstances.

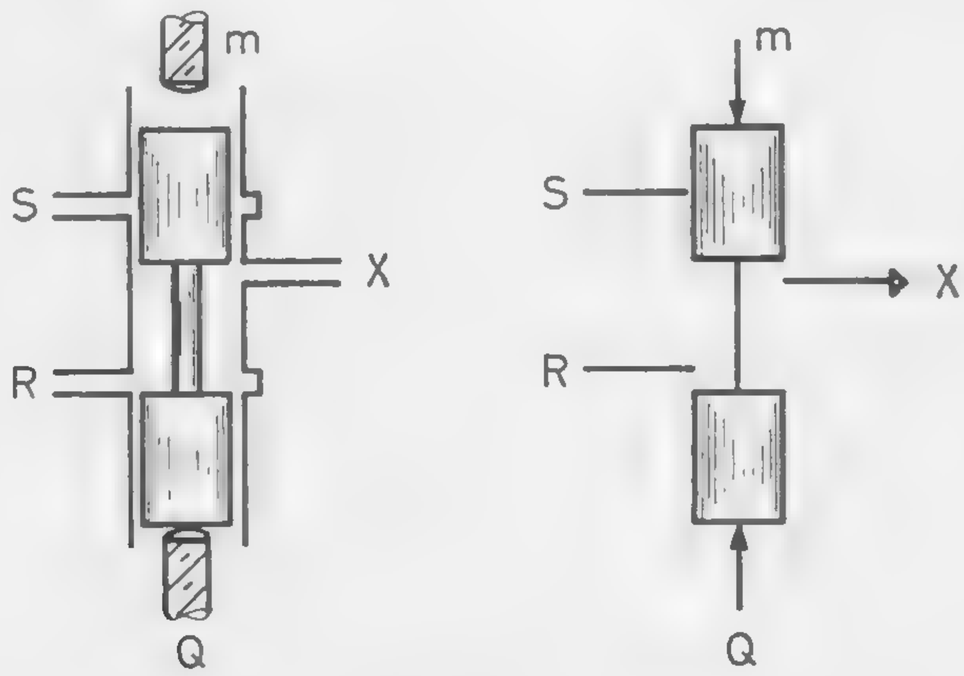



**Figure 1—Basic valve element.**

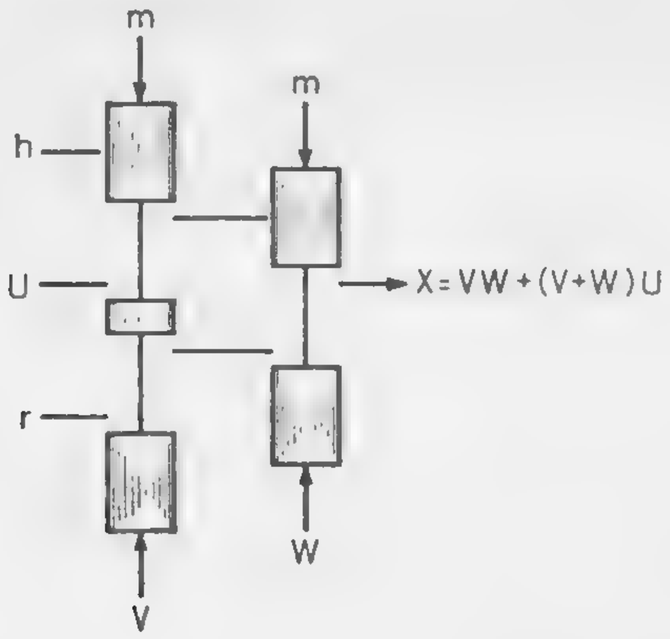



**Figure 2—*Carry* generation in a binary full adder.**

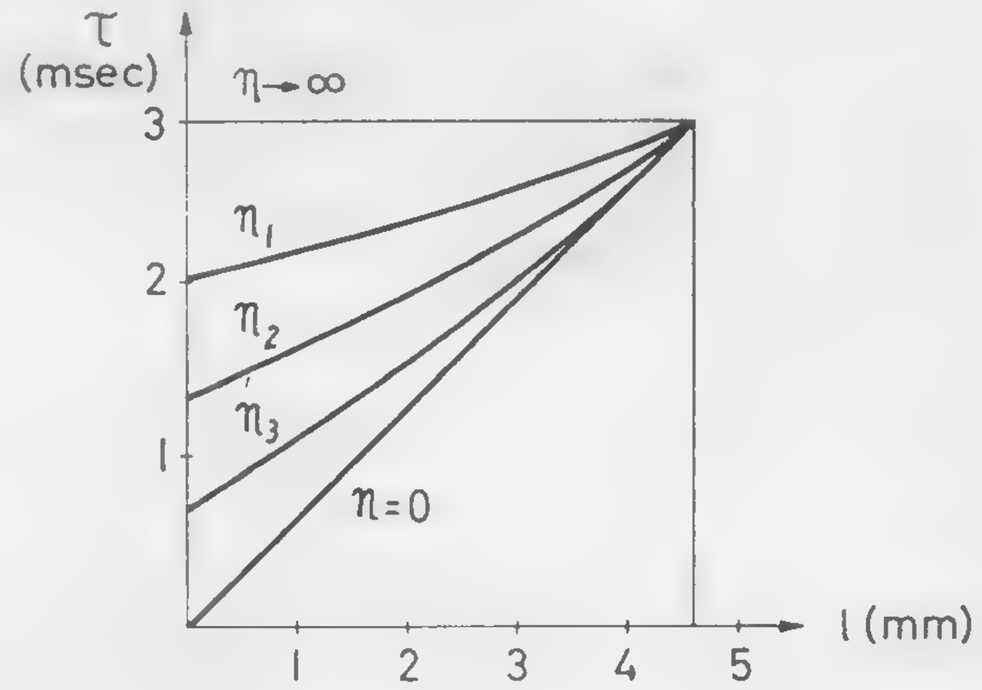



**Figure 3—Response time of a specific arrangement as a function of its linear size.**

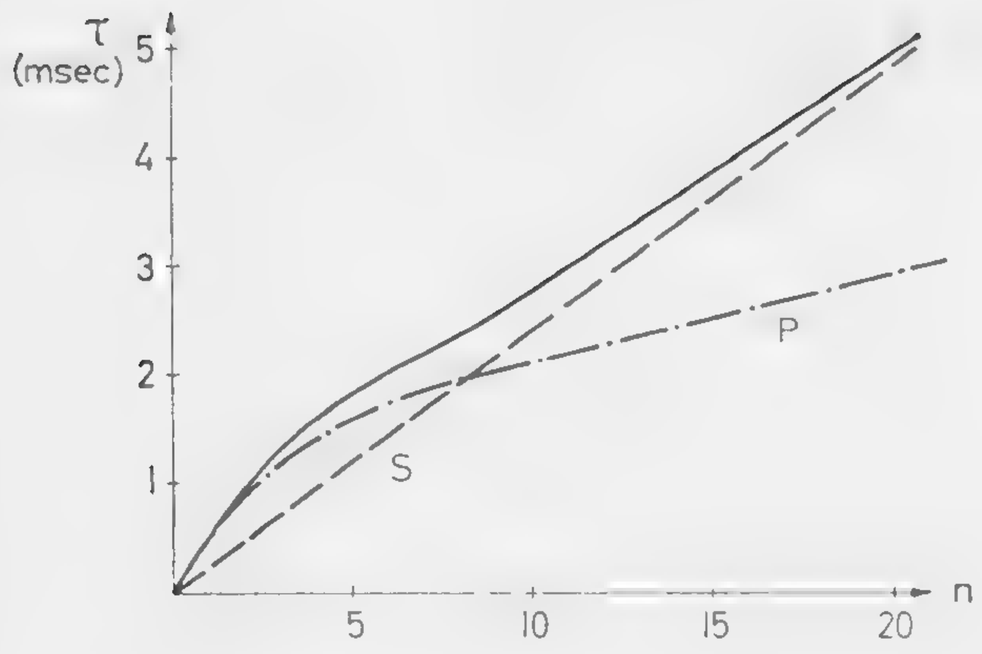



**Figure 4—Increase of response time by branching.**

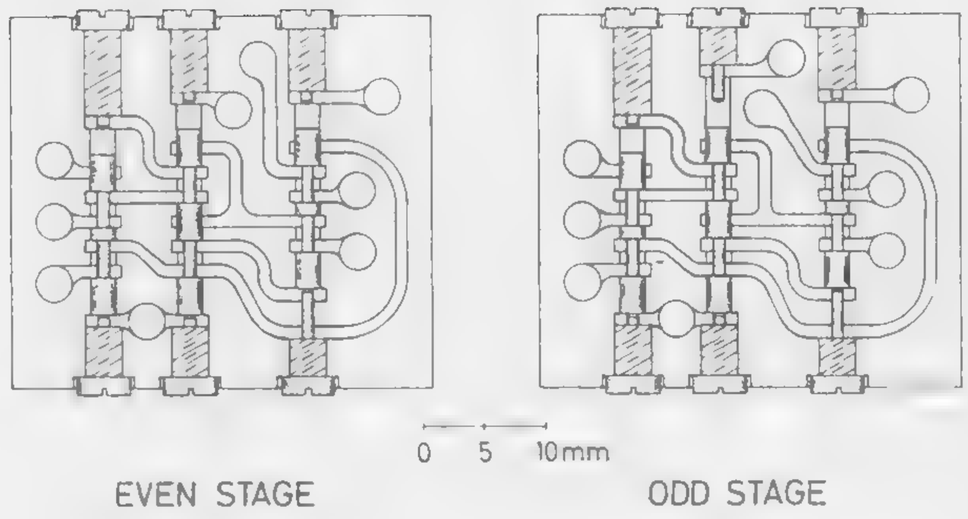



**Figure 5—Adaptation of a binary counter circuit to the *molded circuit* technique.**

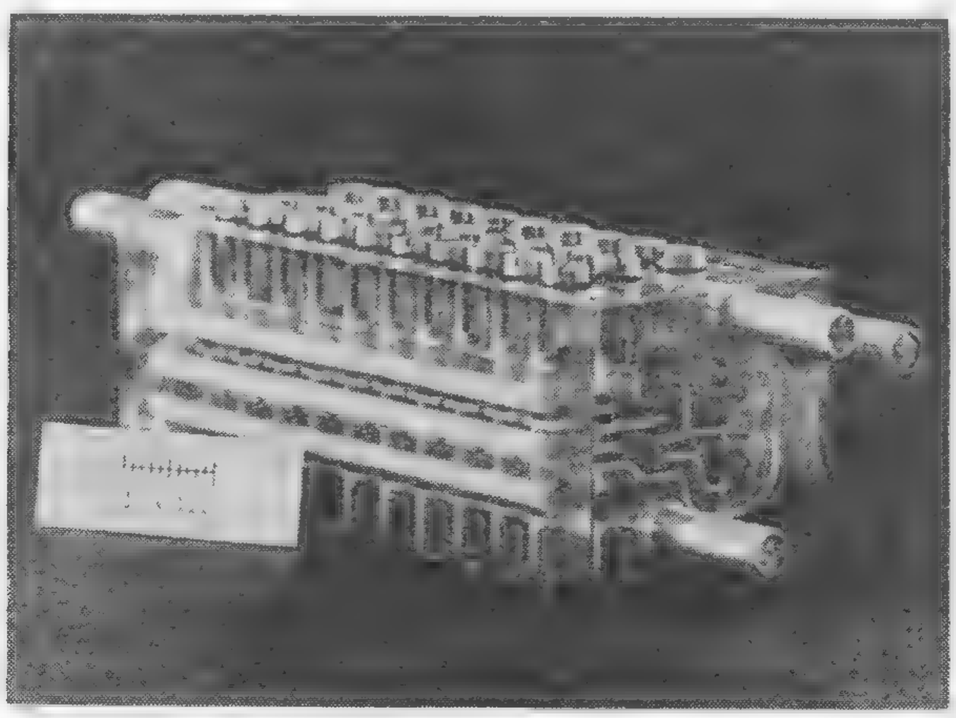


**Figure 6—A 10-stage hydraulic binary counter.**

## Informal Discussion Session

### E.4/1: Wide Tolerance Logic Circuits Using Tunnel Diodes in the Voltage Mode and Rectifier Diode Coupling*

G. B. B. Chaplin and P. M. Thompson

Plessey Company, Ltd.

Hants, England

Logic that depends on the analog addition of inputs has two inherent disadvantages. It requires close tolerance components and tends to be relatively slow. Tunnel diode-resistor logic has both these drawbacks and also requires extra complication to make it unilateral.

This paper will describe a logic system designed to overcome these difficulties; tunnel diodes are used in the voltage mode and information is transferred by recifier diodes. In this system there are two types of basic *A* and *B* circuits, as shown in Figure 1; four possible ways of transferring information between *A* and *B* are shown in Figure 2.

It will be noticed that in the first two transfers, (1) and (2), a pulse must be applied across the *A* and *B* diodes, whereas in (3) and (4) this is not necessary. Thus there are two types of transfer: (1) and (2) transfers, which are always clocked and hence are synchronous, and (3) and (4) transfers, which are asynchronous, and happen as soon as the input tunnel diodes are set.

The logical operations *and* and *or* can be achieved by connecting extra rectifier diodes to the right hand tunnel diode of each pair; this is illustrated for pairs (1) and (2) in Figure 3.

If (1) is an "OR" circuit then (2) must be an "AND" circuit and vice versa depending on how we define a "ONE" and a "ZERO." If we define a "ONE" as a negative level and a "ZERO" as a positive level, then a "ONE" is represented by a low state in an *A* diode, or a high state in a *B* diode. Thus Figure 3 (1) is an "OR"-circuit, since a low state (negative level) in either of the three inputs will switch the right hand tunnel diode to its high state (also a negative level). Similarly, Figure 3 (2) is an "AND" circuit and Figure 2 (3) and (4) can be made into "AND" and "OR" circuits, respectively.

Figure 4 illustrates the basic operation of Figure 3 (1). The rectifier is normally cut off, and a transfer is effected by simultaneous clock pulses, representing 500 *mv* total between *A* and *B*. A comparison of the tunnel diode and rectifier curves shows that the total clock amplitude must be greater than 350 *mv* to transfer a "ONE," and less than 800 *mv* to make sure a *ZERO* is not transferred as a "ONE." This is a fairly wide tolerance, and an actual value of 500 *mv* (i.e., ± 250 *mv*) is used for the clock. To ensure routing of information from *A* to *B*, and not vice versa, the bias current $I_B$ is made greater than $I_A$.

The important logical functions of inhibit and inversion are shown in Figure 5. The two tunnel diodes $B_1$ and $B_2$ are in series, and an input at *X* inhibits an input at *Y* as follows. If *Y* is a "ONE" and *X* a *ZERO* then the *transfer in* clock will set $B_2$ to its high state and so result in a negative output, hence a "ONE." However, if *X* is a "ONE" then $B_1$ is set to the high state and prevents a −250 *mv* level at *Y* from setting $B_2$, resulting in a positive output (a "ZERO") when a transfer-out pulse is applied to $D_1$. Thus *X* inhibits *Y*, and if a permanent "ONE" is applied to *Y* then an input at *X* becomes inverted at the output.

The system is therefore very flexible, since it consists of both synchronous and asynchronous "AND" and "OR" circuits, and any logical operation can be performed.

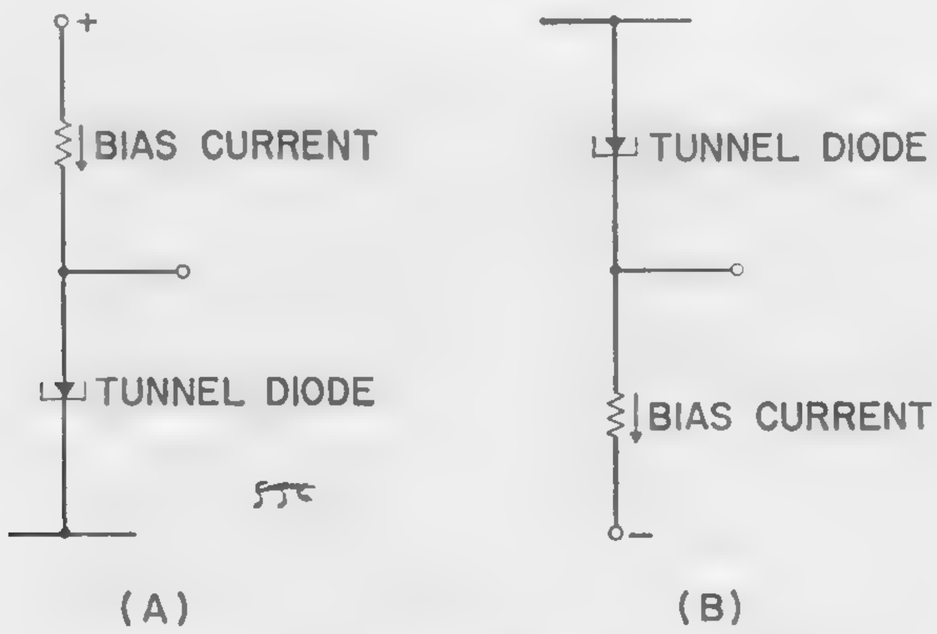



**Figure 1—The two types of basic circuit.**

* To be presented during *informal evening discussion E.4* in *Ballroom West* at the *Sheraton Hotel.*

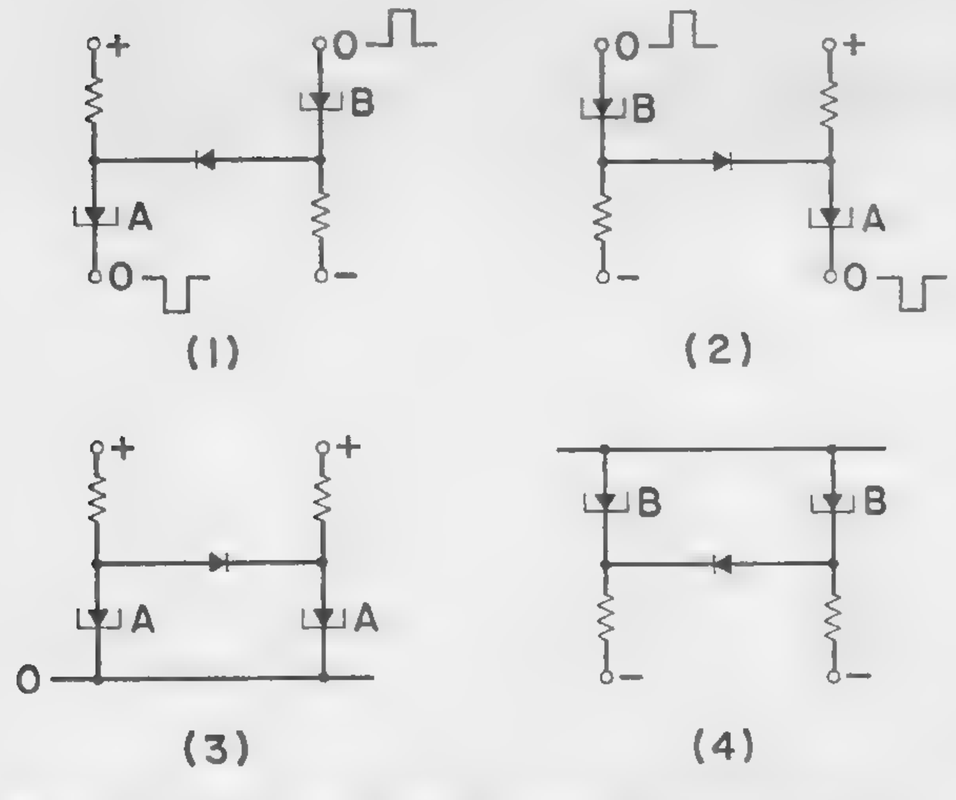
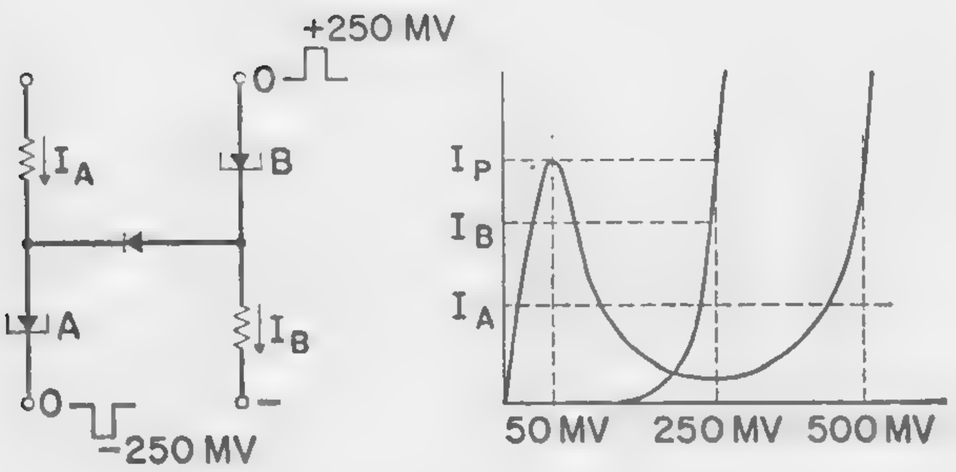



**Figure 2—The four basic transfer connections: (1) *A* to *B*, (2) *B* to *A*, (3) *A* to *A*, (4) *B* to *B*; direction of transfer is from left to right.**




$$V_{CLOCK} \begin{cases} > 50\,MV + 250\,MV + 50\,MV = 350\,MV \\ < 500\,MV + 250\,MV + 50\,MV = 800\,MV \end{cases}$$

**Figure 4—Tolerance on the synchronous transfer pulse voltage between the two tunnel diodes with germanium rectifier diode coupling.**

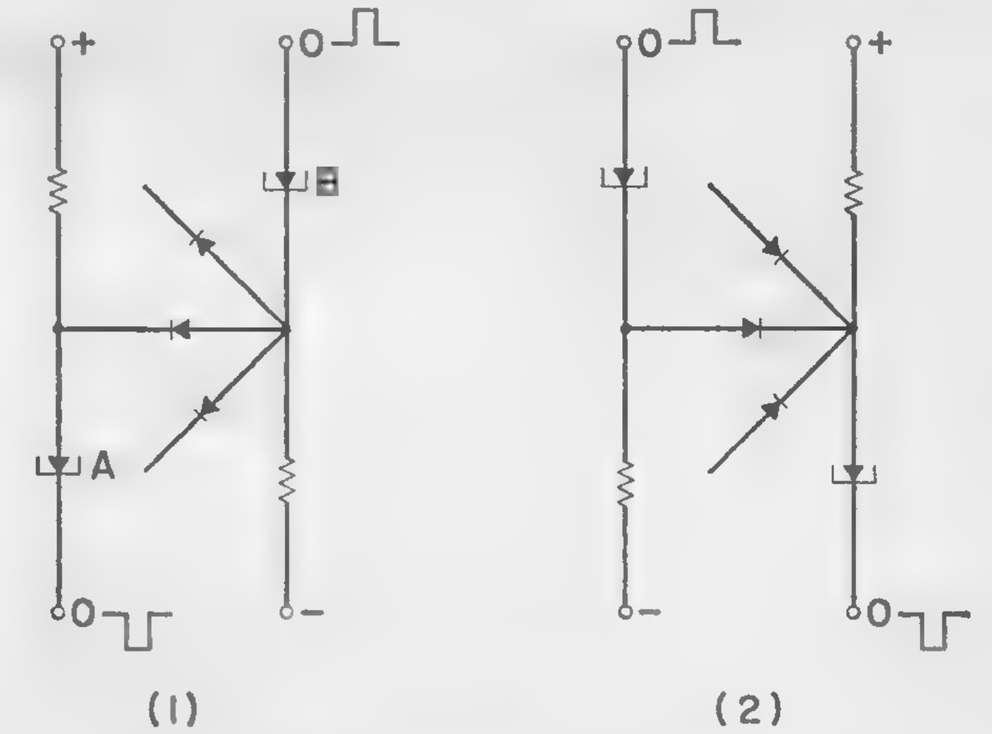



**Figure 3—*(1)* Synchronous OR circuit, and *(2)* synchronous AND circuit.**

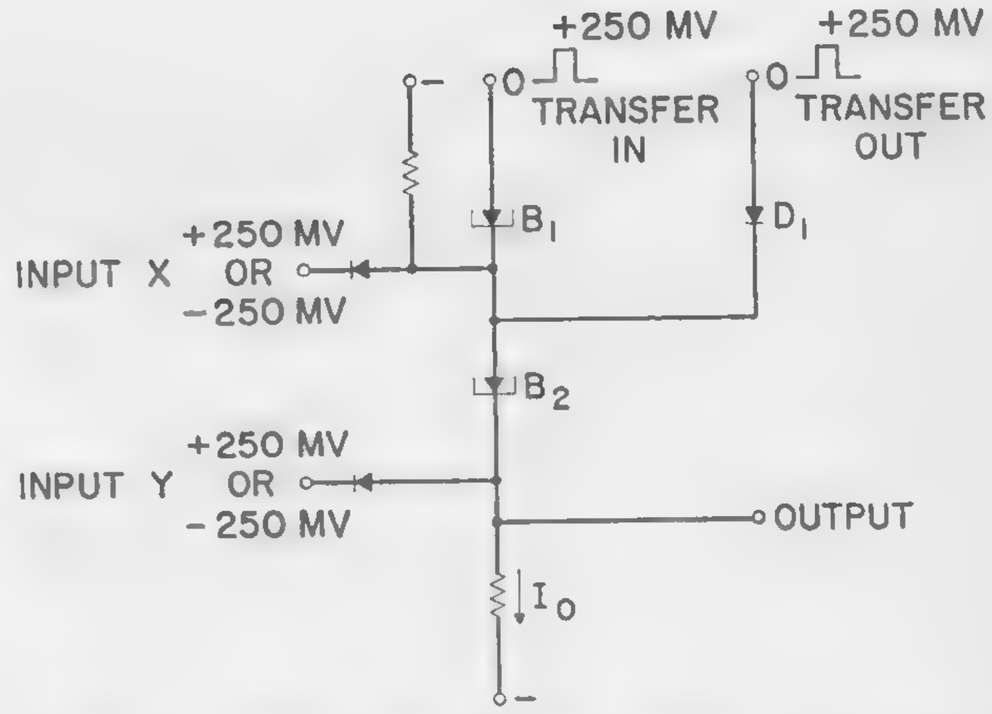



**Figure 5—Inhibit and inverter circuit. A ONE at input *X* inhibits a ONE at input *Y*. A permanent ONE at *Y* inverts the input at *X*.**

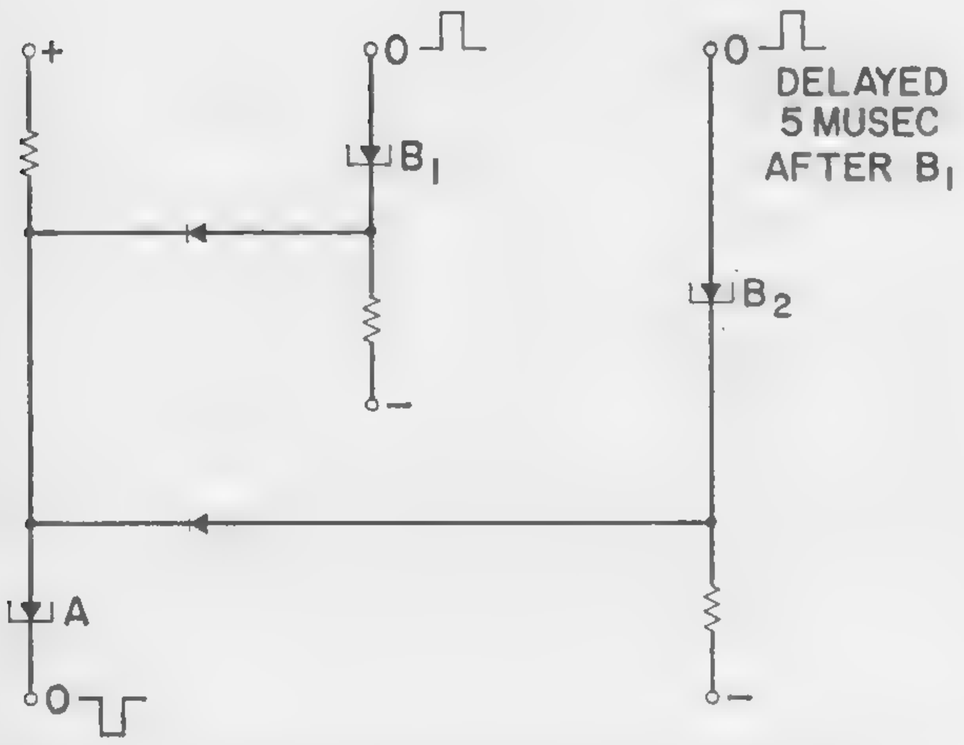
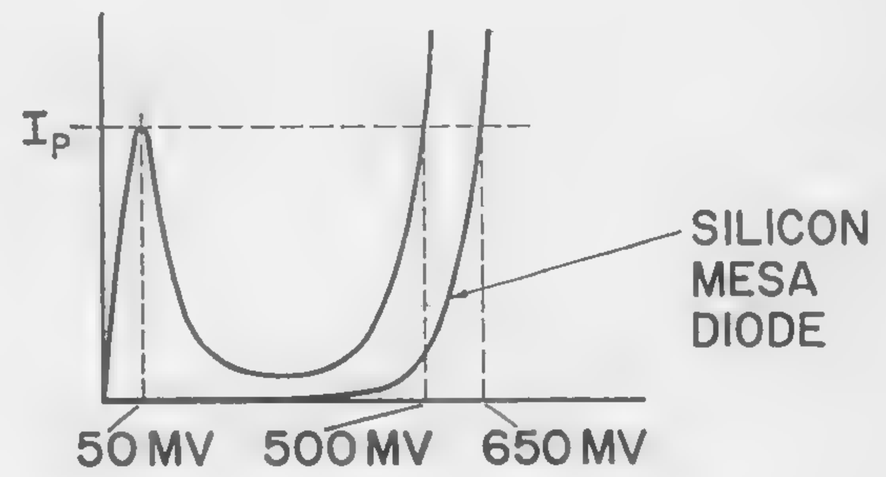



**Figure 6—Fan-out by time multiplex. This imposes little restriction on speed, since most logical circuits require their inputs at different times.**




$$V_{CLOCK} \begin{cases} > 750\,MV \\ < 1200\,MV \end{cases}$$

**Figure 7—Silicon mesa or gallium-arsenide rectifier coupling diodes improve the isolation of adjacent circuits during a synchronous transfer.**

## Informal Discussion Session

### E.4/2: A Fast-Word Organized Tunnel-Diode Memory Using Voltage-Mode Selection*

G. B. B. Chaplin and P. M. Thompson

Plessey Company, Ltd.

Hants, England

THE MINIMUM NUMBER of components per bit of a tunnel diode store is probably one tunnel diode, one biasing resistor, and some means for reading and writing information. The reading and writing can be accomplished by voltage selection through a rectifier diode, and the resulting circuit for one bit of the store is shown in Figure 1.

In this example, the rectifier diode is a conventional computer gold-bonded diode of the same basic material as the tunnel diode (i.e., germanium) but is much more lightly doped, so its forward conducting potential is about 250 *mv* compared with 500 *mv* for the tunnel diode.

The state of the tunnel diode may be read as follows: Let us assume that the digit line is held at ground potential, and the effect of taking the word line negative. Then, if the tunnel diode is in the low voltage state, the rectifier diode will conduct when the word line is at— 300 *mv* (i.e., — 50 *mv* — 250 *mv*), a current will flow in the digit line, and the tunnel diode will switch to the high voltage state. But if the tunnel diode were in the high-voltage state, no current would flow in the read line until the word line reached — 750 *mv* (i.e., — 500 *mv* — 250 *mv*). Thus the state of the diode can be read with a negative pulse of magnitude between — 300 *mv* and — 750 *mv*, and the tunnel diode will always be left in the high voltage state. However, if the digit line were held negative, the rectifier diode could not conduct, and the tunnel diode would not be switched into the high voltage state. Thus new information may be written into the tunnel diode by first returning it to the low voltage state, by momentarily reducing $I_o$ to zero, then applying a pulse (similar to the read pulse) to the word line. The digit line is held at ground potential if a high voltage state is required, and negative if a low voltage state is required.

The digit line is connected to a read transistor emitter as shown in Figure 2. During reading, a low-voltage state in the tunnel diode results in a negative pulse at the collector of $J_1$, when a negative pulse is applied to the word line, and the base of $J_1$ is at ground potential. For writing, the potential of the base of $J_1$ determines the final state of the tunnel diode, $J_1$ operating as an emitter follower.

The store is organized as in Figure 3. A word is selected by a pulse on a word line and each word is reset between read and write operations by a negative pulse on the bias resistors.

The read transistor can be made bistable as shown in Figure 4, so that when a digit is read by the word pulse, it is automatically written back by the next word pulse, unless overidden by an external pulse on the transistor base.

Each read transistor has as many diodes connected to its emitter as there are words, and their self capicitance sets a limit to the speed of the store. For this reason the store is constructed on printed boards, each containing *8* digits of *8* words; *64* bits. The complete cycle consists of read, reset the word, write, and reset the read transistors and takes 40 *μsec*. Each board is self contained and as many as required can be plugged in.

The read and write circuits are simple and the cost of components, per bit of stored information, is little more than that of one germanium tunnel diode, one rectifier diode and a resistor.

* To be presented during *informal evening discussion E.4* in *Ballroom West* at the *Sheraton Hotel.*

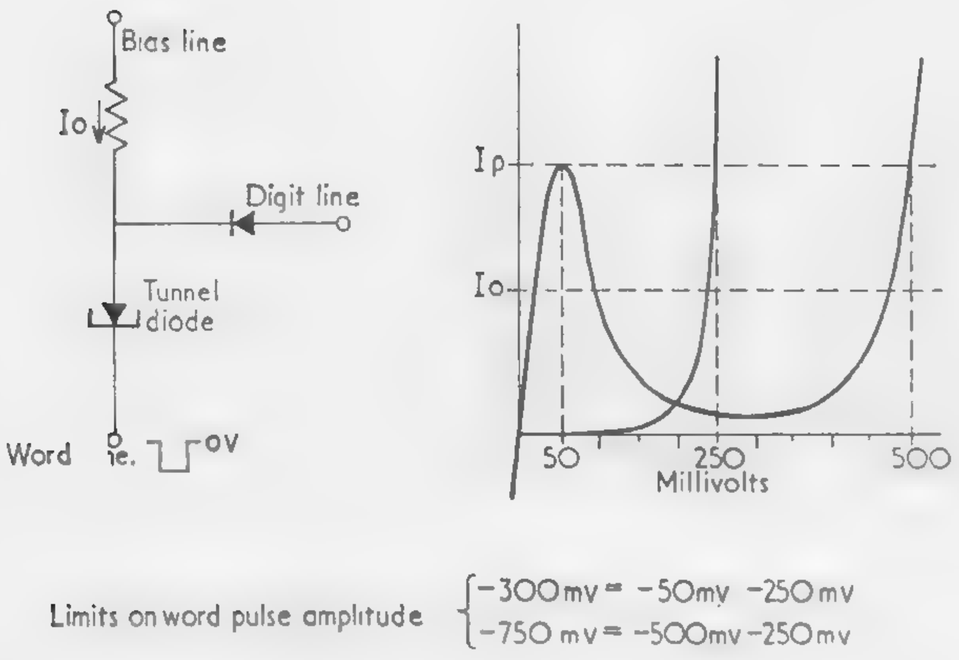



**Figure 1—A basic memory cell. A pulse on the word line of between — 300 *mv* and — 750 *mv* will result in a current in the digit line only if the tunnel diode is in the low voltage state.**

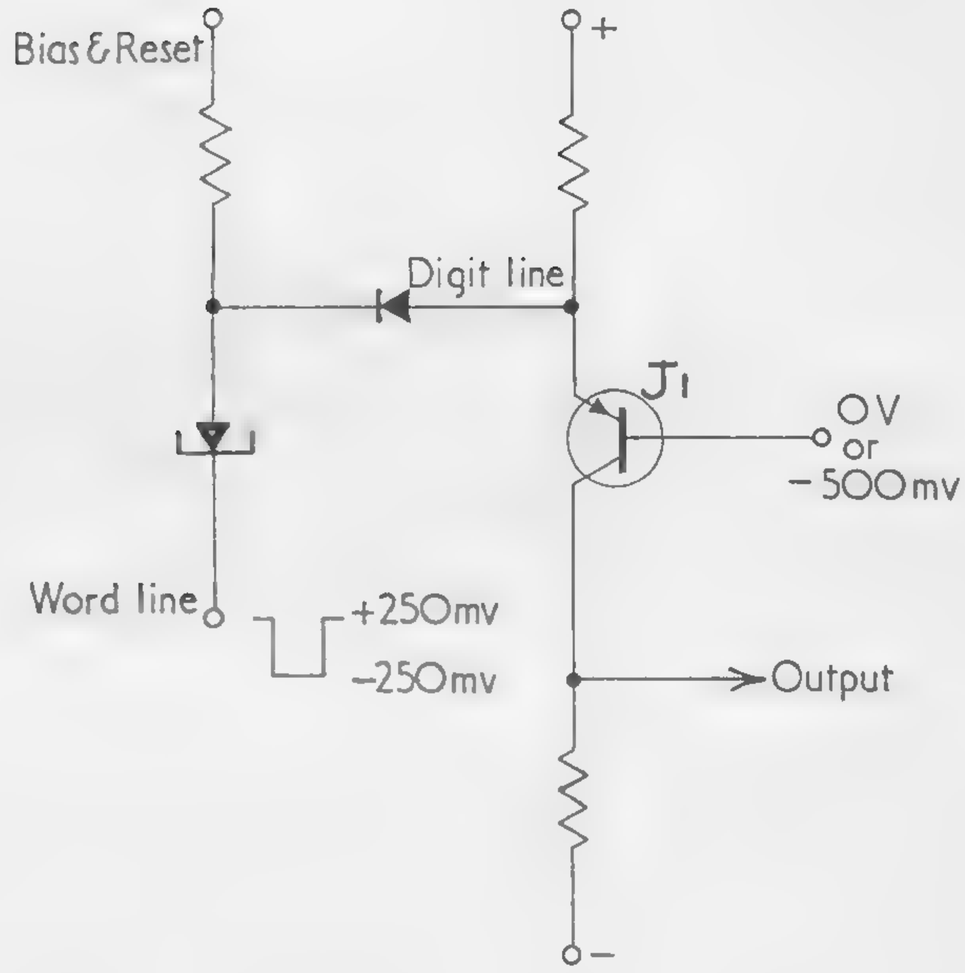



**Figure 2—A memory cell and read transistor. Note that the potentials of the word-line pulse have been shifted to compensate the emitter base voltage of $J_1$.**

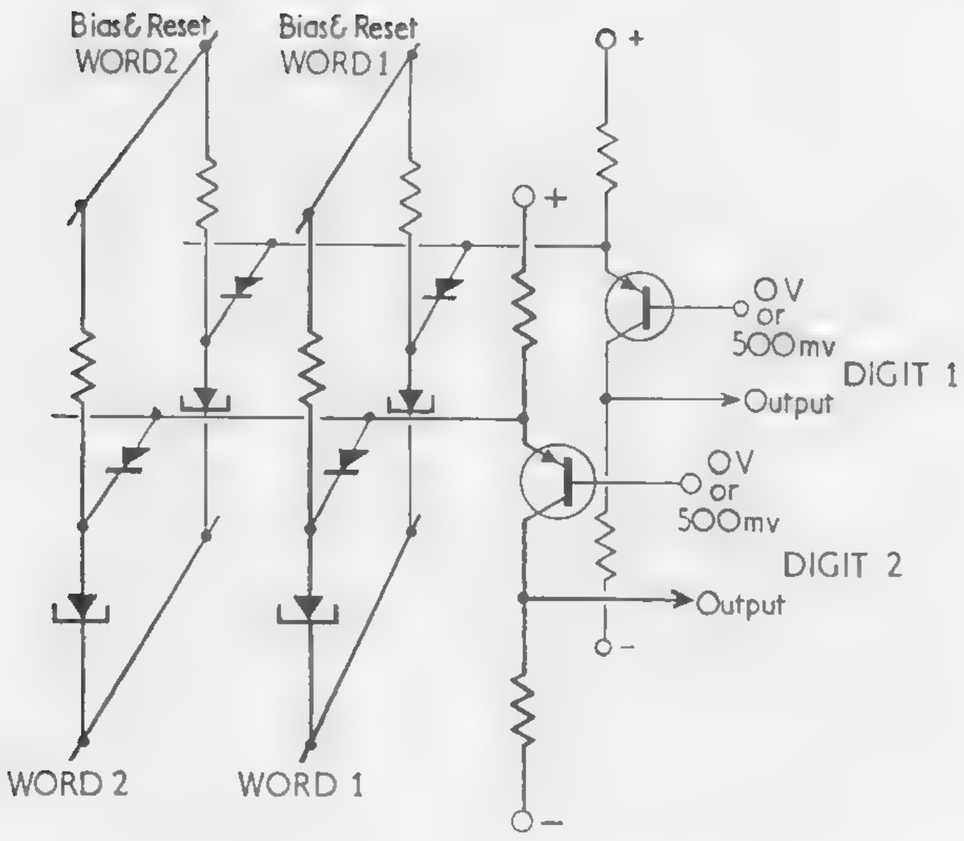



**Figure 3—Organization of memory illustrating two words of two digits. The base of the read transistors are held at o*v* to write a *ONE* or to read, and —500 *mv* to write a *ZERO*.**

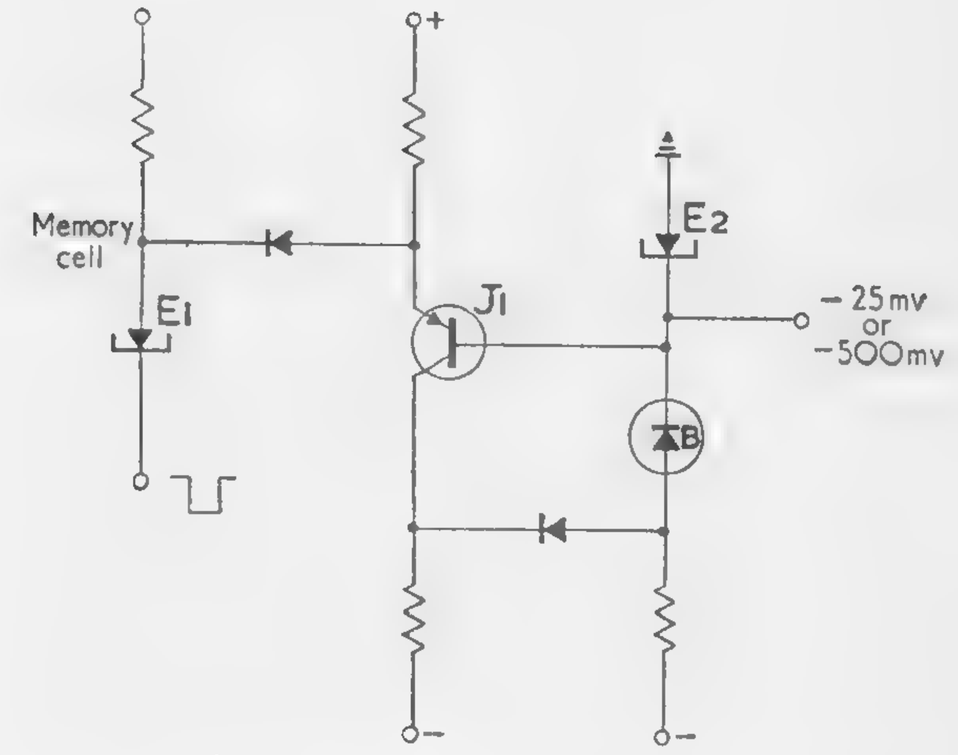



**Figure 4—The read transistor which is made bistable by addition of tunnel diode $E_2$.**

## SESSION IV: Power and Control

Chairman: P. F. Pittman
Westinghouse Electric Corp., Pittsburgh, Pa.

### 4.1: Super Saturated Transistor Switches

**J. F. Gibbons**

Stanford Electronics Laboratories, Stanford University

Stanford, Calif.

A SIMPLE TRANSISTOR SWITCHING CIRCUIT is shown in Figure 1(*a*). The switch is *OFF* when $V_B$ is negative, [i.e., of opposite polarity to that shown in Figure 1*(a)*], and *ON* when $V_B$ is positive and of sufficient magnitude for $(V_B/R_B)$ to provide a saturating level of base current for the transistor. In the *ON* position, it is convenient to construct a *Thevenin* equivalent for the load terminals of the switch, as in Figure 1*(b)*. In this figure, $V_O$ is called the offset voltage and $R_{ON}$ is called the *ON* impedance, each of which is a function of the base current. Since $V_O$ and $R_{ON}$ would be zero for an ideal switch, their size in a real circuit provides a measure of how closely the transistor switch approximates its ideal circuit counterpart in the *ON* condition.

If it is assumed that the transistor is operating under low-level conditions, $V_O$ and $R_{ON}$ may be readily calculated from the *Ebers* and *Moll*[1] equations. They obtain, for the circuit configuration given in Figure 1, and $I_C$ very small

$$V_O = kT/q \quad ln \quad 1/\alpha_i \quad (\cong kT/q\beta_i)$$
$$R_{ON} = kT/qI_B \quad [\,1-\alpha_N/\alpha_N + 1 - \alpha_I\,]$$

The assumption of a low-level operating condition thus yields a $V_O$ which is independent of $I_B$ and an $R_{ON}$ which is inversely proportional to $I_B$ (for small $I_C$).

Measurements made on a typical germanium-alloy transistor at low load currents are shown in Figure 2. The inverted connection is shown, though similar results are obtained for the normal connection. It is apparent that $V_O$ ($V_{CE}$ when $I_E$ equals zero) is not constant; a simple calculation shows that $R_{ON}$, which is the slope of the lines in Figure 2, is not inversely proportional to the base current. Hence, for most practical base drives, low-level conditions do not apply.

This paper will show how to calculate $V_O$ and $R_{ON}$ in the presence of intermediate-level operating conditions[2]. We are especially interested in alloy switching transistors which are operated in the *super-saturated* condition — i.e., $V_O$ and $R_{ON}$ for load to base current ratios which are less than unity. These operating conditions are applicable in a broad class of choppers and analog-to-digital converters.

To perform the calculations, we used the lumped model for a $p\,n\,p$ transistor shown in Figure 3. The elements of the model in Figure 4 are essentially proportionality constants connecting currents to carrier densities; they are defined to account for the current flows in Figure 3. The model is more general than the corresponding low-level model[3] in that: (1)—The recombination currents in the base depend on the $NP$ product instead of simply on $P$; (2)—a more general relationship between carrier densities and junction voltage than that which applies for low-level calculations is used. Since the model does not provide for truly high-level phenomena, such as emitter crowding and a further change of the recombination law, we anticipate that the theory will only be valid up to certain base current levels. However, this is not a serious objection for base currents of less than 8-10 *ma* for the transistors considered in this study, and these base drives cover the range of applications previously mentioned.

The equations given in Figure 5 may be combined to yield exact values of $V_O$ and $R_{ON}$. Useful approximations to these formulas for the inverted connection of the transistor are

$$V_O \cong kT/q\beta_N \quad \sqrt{1+4I'_B\,/\,(1+A_C/A_E)}$$
$$R_{ON} \cong (1+A_C/A_E)\,V_O/I_B$$

In these formulas $A_C$ and $A_E$ are the collector and emitter areas and $I'_B$ is a normalized base current.

### *Comparisons Between Practice and Theory*

Comparisons between experiment and theory are given in Figures 6 and 7. Figure 6 compares the calculated values of $V_O$ and $R_{ON}$ for the 2*N*598 represented in Figure 2. Figure 7 shows values of $V_O$ and $R_{ON}$ calculated for a 2*N*1302 from the *typical parameters* given by the manufacturer, together with measured values of $V_O$ and $R_{ON}$ for two units. The quality of the agreement in Figures 6 and 7 is considered to be satisfactory.

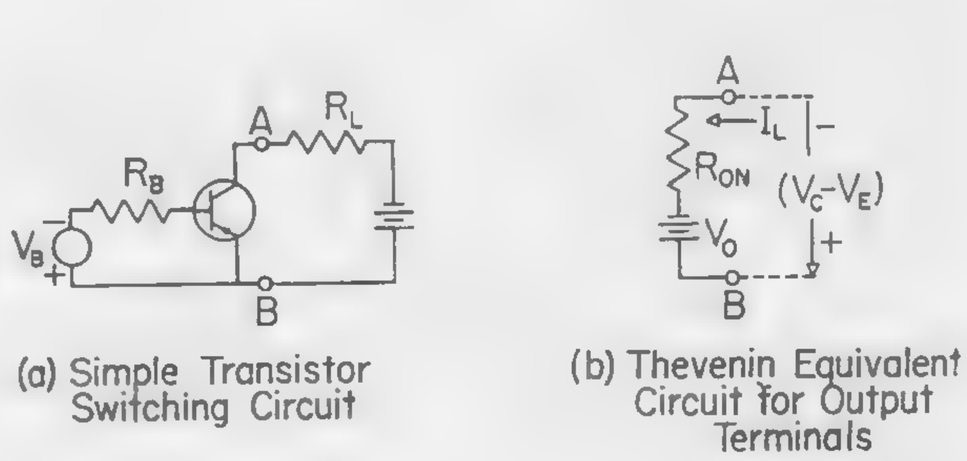



**Figure 1—Simple transistor switching circuit and *Thevenin* equivalent circuit for output terminals.**

[1] Ebers, J. J., Moll, J. L., "Large Signal Behavior of Junction Transistors," *Proc. IRE;* December, 1954.

[2] For a somewhat different approach to some of the same problems considered here, Mead, C. A., *Solid State Electronics;* July, 1960.

[3] Linvill, J. G., "Lumped Models for Transistors and Diodes," *Proc. IRE;* June, 1958.

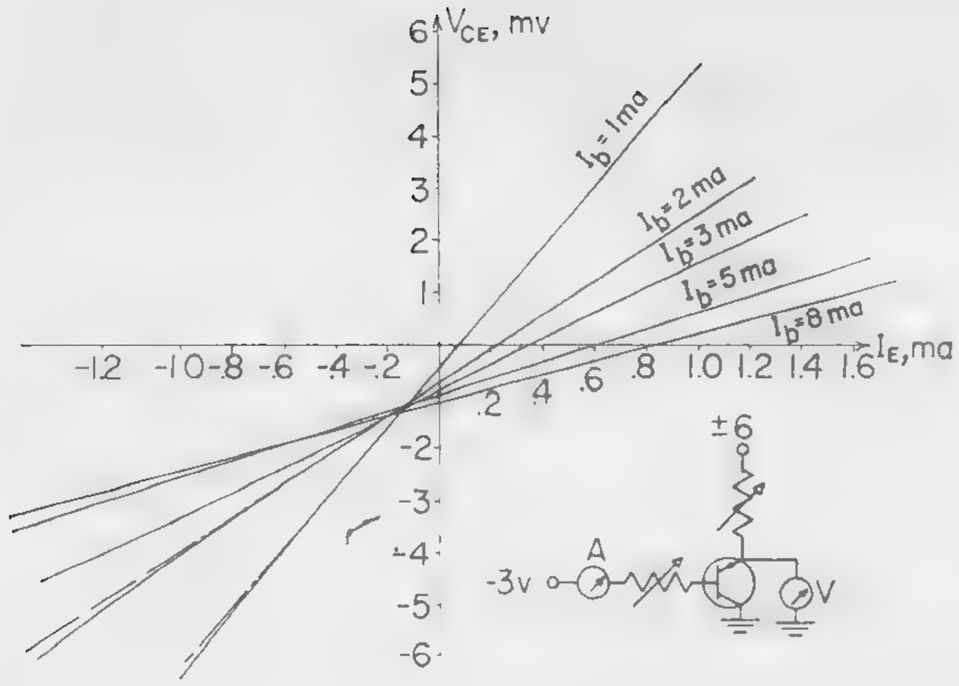



**Figure 2—Experimental measurement of $V_{CE}$ versus $I_E$ for a 2N598 in inverted connection.**

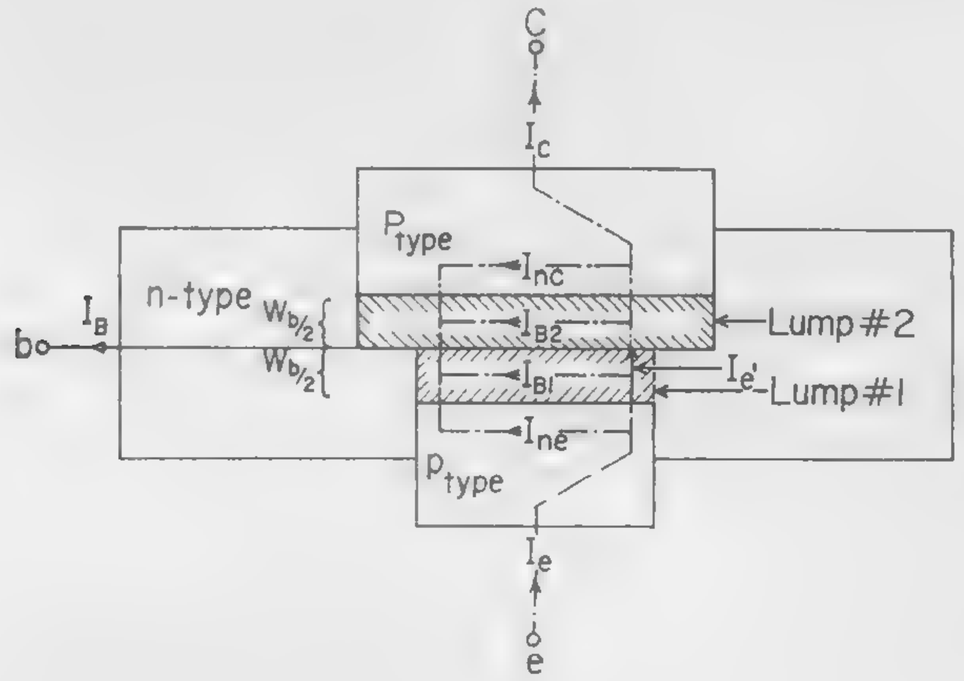
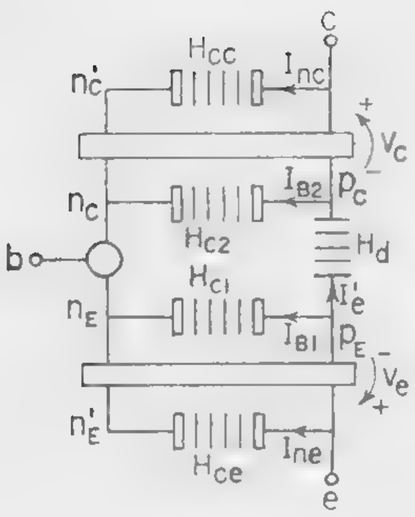



**Figure 3—Approximate physical structure of an alloy switching transistor with current flow diagram.**




$n_C' = n_{pc}(e^{qv_c/kT} - 1)$ } Law of collector-base junction.

$n_C p_C = n_i^2 e^{qv_c/kT}$

$n_E p_E = n_i^2 e^{qv_e/kT}$ } Law of emitter-base junction.

$n_E' = n_{pE}(e^{qv_e/kT} - 1)$

**Figure 4—Lumped model for Figure 3.**

$$I_{nc} = n_C' H_{CC} = \left(\frac{qA_C L_{nc}}{\tau_{nc}}\right) n_C'$$

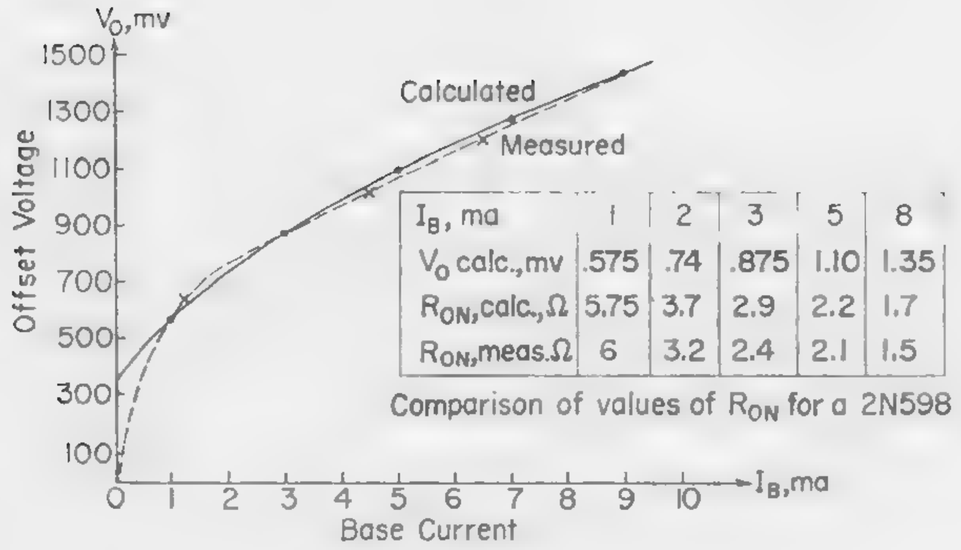
$$I_{B2} \cong H_{C2} N_D (p_C n_C / N_D^2) = \frac{qA_C W_b N_D}{2\tau_{pb}} \left[\frac{p_C}{N_D}\left(1 + \frac{p_C}{N_D}\right)\right]$$

$$I_e' = H_D (p_E - p_C) = \frac{qA_E D_p N_D}{W_b} \left[\frac{p_E}{N_D} - \frac{p_C}{N_D}\right]$$

$$I_{B1} \cong H_{C1} N_D (p_E' n_E / N_D^2) = \frac{qA_E W_b N_D}{2\tau} \left[\frac{p_E}{N_D}\left(1 + \frac{p_E}{N_D}\right)\right]$$

$$I_{ne} = n_E' H_{ce} = \frac{qA_E L_{nE}}{\tau_{nE}} n_e'$$

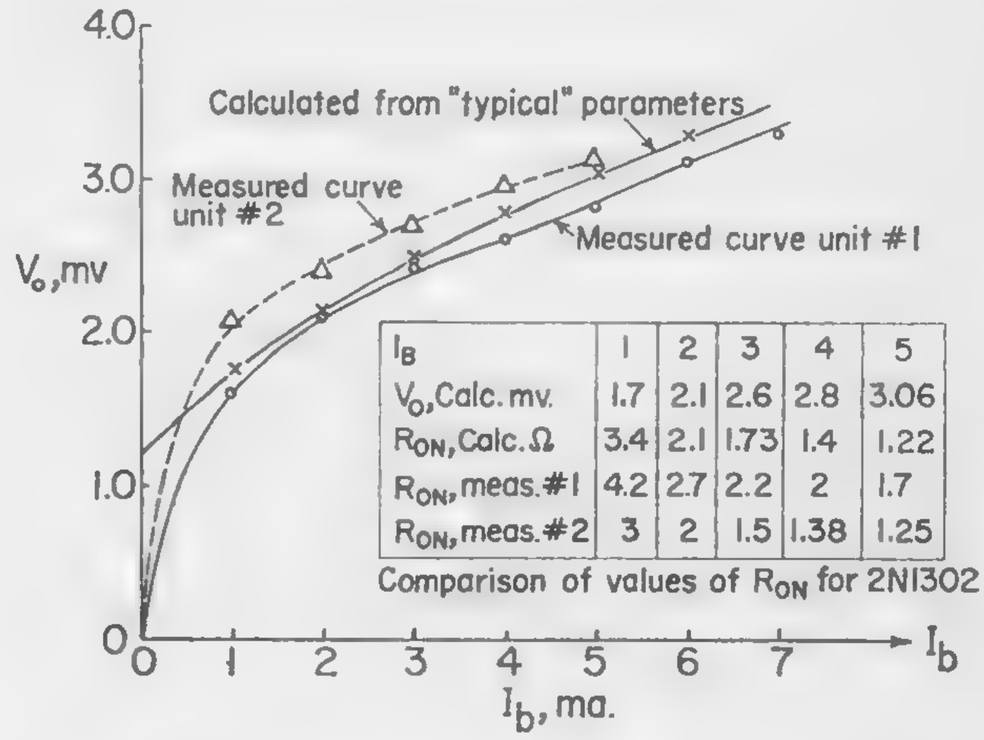
**Figure 5—Equations for current components indicated in Figure 3.**




| $I_B$, ma | 1 | 2 | 3 | 5 | 8 |
|---|---|---|---|---|---|
| $V_O$ calc.,mv | .575 | .74 | .875 | 1.10 | 1.35 |
| $R_{ON}$,calc.,Ω | 5.75 | 3.7 | 2.9 | 2.2 | 1.7 |
| $R_{ON}$,meas.Ω | 6 | 3.2 | 2.4 | 2.1 | 1.5 |

Comparison of values of $R_{ON}$ for a 2N598

**Figure 6—Calculated and measured dependence of $V_O$ and $R_{ON}$ versus $I_B$ for 2N598.**




| $I_B$ | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|
| $V_O$,Calc. mv. | 1.7 | 2.1 | 2.6 | 2.8 | 3.06 |
| $R_{ON}$,Calc.Ω | 3.4 | 2.1 | 1.73 | 1.4 | 1.22 |
| $R_{ON}$,meas.#1 | 4.2 | 2.7 | 2.2 | 2 | 1.7 |
| $R_{ON}$,meas.#2 | 3 | 2 | 1.5 | 1.38 | 1.25 |

Comparison of values of $R_{ON}$ for 2N1302

**Figure 7—Calculated and measured dependence of $V_O$ and $R_{ON}$ versus $I_B$ for 2N1302.**

## SESSION IV: Power and Control

### 4.2: A New DC Differential Transistor Amplifier

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THE STABLE AMPLIFICATION of low level signals of less than 1 millivolt magnitude has usually been done with a carrier-type feedback amplifier employing a complex modulation-demodulation system incorporating a short-lived and bulky mechanical chopper. The much simpler all-transistor *dc* differential amplifier, however, has not been suitable due to drifts in gain and operating point during aging and temperature variations. This paper will relate improvements in both, as a result of improved device characteristics obtained with the double-diffused planar silicon transistors having a passivated surface[1], and a compound transistor circuit.

It shall be shown that this circuit offers quite good incremental gain stability, with single ended as well as differential output capabilities.

#### *The Conventional Differential Stage Characteristics*

*Okada*[2] has shown for the generalized transistor differential stage, Figure 1, that the output function can be described as a function of the device current gains, emitter-base terminal voltages, and collector reverse-bias currents; Figure 2. There it is assumed that $\alpha$ remains constant, $R_L << r_c$, and $R_{ek}$ and $R_{bk}$ include the extrinsic device emitter and base resistances, respectively. It should be noted, however, that for devices such as the double-diffused planar passivated type, the magnitudes of $r_e'$ and $r_b'$ are trivial, and may therefore be neglected.

To establish a *dc* balance condition ($\Delta E_o$ and $\Delta E_{in}$ both zero), the remainder of the output equation must sum to zero. The term relating to $V_{EE}$ may be made quite small by making $R_{ee}$ sufficiently large, readily accomplished by employing the impedance gain of a transistor operated as a current source. Then, for ideally matched transistors, where $\Delta V_{BE}$ and $\Delta (R_b \cdot I_{co})$ are zero, the balance is attained. Since the ideal case is seldom realized, the relative magnitudes of $R_{e1}$ and $R_{e2}$ are varied, resulting in unequal emitter currents. This method is undesirable, however, where the temperature cannot be maintained constant as the $V_{BE}$ temperature coefficient is a function of the emitter current; Figure 3*a*.

A further consideration affecting operating point stability is the magnitude of the source impedances $R_{b1}$ and $R_{b2}$. Since $\beta$ and $I_{co}$ increase with temperature, the input current can change quite appreciably. This change, $\Delta I_{in}$, through $R_b$ behaves as an error signal introduced with the desired input. For the class of transistors mentioned previously, a typical distribution of $I_{co}$ versus temperature is given in Figure 3*b*. Considering the magnitudes involved, ($R_{b1} \cdot I_{co1}$—$R_{b2} \cdot I_{co2}$) will remain small for $R_b$ ranging to $10^3$-$10^4$ ohms at temperatures up to 100-125°C. However, the equivalent-input-drift resulting from $\beta$ variations is generally larger in magnitude than that introduced by $\Delta I_{co}$, and requires $\beta$ large in magnitude and well matched for best performance.

The incremental (small-signal) gain characteristics of the stage are sensibly those of the common-emitter stage with emitter series resistance. However, it must be noted that since the limit value of the voltage gain is $R_L/R_e$, it is immediately apparent that when $R_{e1} \neq R_{e2}$ the gains of the two halves are no longer equal and single-ended output is not desirable.

#### *The Compound Block Differential Stage*

The purpose of the improved amplifier is to realize the advantages of the uniform $\Delta V_{BE}/\Delta T$ behavior inherent in the planar-passivated device, and to achieve an independence of current gain variations with temperature. The fundamental circuit embodying these principles is shown in Figure 4. The resistances are chosen such that $R_{e1} = R_{e2}$, and $R_{L1} = R_{L2}$. Breakdown diodes $D_1$ and $D_2$ are selected to provide a positive voltage-temperature coefficient which cancels the negative emitter-base coefficients of $Q_2$ and $Q_3$, and to furnish a voltage drop sufficiently large that $R_3 >> h_{ic2}$ for the required $I_{C1}$ (and $I_{C4}$). The *dc* balance is attained by varying $R_3$ to supply the proper base current to $Q_2$. The magnitude of $I_{C1}$, and hence $R_3$, is chosen such that $\Delta I_{b2} << I_{C1}$, where $\Delta I_{b2}$ is the quiescent excursion of $I_{b2}$ over the operating temperature range. By this choice, $I_{C1}$ will remain essentially constant regardless of temperature variations, and the $\Delta V_{BE}/\Delta T$ coefficients of $Q_1$ and $Q_4$ will be sensibly equal for matched devices. By this criteria, $I_{C1}$ is typically an order of magnitude less than $I_{C2}$ and hence $I_{B1}$ will be correspondingly less than for the conventional stage input. The *block* current gain is thus increased by an order of magnitude. This effect is immediately evident in the reduction of equivalent-input-drift resulting from $\beta$ variations.

The small-signal gain more nearly approaches the limit value of $R_L/R_e$ than does the conventional stage.

The advantages obtained by the *pnp/npn* pairs may be extended by the addition of a third transistor to the group. Such a circuit is shown in Figure 5. The input current is typically less than 0.1% of the load current and hence operation with higher values of $R_b$ is permissible. A further increase of small-signal gain is also realized. Figure 6 gives a comparison of the differential small-signal gain behavior for the three stage types discussed.

The circuits described (Figures 4 and 5) have been operated well over the temperature range of —55°C to +125°C with equivalent input drifts in the range of 4-6$\mu V$/°C. They are ideally suited to single-ended output operation, and have excellent common mode rejection. The input transistors alone require selection, the other units being non-critical.

#### *Credits*

The author acknowledges with gratitude the many helpful discussions held with *V. H. Grinich* and *C. T. Sah.*

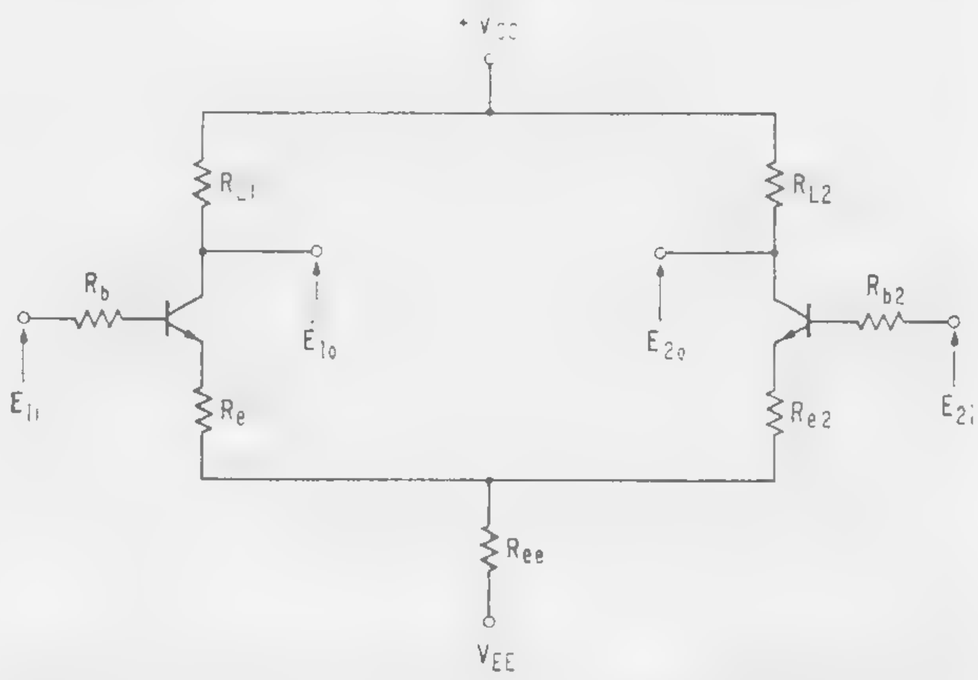



**Figure 1—The generalized transistor differential stage.**

[1] Hoerni, J. A., "Planar Silicon Transistors and Diodes," 1960 Electron Devices Meeting, Washington, D. C.; October, 1960.

[2] Okada, R. H., "Stable Transistor Wide-band and DC Amplifiers," *AIEE Electronics and Communications*, p. 26-33; March, 1960.

$$E_{20} - E_{10} = \frac{(E_{1L} - E_{2i})(\alpha_1 R_{L1} + \alpha_2 R_{L2})}{\Delta}$$

$$+ \frac{(V_{BE2} - V_{BE1})(\alpha_1 R_{L1} + \alpha_2 R_{L2})}{\Delta}$$

$$+ \frac{(R_{b2} I_{CO1} - R_{b2} I_{CO2})(\alpha_1 R_{L1} + \alpha_2 R_{L2})}{\Delta}$$

$$+ \frac{\frac{V_{EE}}{R_{ee}}\left(\frac{R_{b1}}{\beta_1} + R_{E1} - \frac{R_{b2}}{\beta_2} - R_{E2}\right)\left(\alpha_1 R_{L1} + \alpha_2 R_{L2}\right)}{\Delta}$$

$$+ (I_{CO1} R_{L1} - I_{CO2} R_{L2})$$

$$\text{Where } \Delta = R_{e1} + R_{e2} + \frac{R_{b1}}{\beta_1} + \frac{R_{B2}}{\beta_2} + \frac{R_{b1} R_{b2}}{\beta_1 \beta_2 R_E}$$

**Figure 2—The differential output of the generalized stage.**

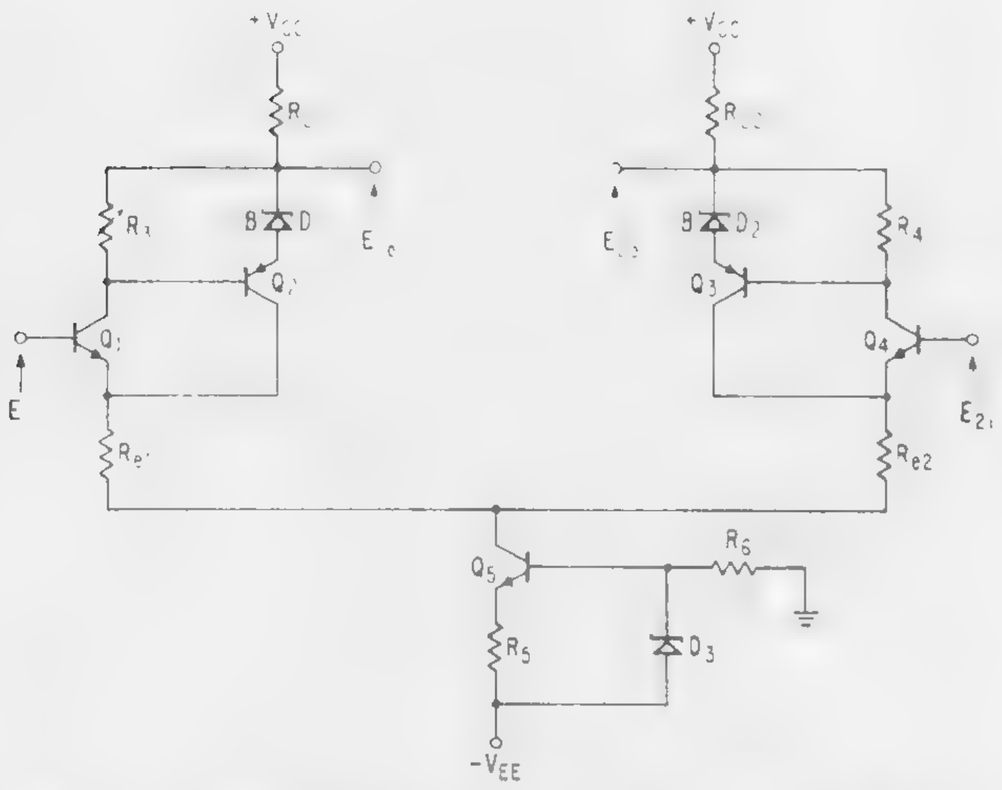
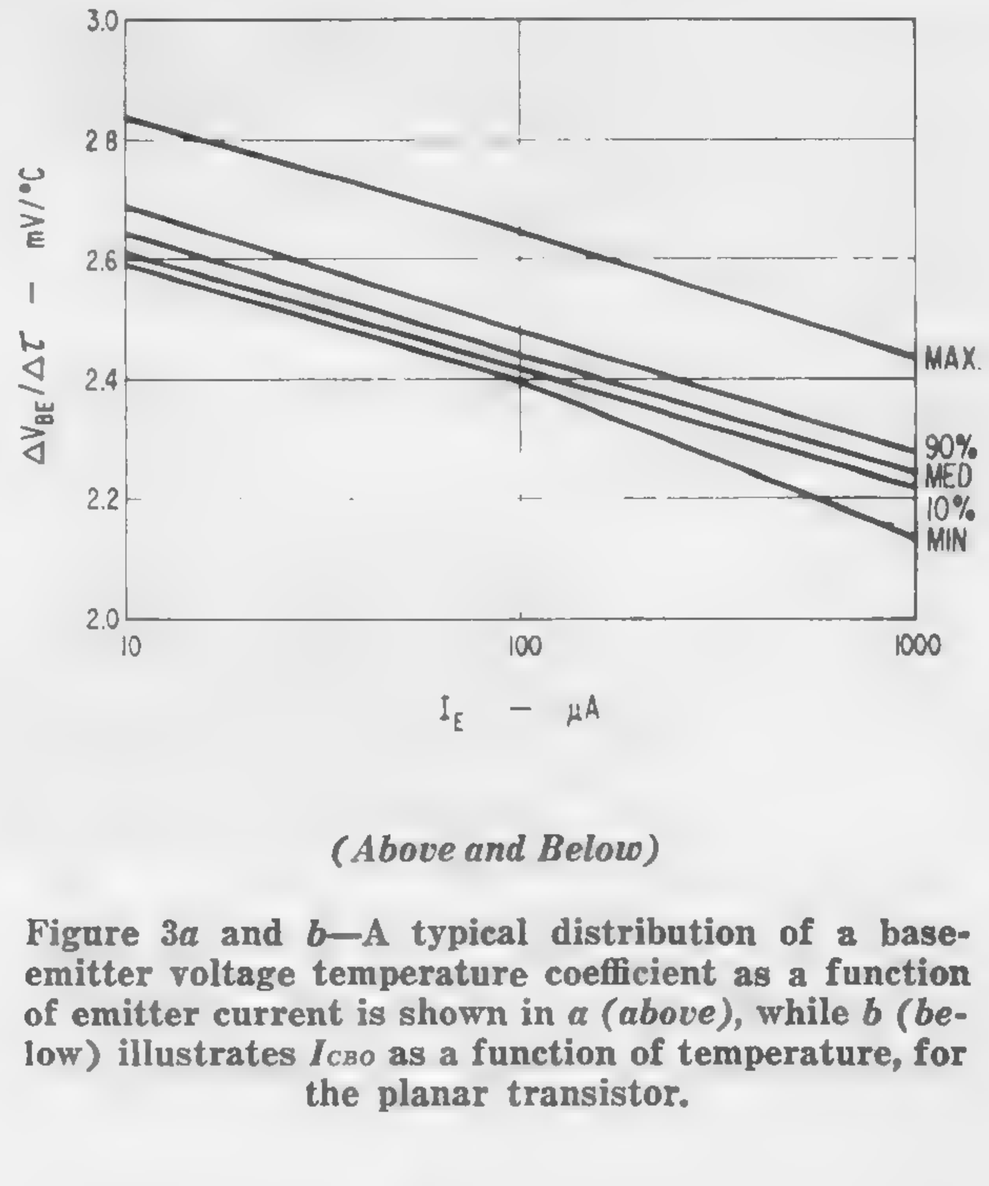



**Figure 4—The fundamental *pnp/npn* compound *block* amplifier.**




*(Above and Below)*

**Figure 3*a* and *b*—A typical distribution of a base-emitter voltage temperature coefficient as a function of emitter current is shown in *a (above)*, while *b (below)* illustrates $I_{CBO}$ as a function of temperature, for the planar transistor.**

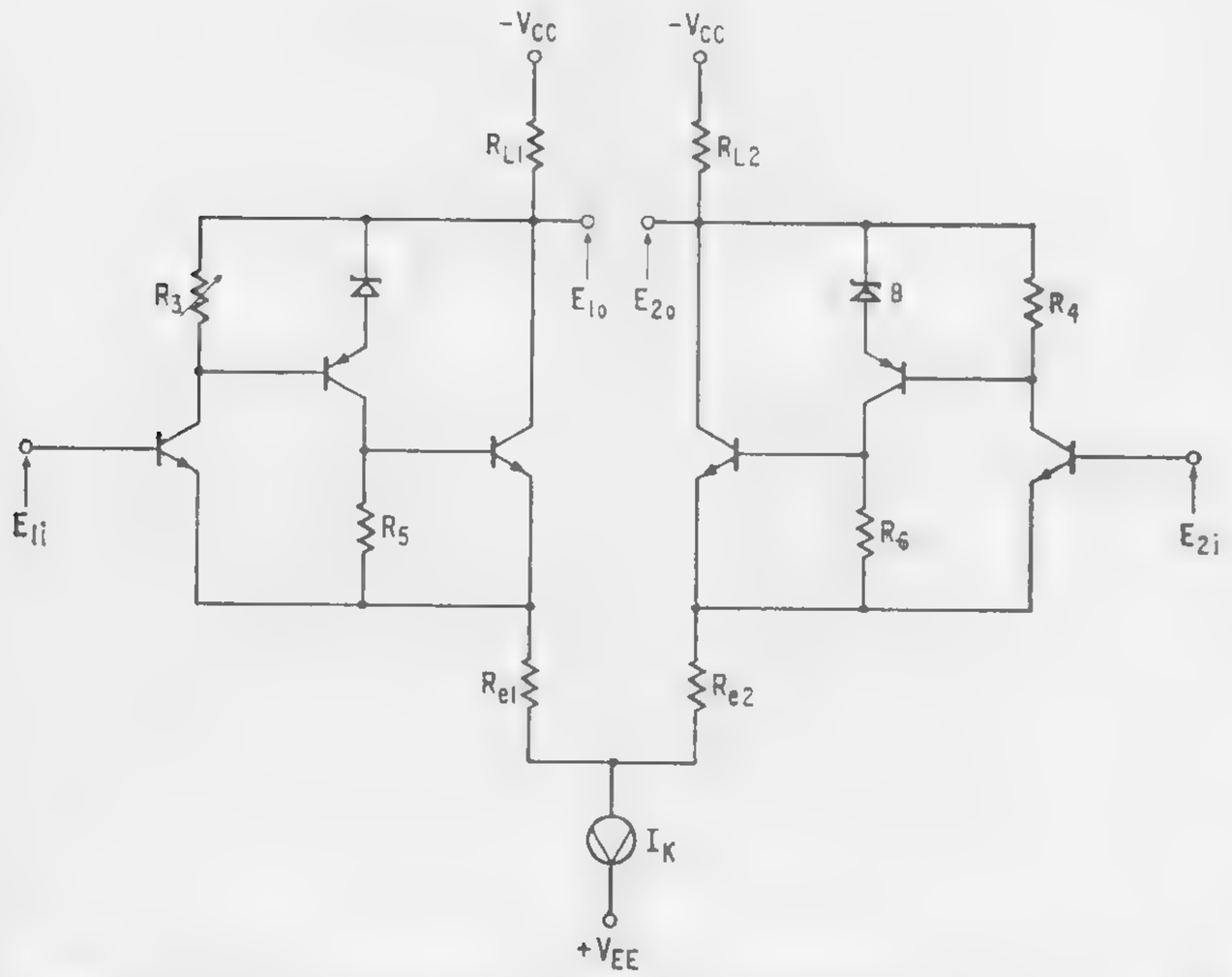



**Figure 5—An extension of the *pnp/npn* pair having a high gain stability.**

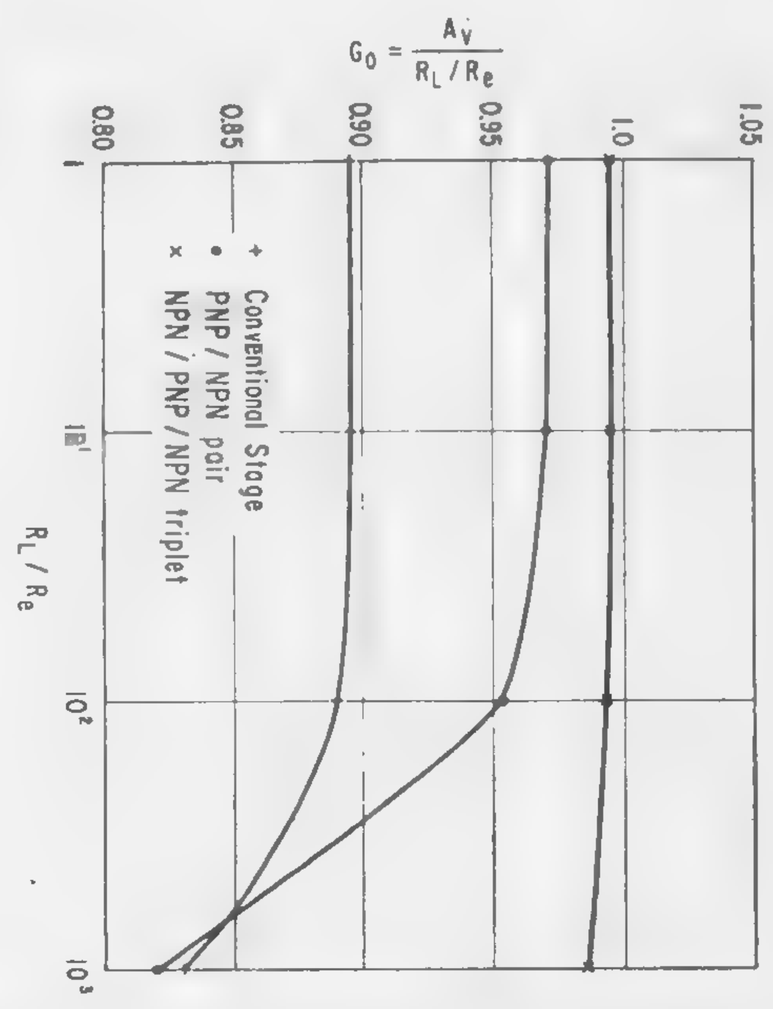



**Figure 6—The ratio of actual differential voltage gain to limit ($R_L/R_e$) with constant $R_e$.**

## SESSION IV: Power and Control

### 4.3: Improved Magnetic Voltage Stabilizer Employing Silicon-Controlled Rectifiers

**E. W. Manteuffel**

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Ithaca, N. Y.

CONVENTIONAL MAGNETIC VOLTAGE STABILIZERS[1] consist of a linear inductor connected in series with the parallel connection of a capacitor, saturable reactor and load. The reactor limits the flux-swing and operates as a switch reversing the capacitor charge at the end of each half-cycle. At these instances, high peak discharge currents flow through the reactor driving its core far into saturation. They cause considerable winding and core losses which are the main factor for its relatively large volume and weight.

This paper will describe an improved stabilizer illustrated in Figure 1. Inductor $L$ and capacitor $C$ are the same as in conventional stabilizers, while the heavy saturable reactor is replaced as follows: Capacitor $C$ is shunted by a small inductance $L_2$ in series with two parallel-connected controlled rectifiers $SCR_1$, $SCR_2$ of opposite polarity. Alternate firing of the controlled rectifiers is controlled by a small saturable reactor $SR$ of square loop material. This reactor is connected in series with resistors $R_1$, $R_2$ and in parallel with the controlled rectifiers. The physical size of reactor $SR$ is almost independent of the power rating of the stabilizer. Resistors $R_1$, $R_2$ have low ohmic value. They serve to bypass the magnetizing current of $SR$ in either direction during its nonsaturated state and permit alternate firing of the controlled rectifiers only at instances of saturation.

At these instances, the current through $R_1$-$SR$-$R_2$ will rise rapidly and, depending on its direction, either $SCR_1$ or $SCR_2$ will fire, cutting off further increase of current through $SR$. Capacitor $C$ then reverses its potential by discharging through $L_2$ within the time $t_d = \pi\sqrt{CL_2}$. This time can be made very small compared with the time of one half-cycle of the supply-line, since controlled rectifiers can conduct high current pulses at low duty cycle. After elapse of time $t_d$ the discharge current passes through zero and the respective $SCR$ ceases to conduct, thus permitting flux reversal of $SR$.

Controlled rectifiers exhibit a finite recovery time before returning to the blocking condition. Therefore, the discharge current may overshoot during this time in the reverse direction. At the instant of final interruption, energy will be stored in $L_2$, causing a relatively large voltage spike across the anode-cathode terminals of the controlled rectifiers. The amount of overshoot is dependent on the rate of change of current at zero crossover. The voltage spike may be reduced by a shunt resistor $R_S$ across $L_2$ or by a small capacitor $C_1$ and resistor $R_3$ across the controlled rectifiers.

A preferable solution is to make $L_2$ nonlinear such that its inductance at zero crossover is considerably larger than at peak current. Less energy will then be stored in $L_2$ and resistors $R_S$ or $R_3$ can be considerably increased in value thus reducing inherent losses of the circuit.

In many cases it is desirable for reasons of weight economy to operate $C$ at a larger voltage than the supply voltage. Also, the stabilizer output voltage may be required to be smaller or larger. A circuit permitting freedom of choice of both voltages is illustrated in Figure 2.

Experimental results obtained with a stabilizer having the following design data are presented in Figures 3-8.

Output voltage—200 *v* (avg.)
Output power—200 *w*
Input voltage—200 *v* ±20% (*rms*)
Frequency—420 *cps*

Output voltage regulation (Figure 3) was better than ±¼% with input voltage variations of ±20%. Voltage regulation over the range from no load to full load was 1.25%.

Data on efficiency and input power factor are shown in Figures 5 and 6. At rated load and output voltage, efficiency was 92.5% with a lagging power factor 0.9.

Typical output voltage wave shapes at different input voltages are shown in Figure 7. Single discharge current pulses for a linear inductor $L_2$ and a *Mo-Permalloy* powder core inductor are shown in Figure 8 which indicate a discharge time of only 40 microseconds. The very short discharge time helps to improve stability of the output voltage which depends mainly on variations of the volt-time integral during the transient with changes of input voltage.

Active components of the stabilizer weighed 1.9 pounds.

[1] Buchhold, T. A., and Stuhlinger, E., "Oscillating Circuit Incorporating a Choke with Rectangular Magnetization Curve," *Technical Report No.* 70, Redstone Arsenal, Huntsville, Alabama.

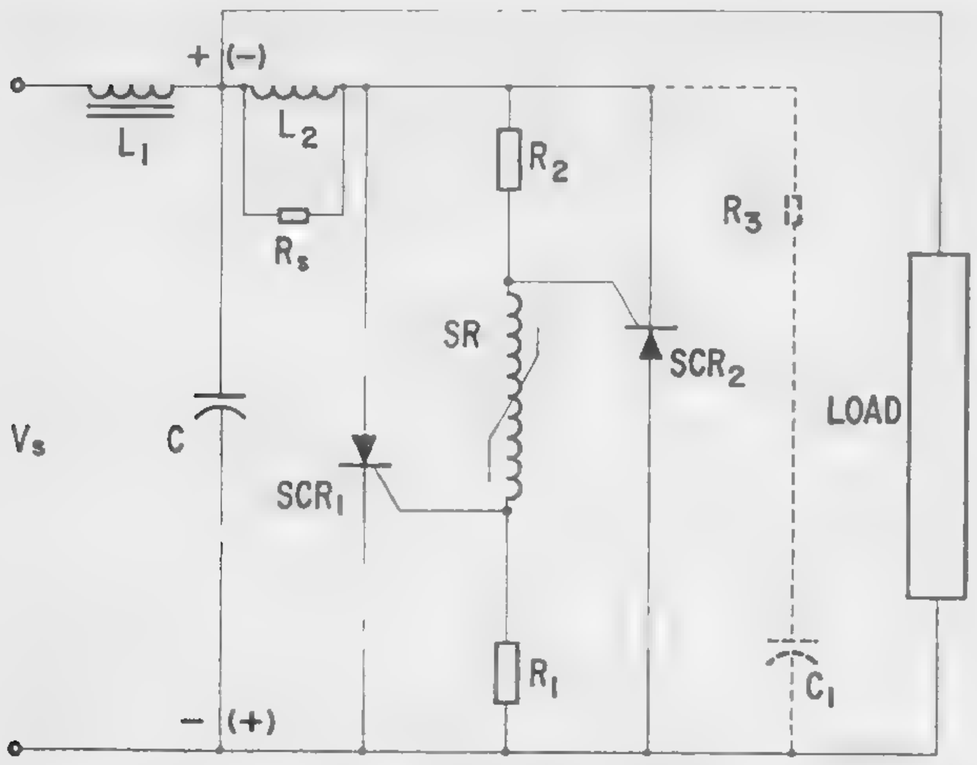



Figure 1—Circuit diagram of improved magnetic stabilizer.

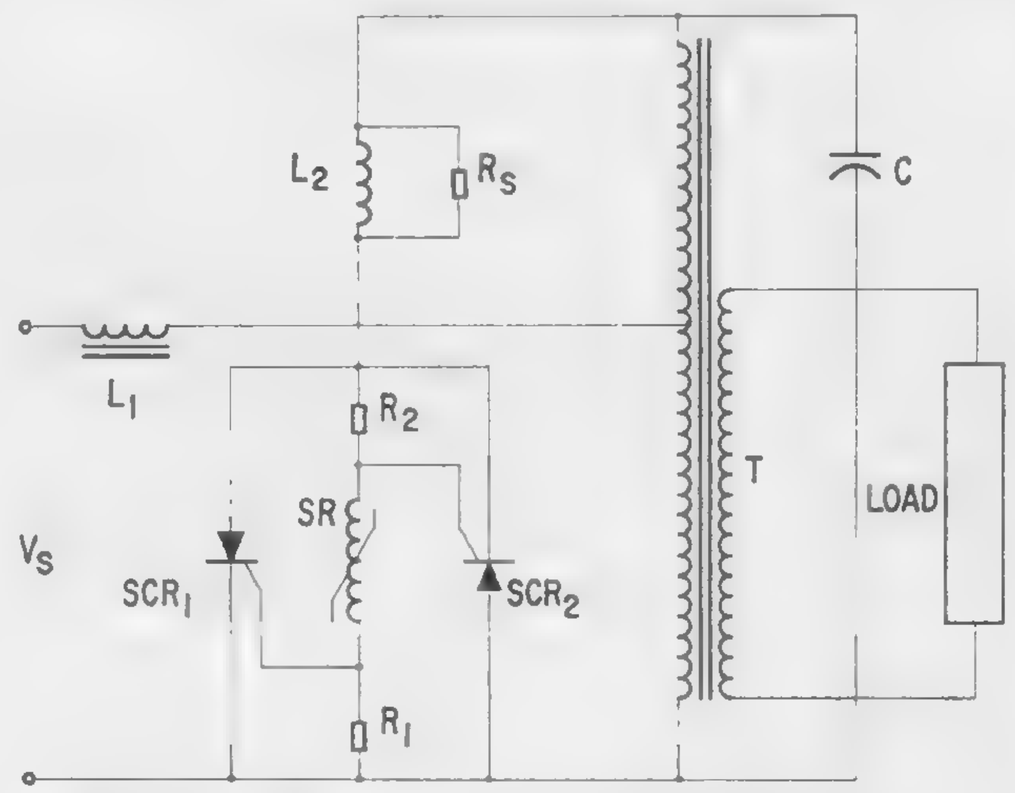



Figure 2—Modified circuit of improved magnetic stabilizer.

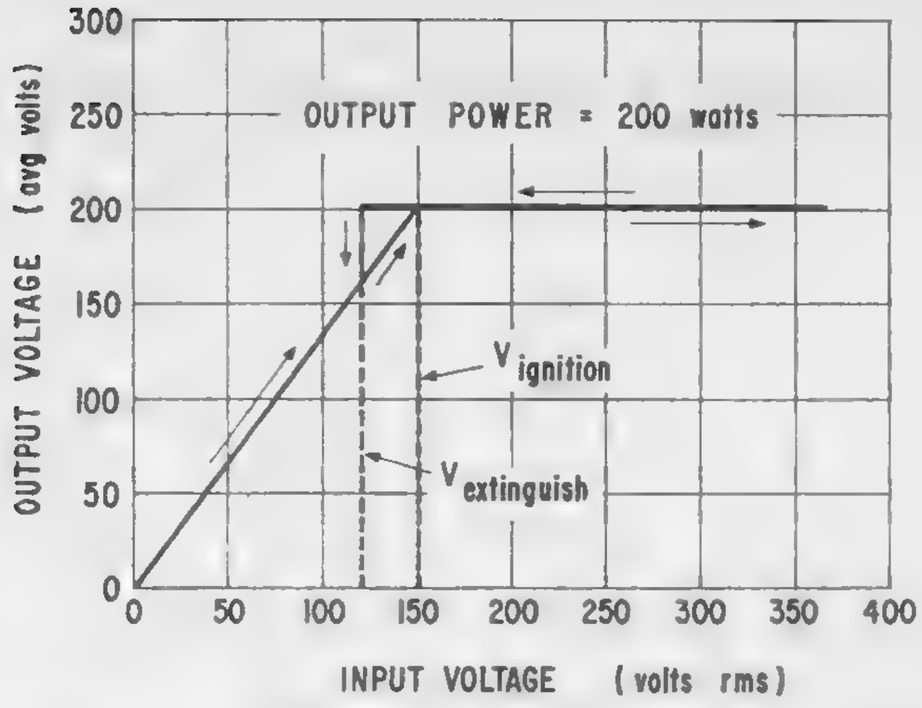



Figure 3—Operating characteristics of the voltage stabilizer.

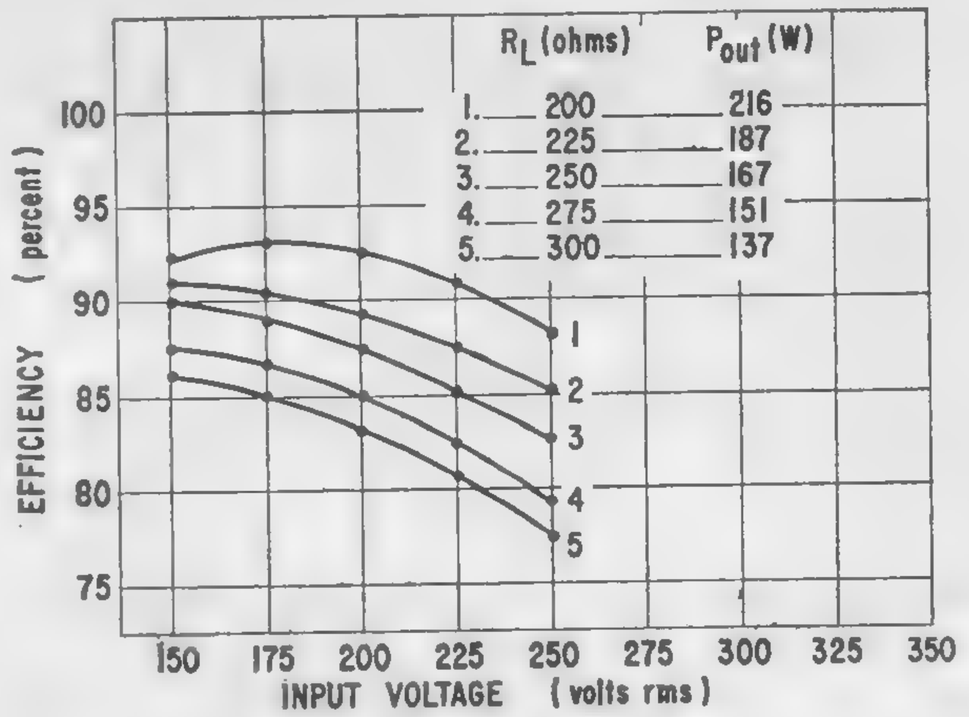



Figure 4—Efficiency versus input voltage at various loads.

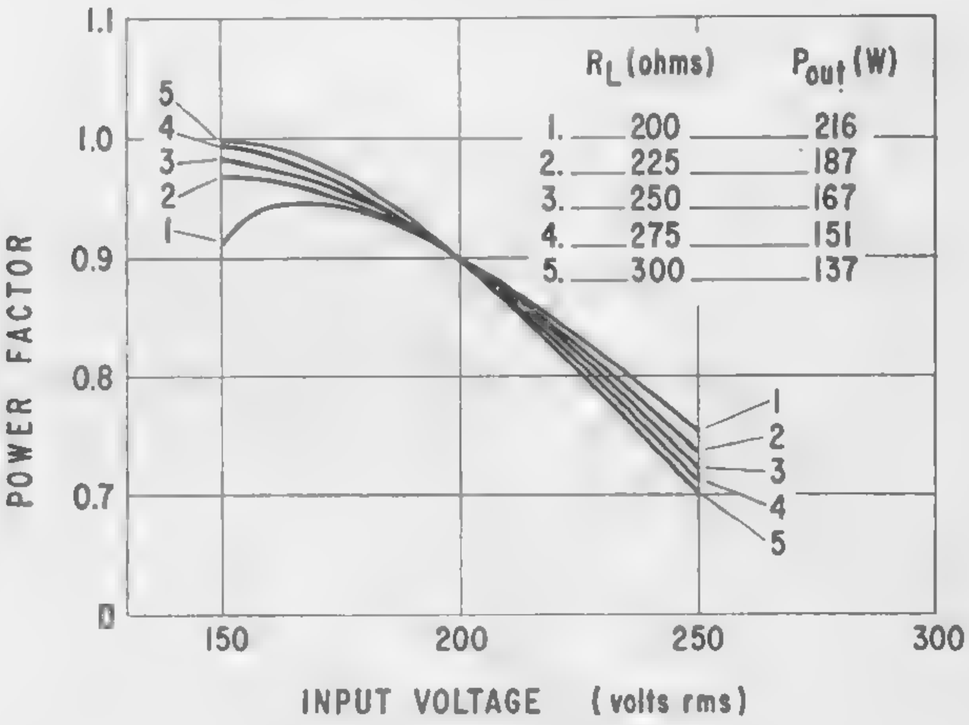
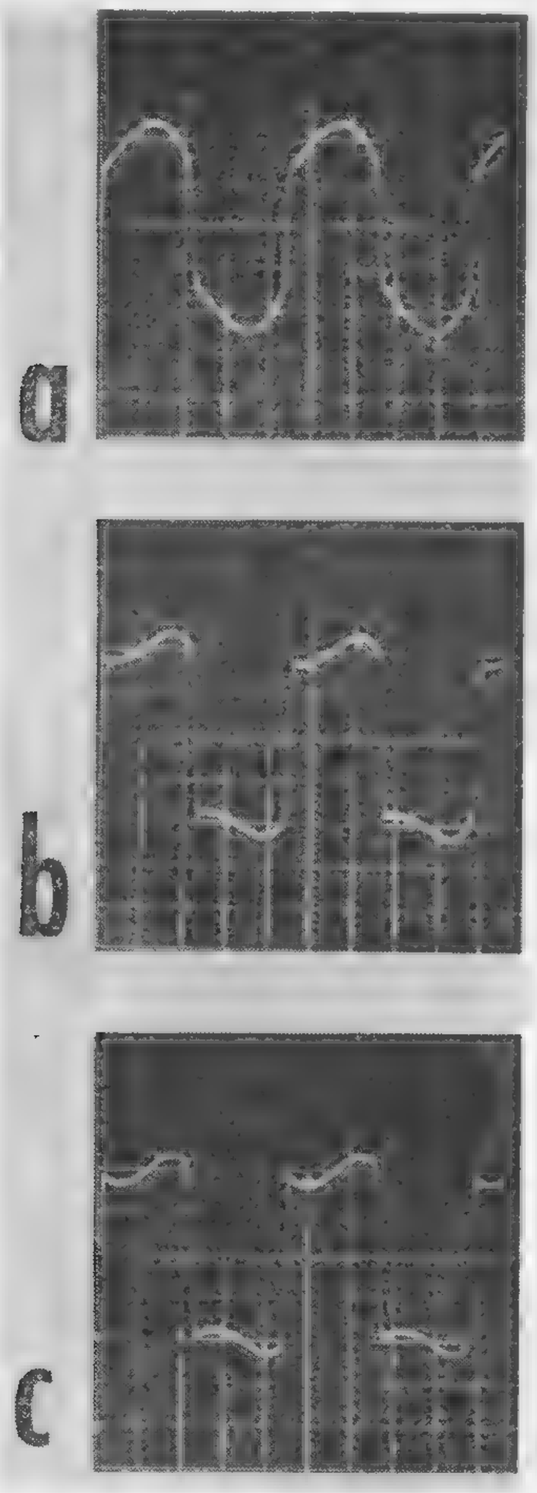



Figure 5—Power factor versus input voltage at various loads.




*(Left)*

Figure 7—Output voltage waveshapes at different input voltages. Waveforms: *(a)*—$V_s$ = 150 *v*; *(b)*—$V_s$ = 220 *v*; *(c)*—$V_s$ = 275 *v*. Scale factors—100 *v/div*; 500 *μsec/div*.

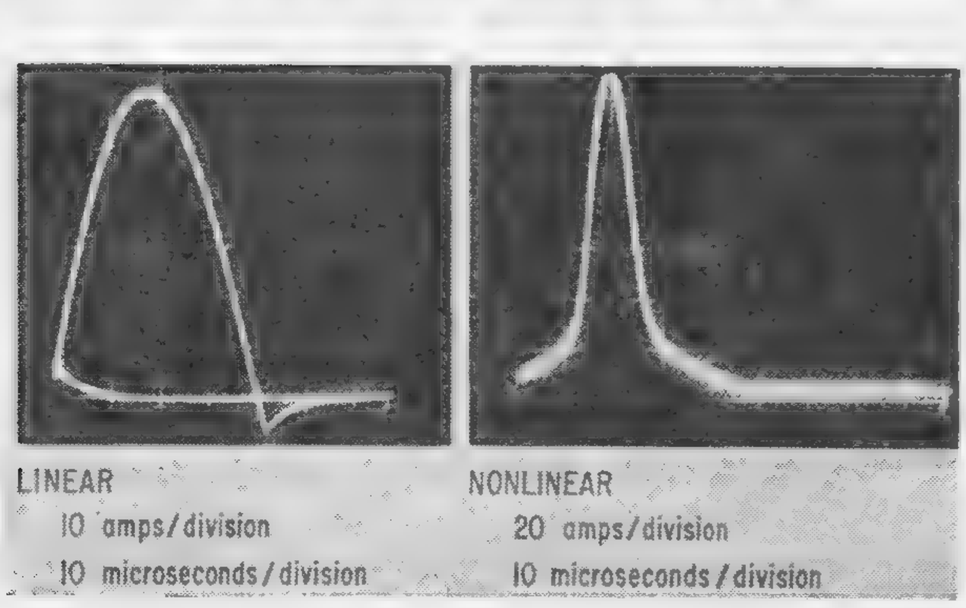



Figure 8—Discharge currents in inductor $L_2$.

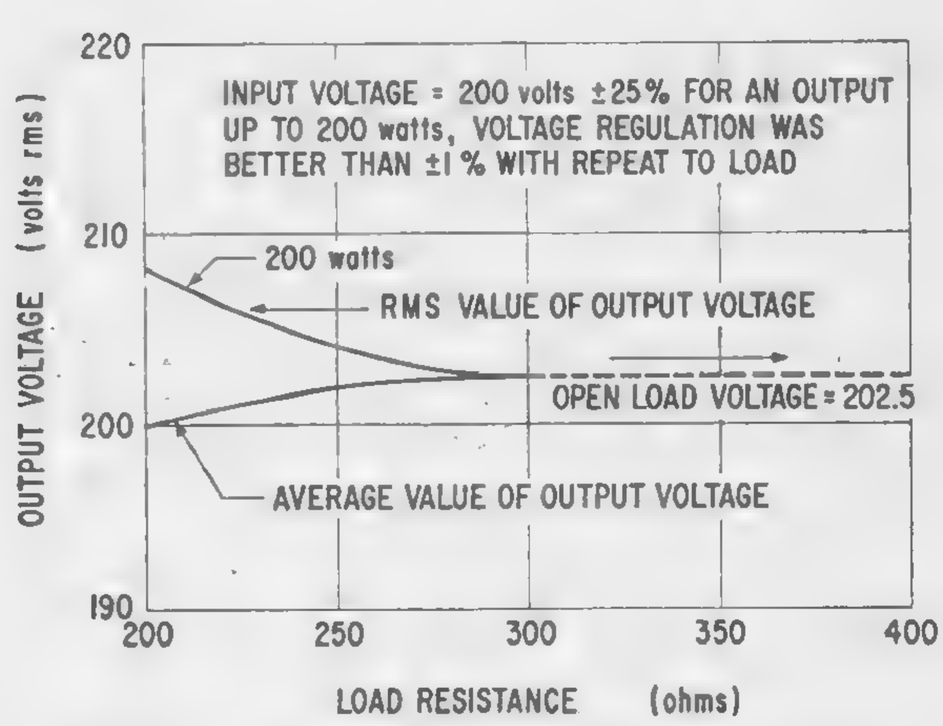



Figure 6—Output voltage versus load resistance.

## SESSION IV: Power and Control

### 4.4: A Control Circuit for PNPN Regulated Rectifiers

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THERE HAVE BEEN MANY profitable applications of *pnpn* switches. In particular, their use in high-power regulated rectifiers has been effective in achieving an improved efficiency. Many of the control methods used with these devices can complicate the problem of maintaining feedback loop stability in wide range precision regulator circuits. A schematic diagram of a full-wave *pnpn* regulated rectifier circuit with a double-base diode providing the control pulses appears in Figure 1. This diagram will serve to illustrate the stability problem for the steady state case. Figure 1 also shows the equation for the *dc* output voltage ($V_o$) and an expression $\frac{(dV_o)}{dV_f}$ for the portion of the steady state regulator loop gain which is due to the *pnpn* switches and double-base diode-control circuit. The latter expression indicates that the loop gain is, among other things, a function of the firing angle, $\theta$, and the line voltage. These equations are derived with the assumption that the capacitor voltage is approximately equal to the emitter-base one voltage, and the control voltage, $V_f$, is approximately equal to the interbase voltage, $V_{bb}$, on the double-base diode. A plot of gain as a function of firing angle with line voltage as a parameter is shown in Figure 2.

If a circuit of the type illustrated in Figure 1 must operate over a wide range of firing angles, it is clear that it will not perform equally well for all values of firing angle. A circuit of this type, which is designed for high performance while operating at low values of firing angle, may become unstable at higher values of firing angle due to the increase in loop gain. A solution to this problem is proposed with the circuit that appears in Figure 3.

In this circuit, the components $R$ and $C$ are used to form an integrator. That is, the $RC$ time constant is large with respect to the largest interval of interest. The output of the integrator is the voltage on the capacitor which, as before, is approximately equal to the emitter voltage of the double base diode. With the knowledge that the choke, $L$, is designed for continuous conduction of current, a path may be traced from the upper (or lower) side of the transformer secondary winding through the upper (or lower) diode connected to $R$, through $R$ and $C$, through the forward biased lower (or upper) *pnpn* switch back to the other side of the transformer secondary. This shows that the input to the $RC$ integrator is the secondary voltage of the input transformer. The circuit is self-synchronizing, because the input to the integrator is reduced to essentially zero by the fired *pnpn* switch until the beginning of the following half cycle of input voltage.

The equation for the *dc* output voltage ($V_o$) and an expression $\frac{(dV_o)}{dV_f}$ for the portion of the steady-state loop gain, which is attributed to the *pnpn* switches and double base diode control circuit, is also shown in Figure 3. Except for the line frequency, which may vary a few per cent, the latter expression is a constant. Therefore, so far as the *pnpn* switches and control circuit are concerned, stability or gain margin can be maintained over wide ranges of firing angle. Experimental measurements substantiate the theory very well.

An application of the circuit principle described is shown in Figure 4. The circuit shown is a three-phase rectifier; expressions for the *dc* output voltage and steady state loop gain are enumerated.

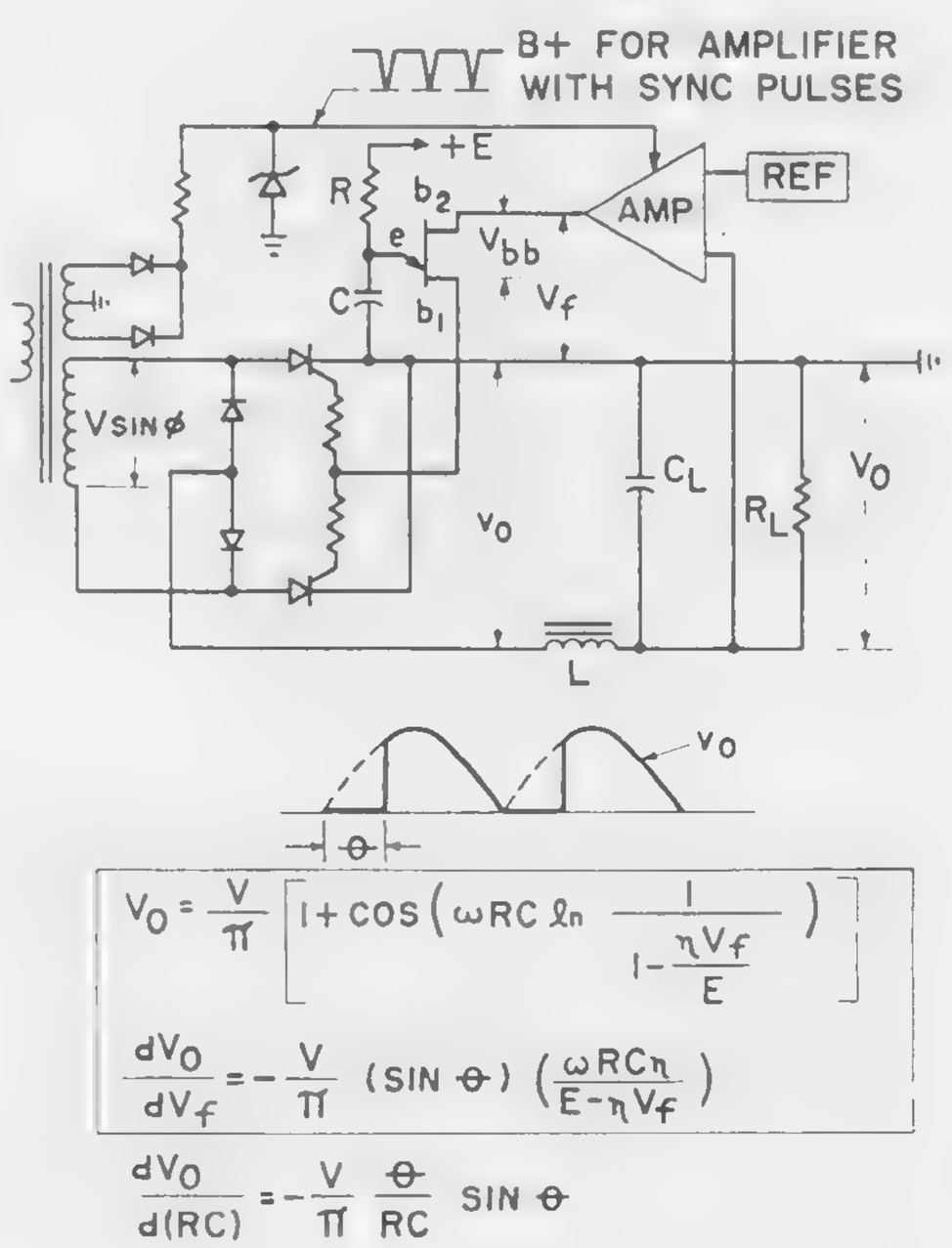



**Figure 1—Schematic diagram and equations for a single-phase *pnpn* regulated rectifier employing a double base diode for pulse control.**

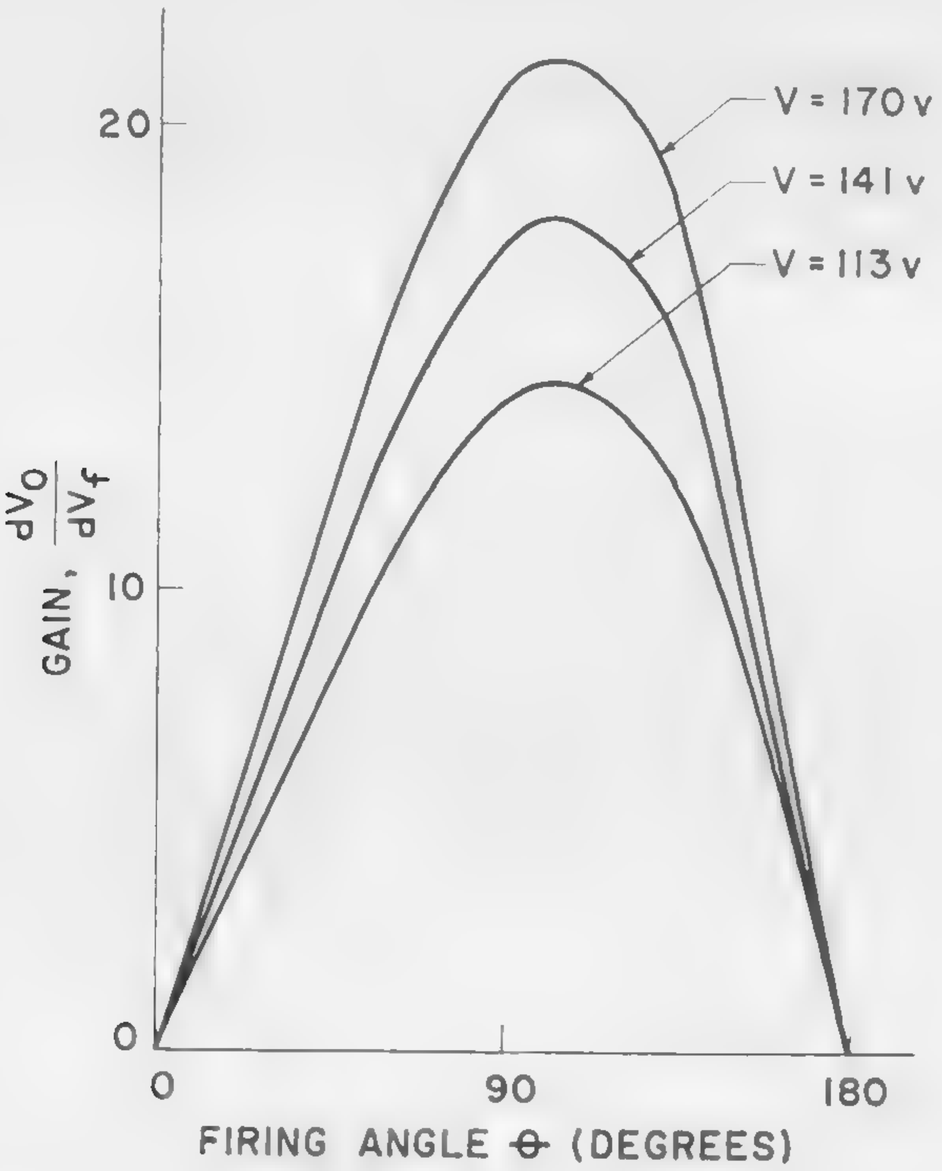
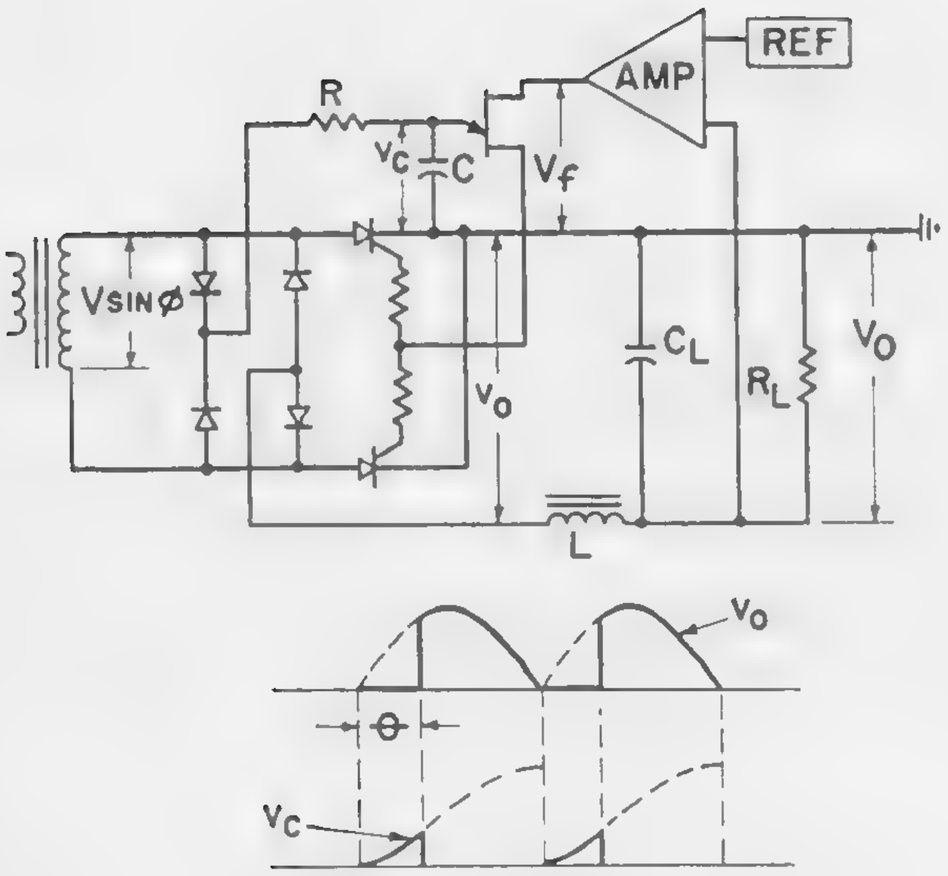


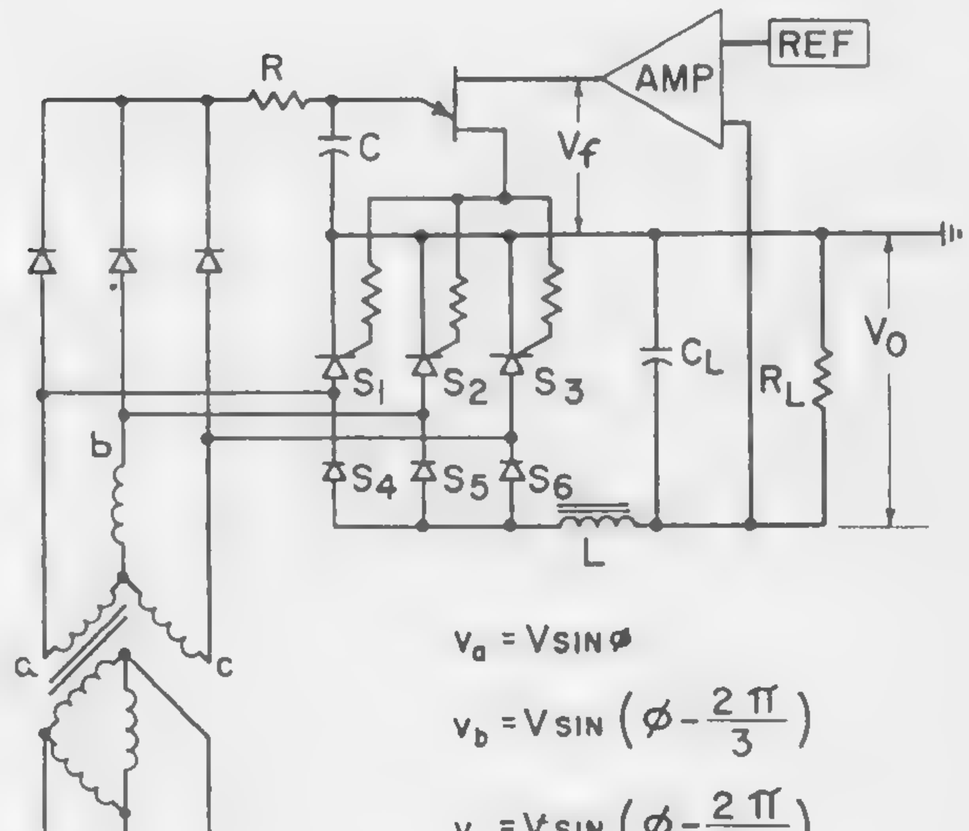

**Figure 2—Voltage gain versus firing angle for the circuit of Figure 1.**




$$V_O = \frac{V}{\pi}\left(2 - \frac{\eta\omega RC\,V_f}{V}\right)$$

$$\frac{dV_O}{dV_f} = -2\eta f RC, \quad f = \text{LINE FREQUENCY}$$

**Figure 3—Schematic diagram and equations for a single phase *pnpn* regulated rectifier with integrator control.**




$$V_O = \frac{3\sqrt{3}V}{2\pi}\left(2 - \frac{\eta\omega RC\,V_f}{\sqrt{3}V}\right)$$

$$\frac{dV_O}{dV_f} = -3\eta f RC$$

**Figure 4—Schematic diagram and equations for a three-phase *pnpn* regulated rectifier.**

## SESSION IV: Power and Control

### 4.5: Redundancy Techniques in Reliable Power Supply Design

**D. A. Paynter and V. P. Mathis**

Electronics Lab., General Electric Company

Syracuse, N. Y.

PRACTICALLY ALL MODERN military or industrial information handling systems include circuits that perform electronic signal processing. The power supplies for these processing stages are dependent also for their proper operation on the reliability of electronic devices and circuits; they occupy a critical position in overall system reliability. A component failure in the signal-processing channel need not necessarily be catastrophic to the system, but a power-supply failure may totally inactivate one or more of the signal circuits or a transducer.

Redundancy in power supply design may be applied at any of several levels. For example, an individual supply for each circuit could be employed, several identical general purpose supplies could be used, or one power source may be made more reliable by the inclusion of component and circuit redundancy within the single supply. The use of redundant elements is most efficiently applied at the level at which the probability of failure is greatest. In the present study it has been assumed that the semiconductor switches, an integral part of most power supplies, constitute one of the weakest links and these have, therefore, been singled out for attention.

### *Switch Redundancy Techniques*

*Moore* and *Shannon*[1] have noted that a single contact of the type shown in Figure 2*a* may be duplicated by networks such as those of Figure 2*b*-2*d*. Series parallel configurations, such as the elementary one of Figure 2*d*, can be designed to improve the probabilities of both opening and closure of the network as compared to an individual contact. Figure 3 illustrates the general type of probability function obtained with such networks. *Moore* and *Shannon* point out that the probability of closure for a given type of contact may not be equal to that for opening and their theory takes this into account.

It is seen that network 2*b* cannot increase the probability of closure, nor can 2*c* increase the probability of opening. The configuration of Figure 2*d* is a simple network that improves both probabilities and is somewhat more suited to improving the reliability of the *break* contact.

The failure of a transistor switch, used as a *contact* is not ordinarily reversible. The switch may fail to close completely on command due to a decrease in current amplification or, more normally, may fail completely to open due to an emitter-to-collect short. Once shorted it remains shorted. A series string of transistor switches such as an extension of 2*b*, would increase the *time to failure* of the overall contact to the time required for the *best* device in the string to fail by shorting. The network of 2*d* was actually selected for experimental investigation since it is helpful in combating both types of failure.

### *Experimental Circuits*[2]

The redundancy configuration of Figure 2*d* was incorporated in the circuits of Figures 4, 5, and 7 to demonstrate the operation and behavior of redundant connected transistors as switching devices. The experimental designs were computed using normal derating procedures. In addition, it was assumed that any individual transistor may be required to conduct full load current and withstand the total inverse circuit voltage during the converter lifetime. These conditions lead to a converter operating lifetime greater than would be expected from redundancy considerations alone. Under normal operating conditions and with no transistor failures, the individual transistor currents and voltages are half of the design values. This allowed for a significant additional derating factor. Figures 6 and 7 illustrate redundancy techniques as applied to a regulated converter in which the transistors operate in the linear mode as well as in the switching mode. The experimental results indicate that redundant techniques should prove useful in other linear applications.

The use of redundant semiconductor switches in converter-type power supplies and regulators is feasible in practical circuits. The concepts of *Moore* and *Shannon* may be extended and modified to predict mean time-to-failure for the redundant units. Since the individual switches are themselves quite reliable, a considerable improvement is obtained with only low redundancy. Quantitative statistical information is needed on the failure modes of the devices employed before an optimum redundant configuration can be designated. A significant additional advantage of redundancy on the device level is the reduced dissipation per switch due to the current and voltage load sharing aspect of the circuits used.

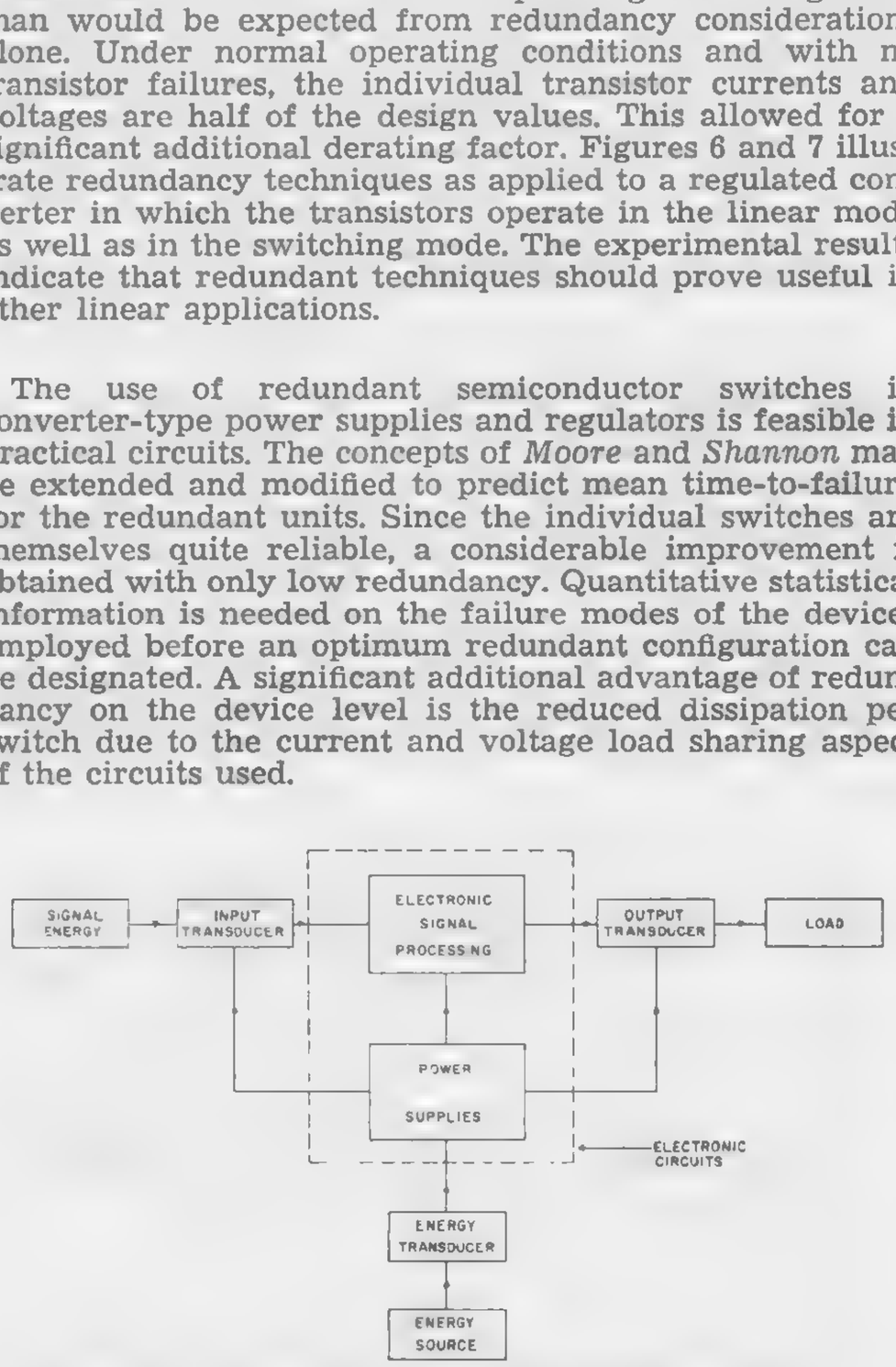



**Figure 1—General electronic system diagram.**

[1] Moore, E. F. and Shannon, C. E., "Reliable Circuits Using Less Reliable Relays," *Journal of the Franklin Institute;* Sept.-Oct., 1956.

[2] The authors wish to acknowledge the valuable contributions of *G. Jansen* in constructing and testing the experimental circuits.

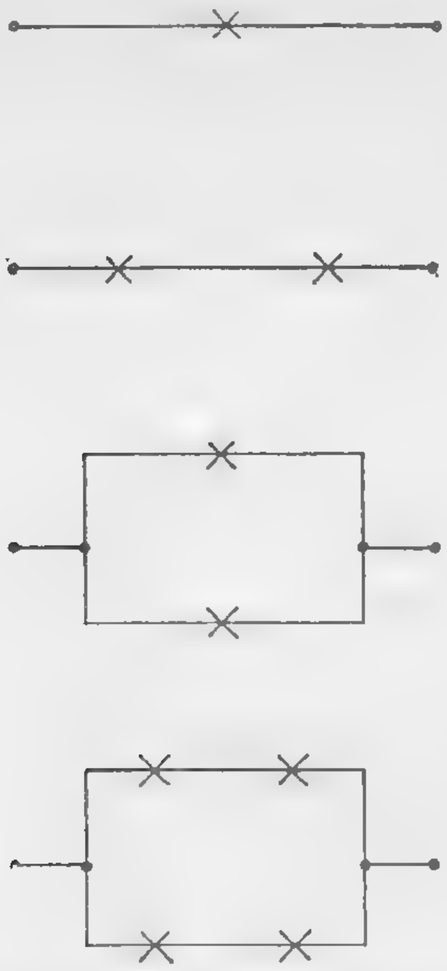



Figure 2—Redundant switch configurations.

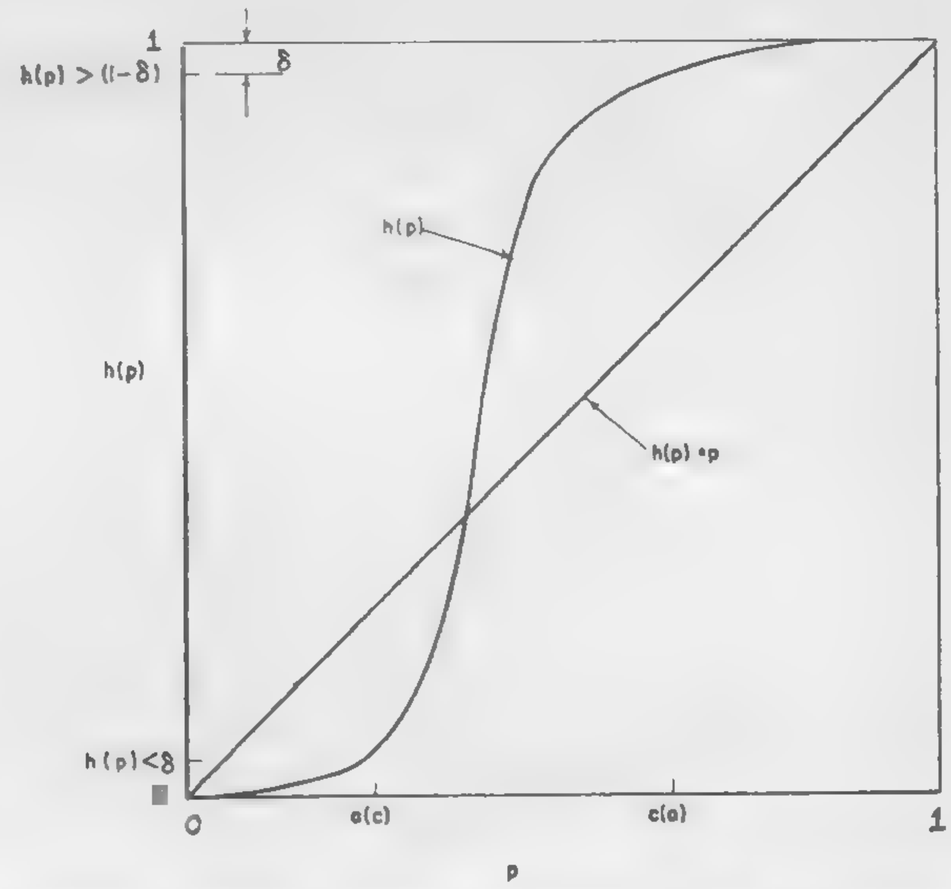
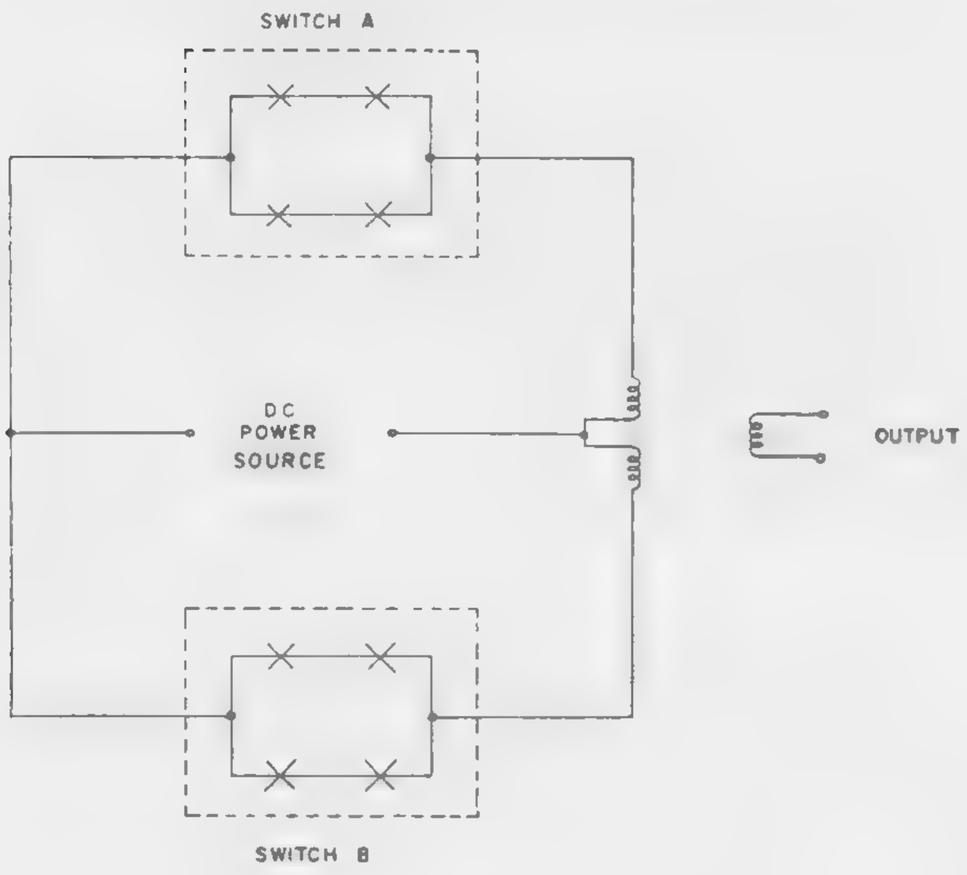



Figure 3—General curve illustrating type of probability function obtained using redundant contact networks (*Moore* and *Shannon*); *p* is the probability of operation of a single contact and $h(p)$ applies to the overall network.



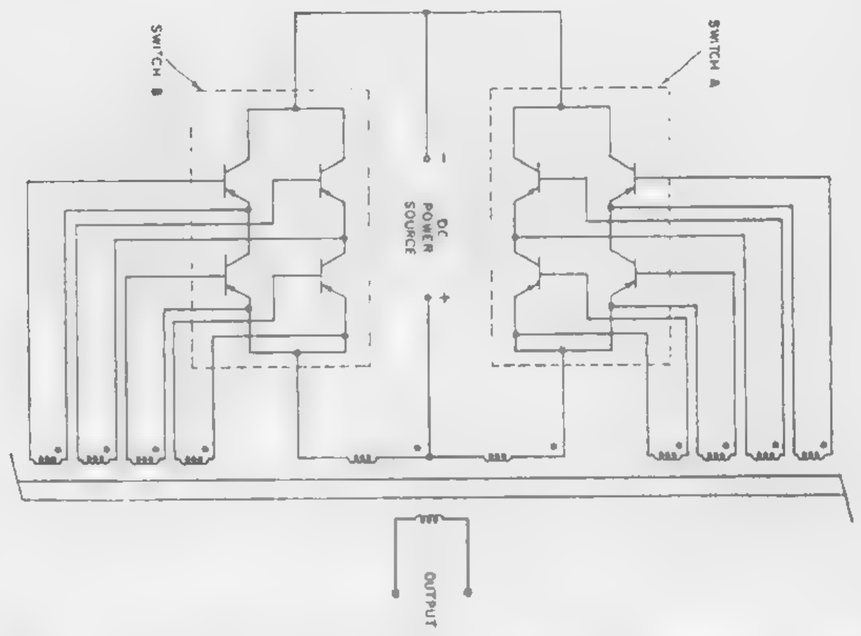




Figure 4 — *(left)* — Basic converter circuit showing redundant switch configurations in the positions of primary switches *A* and *B*.

Figure 5—*(above)*—Elementary converter employing redundant connected transistors in the Figure *2d* configuration. The multiple feedback windings may be considered to be a part of the redundant switches.

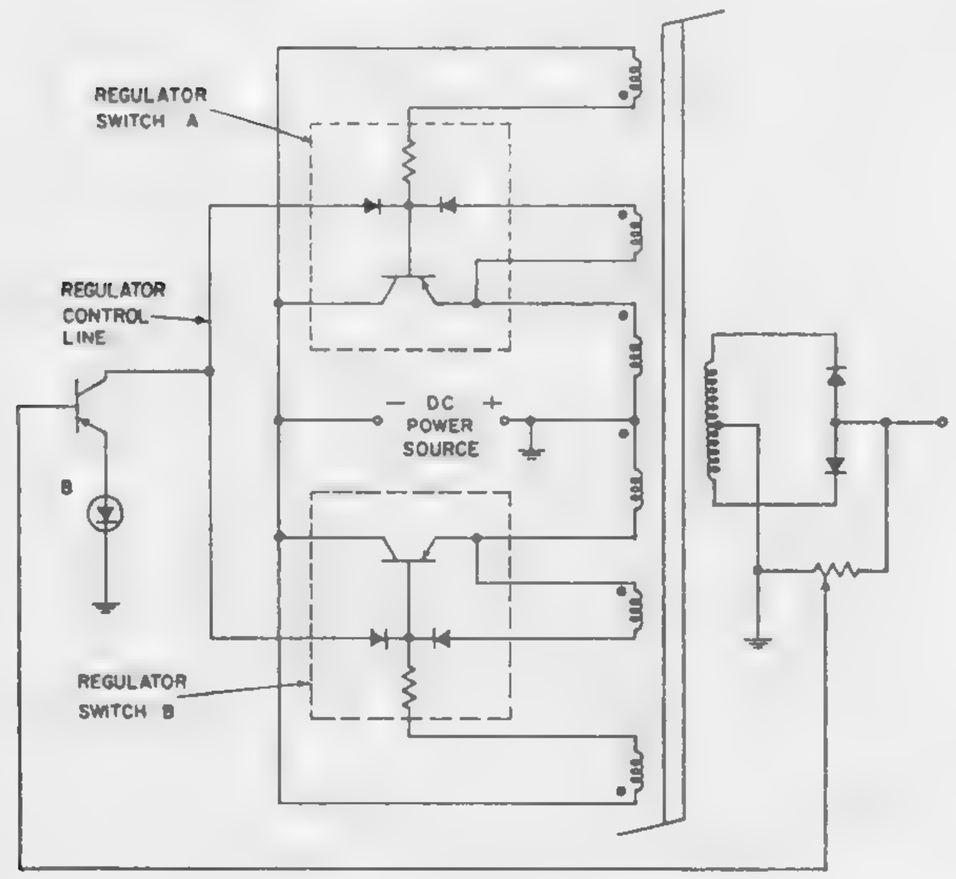



Figure 6—A regulated converter which employs transistors as combined linear and switching elements. Constant output voltage is provided by a compensating voltage drop across the converter regulator switches *A* and *B* which oppose output voltage deviations.

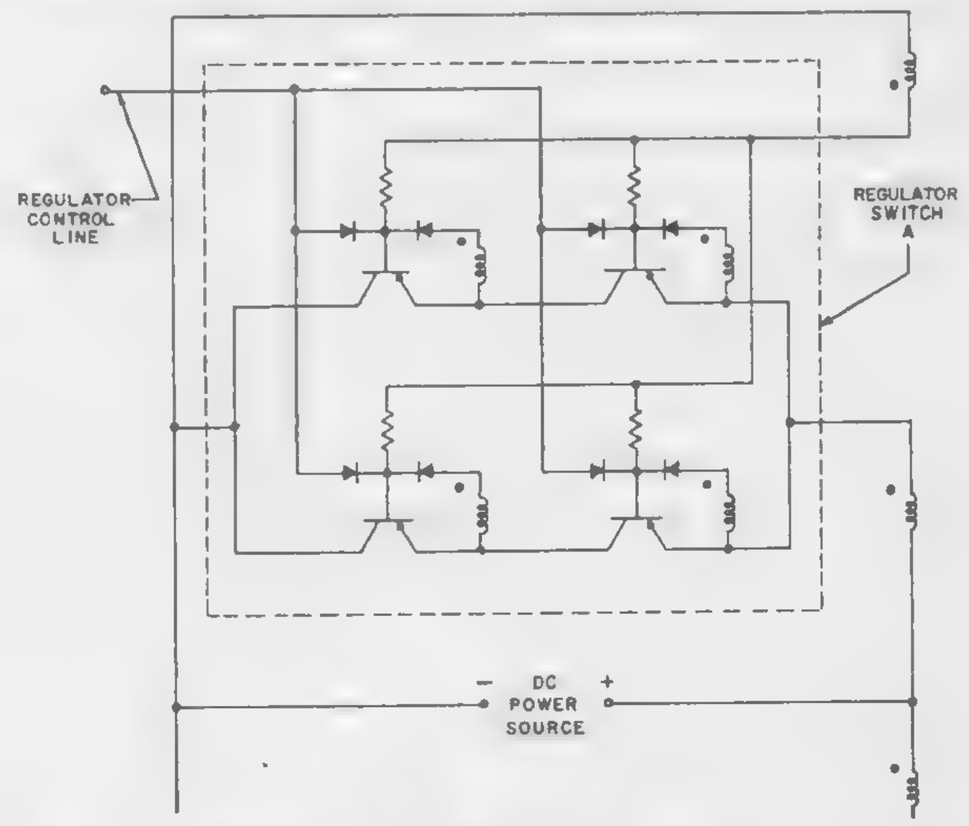



Figure 7—Detail of the Figure *2d* redundant configuration as applied to the regulated converter of Figure 6. Additional circuit elements are required to maximize the loadsharing aspect.

## Informal Discussion Sessions

### E.1: High Frequency Measurements and Characterization of Transistors *[Ballroom East]*

**Moderator: A. K. Rapp,** Philco Corp., Philadelphia, Pa.

**Panel Members:** M. M. McWhorter, Stanford University, Stanford, Calif.
R. P. Abraham, Texas Instruments, Inc., Dallas, Tex.
Y. C. Hwang, Electronics Lab., General Electric Co., Syracuse, N. Y.
V. R. Saari, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
V. H. Grinich, Fairchild Semiconductor Corp., Palo Alto, Calif.
E. J. Rymaszewski, IBM Corp., Poughkeepsie, N. Y.

### E.2: Microwave Applications *[Pennsylvania East/West]*

**Moderator: R. M. Ryder,** Bell Telephone Lab., Inc., Murray Hill, N. J.

**Panel Members:** E. Baldinger, University of Basel, Basel, Switzerland
F. R. Arams, Airborne Instrument Laboratories, Melville, N. Y.
B. C. DeLoach, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
J. H. Forster, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
M. E. Hines, Microwave Associates, Inc., Burlington, Mass.
K. K. N. Chang, RCA, Princeton, N. J.
E. Stern, Electronics Lab., General Electric Co., Syracuse, N. Y.

### E.3: Micro-Power Circuit Operation *[Delaware Valley]*

**Moderator: R. L. Trent,** Fairchild Semiconductor Corp., Mountain View, Calif.

**Panel Members:** R. H. Baker, MIT Lincoln Laboratories, Lexington, Mass.
R. A. Henie, IBM Corp., Poughkeepsie, N. Y.
R. Shultz, Fairchild Semiconductor Corp., Mountain View, Calif.
G. Saltus, Bell Telephone Laboratories, Inc., Whippany, N. J.
C. D. Simmons, Philco Corp., Lansdale, Pa.
R. D. Lohman, RCA, Somerville, N. J.

### E.4: New Logic Techniques *[Ballroom West]*

**Moderator: E. Stabler,** Electronics Lab., General Electric Co., Syracuse, N. Y.

**Panel Members:** G. B. B. Chaplin,* Plessey Co., Ltd., Hants, England
M. K. Haynes, IBM Corp., N. Y. C., N. Y.
J. A. O'Connell, IBM Corp., Poughkeepsie, N. Y.
S. Einhorn, Burroughs Corp., Paoli, Pa.
U. F. Gianola, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
M. H. Lewin, RCA Laboratories, Princeton, N. J.
E. Goto, University of Tokyo, Tokyo, Japan
W. W. Davis, Remington Rand Univac, St. Paul, Minn.
H. D. Crane, Stanford Research Institute, Menlo Park, Calif.

* Coauthor of following papers

**E.4/1: Wide-Tolerance Logic Circuits Using Tunnel Diodes in the Voltage Mode and Rectifier-Diode Coupling**

**E.4/2: A Fast-Word Organized Tunnel-Diode Memory Using Voltage-Mode Selection**

## E.5: Reliability

*[Constitution]*

**Moderator: B. T. Howard,** Bell Telephone Laboratories, Inc., New York, N. Y.

**Panel Members:** K. G. Ashar, IBM Corp., Poughkeepsie, N. Y.
R. R. Painter, RCA, Sommerville, N. J.
C. H. Zierdt, General Electric Co., Syracuse, N. Y.
E. R. Kretzmer, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
J. W. Tarzwell, Autonetics Div., North American Aviation, Inc., Downey, Calif.

## E.6: Power Conversion and Control

*[Independence]*

**Moderator: L. Bright,** Westinghouse Electric Corp., Cheswick, Pa.

**Panel Members:**
D. A. Paynter, Electronics Lab., General Electric Co., Syracuse, N. Y.
H. Storm, General Eng. Lab., General Electric Co., Schenectady, N. Y.
R. P. Putkovich, Westinghouse Electric Corp., Cheswick, Pa.
A. Walker, Westinghouse Mfg. Co., Ltd., London, England

*Notes*

## SESSION V: New Technologies

Chairman: J. M. Early

Bell Telephone Laboratories, Inc., Murray Hill, N. J.

### 5.1: Microminiaturization Developments

G. Moellenstedt and R. Speidel

University of Tübingen

Tübingen, West Germany

ELECTRON PROBES OF 200Å UNITS can be prepared by reducing an electron source. A collodion film 1000 Å units in thickness serves as the recording film. *H. Konig* has shown that it decomposes into carbon as a result of electron irradiation which entails a loss of mass and thickness; Figure 1. The track can be intensified by rotating oblique vaporization with platinum.

Figure 2 shows the movement of the micro-probe under the control of an electron microscope.* When the double condenser $K_1$ and $K_2$ (Figure 2) is switched on, a small aperture or a $4\,\mu$ diaphragm is inserted in place of the usual object. The dimensions of the small aperture are: $B = 1\mu$, $L = 100\mu$, $T = 2\mu$. The objective produces a 100-fold reduction of the $1\mu$-aperture. The collodion foil is stretched across the aperture diaphragm and placed in the beam path above the focal point of the objective. Electrons (60 *kev)* penetrate the thin foil so that the slit image can be clearly observed on the luminescent source despite the insulated foil. If the collodion foil is not precisely focused on the side of the image, then an additional silhouette is produced from the irradiated point on the foil. The 100-fold reduction of the aperture near the focal plane on the image side makes it possible to use the standard precision drives for shifting the aperture. A movement of the aperture in the objective plane by $1\,\mu$ results in a shift of the slit image on the foil by only 100 Å units. If a diaphragm is used instead of the aperture, then, with the aid of the objective drives, a better pattern several centimeters in size can be traced with the electron beam on the luminescent beam or in the intermediate image plane.

Figure 3 shows the resolving power of the electron micro-recorder. The total width of the area divided in lines amounts to about $1.5\,\mu$. The ten short lines in the center of the figure have a spacing of about 1000 Å units while the line width amounts to 140 Å units.

A $4\mu$ *Pt* diaphragm was incorporated in the objective plane. The electron beam is conducted to the luminescent screen along a template with an inscription. It has been found possible to store complete Bible data on 1/30 of the area of a postage stamp (3x2.5 cm) by means of electron micro-recording.

In the method described, writing is realized by shifting the aperture over the objective. However, in a recently designed device the gratings on the writing have been produced by shifting a rotation-symmetrical probe by means of a magnetic deflection element.

The collodion foil is also suitable for contact photographs of objects by means of electron, ion, *uv* and x-ray beams.

Reduction of [current] conductivity has been found possible through the use of polymuride films.

In this application a hydrocarbon polymuride film is primed as a surface in a vacuum of $10^{-4}$ *Torr* or irradiation with ion, electron, *uv* or x-ray beams. A silver film, as shown in Figure 5, is irradiated with a linear electron probe of 50 *kv* and $0.10\,\mu a$, 1000 Å units in width, as long as a polymuride deposit, 10 Å units in thickness is primed. This deposit is sufficient for preventing copper-growth in an electrolytic bath. The micro-aperture is obtained by pulling off the copper foil; Figure 5.

Preparation (and multiplication) of fine absorption gratings for super-orthicon image receivers, etc., have also been found practical.

If a fine absorption grating is available, the original is placed on a silver-coated glass plate (Figure 6) and exposed to ion radiation. A hydrocarbon polymuride is again primed; this reduces the conductivity of the silver coating to such an extent that no copper is primed in the electrolytic bath. A sharply traced copper grating is obtained after stripping which corresponds to the original.

A narrow ion beam produces a hydrocarbon polymuride strip on a copper film. The aperture can be shifted and moved vertically in relation to the first direction by a precision-movement-mechanism with interferometer control; Figure 7. If this copper film is exposed to chlorine gas, then all of the copper not protected by the polymuride is converted to copper chloride, and this can be dissolved in water.

Micro-resistances of copper, $1\mu$ in width, 1000 Å units in thickness, and 1 *mm* in length, with a resistance of $R = 300\ k\Omega$ can also be prepared in this manner.

Since *uv*-irradiation also produces polymuride deposits, reductions of an original can be produced in this manner with *uv*-objectives.

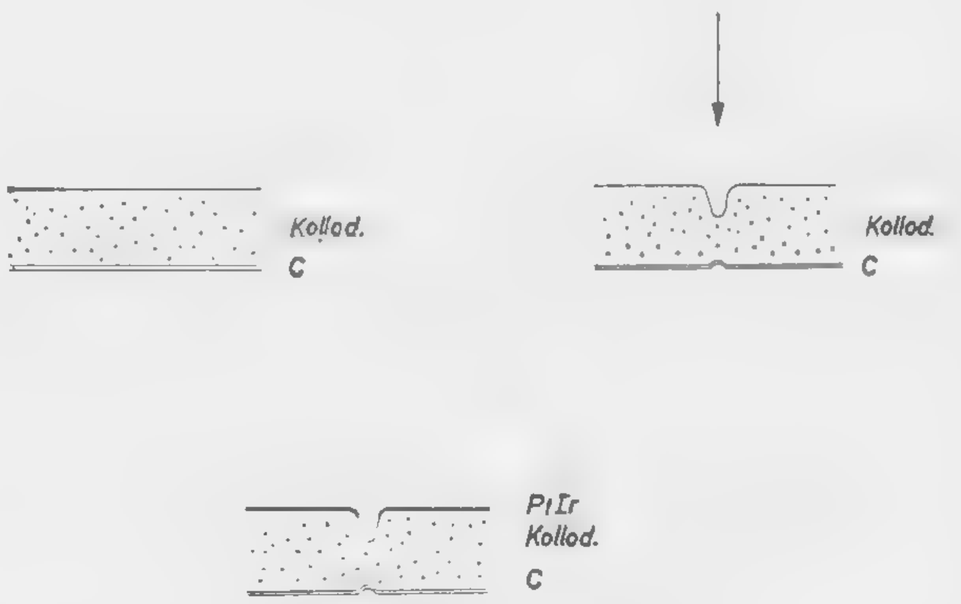



**Figure 1—High contrast visualization of electron track.**

* Elmiskop 1, Siemens and Halske.

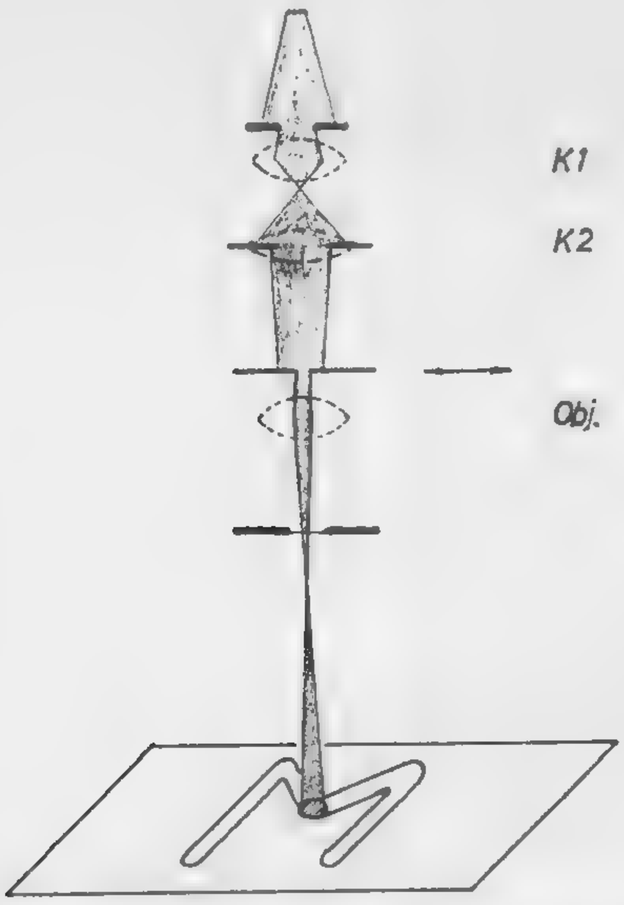



**Figure 2—Electron-optical beam path for producing and guiding the electron precision probe under electron-microscopic observation.**

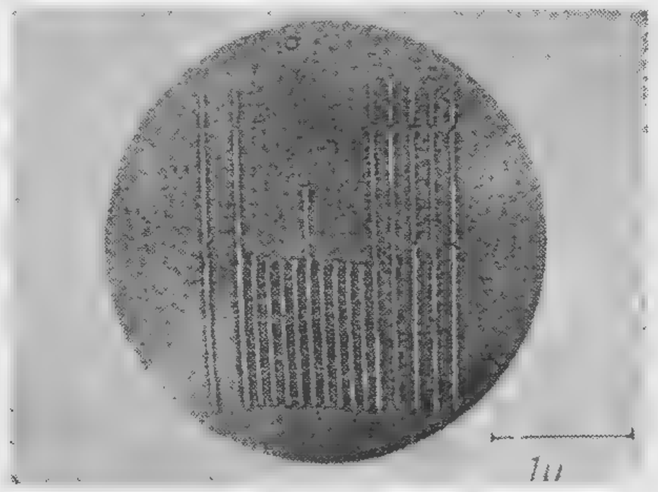



**Figure 3—A 25,000-fold electron microscope magnification of a stage micrometer for electron microscope.**


**Figure 4—Letters (0.5 µ) written on collodion foil with electron micro-recorder.**

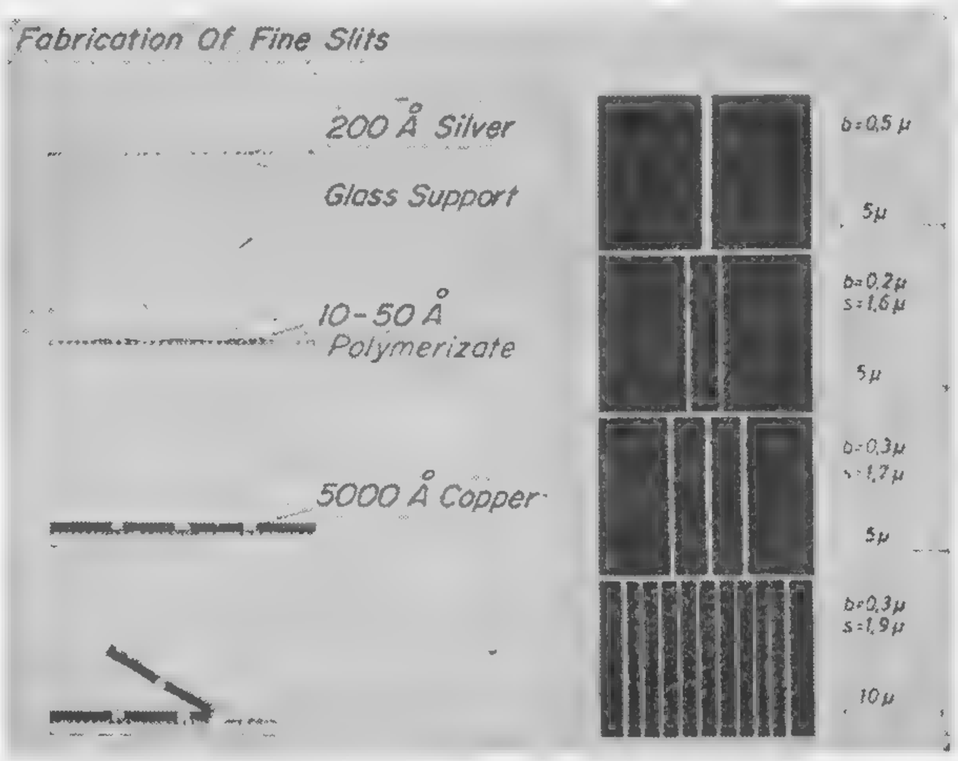



**Figure 5—Preparation of microapertures.**

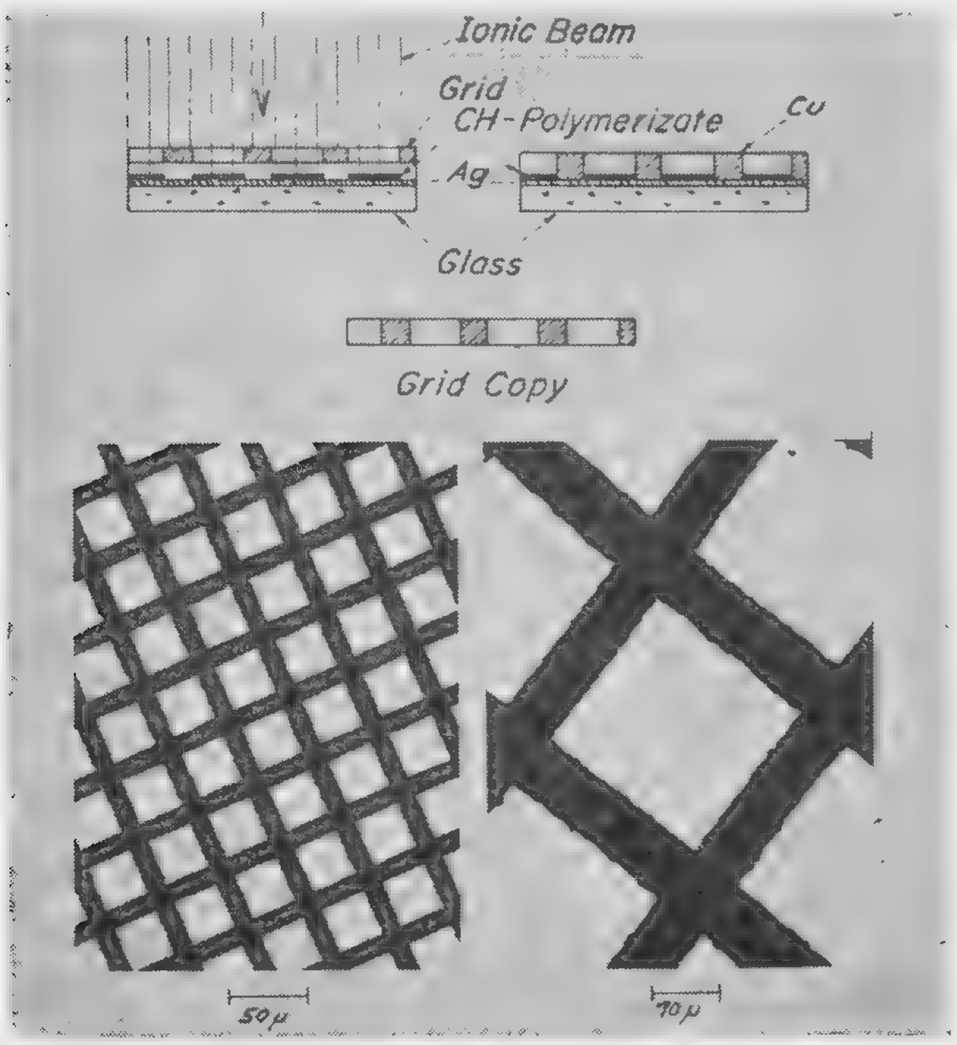



**Figure 6—Preparation of micro-gratings by the printing method.**

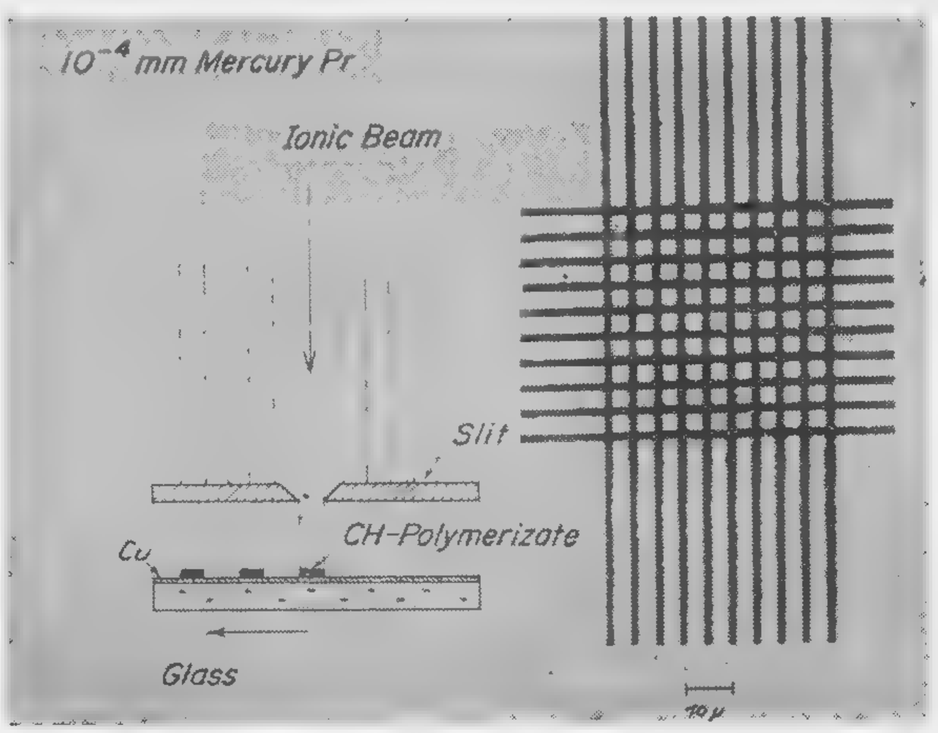



**Figure 7—Preparation of gratings with small mesh width.**

## SESSION V: New Technologies

### 5.2: Progress Report on Thin Film Circuitry

R. G. Counihan

Federal Systems Division, IBM Corporation

Kingston, N. Y.

MANY ORGANIZATIONS throughout the world are currently investigating the applications of thin films of various kinds to form the *RC* networks and interconnections necessary for producing electronic equipments. The principal motivation is the desire for higher reliability and lower costs. The speed and power improvements made possible by the compactness of film structures and the potential for size and weight reductions in operational equipment are simply not strong enough reasons to warrant the vast effort required to reduce to practice a new technology such as this. Most of the work reported to date has been aimed at proving the feasibility of film circuitry and interconnections. We are about at the close of this phase. Resistor and capacitor values adequate for over 90% of all military applications have been demonstrated, and working circuits representative of the audio, *if*, *rf*, and digital applications have been operated. We must now consider what else must be done before useful equipments can be designed and put to use employing these concepts.

A number of problems must be overcome before practical applications of thin film circuits techniques can be expected. These are:

*(a)* Stability under environmental stress must be proven.
*(b)* Satisfactory reproducibility and yield must be attained.
*(c)* The design-fabrication cycle time must be shortened to accommodate rapidly changing requirements.
*(d)* Quantities of semiconductor devices specifically designed for compatibility with film structures must be made available.

One of the factors that has received considerable publicity is the power dissipation-circuit density limitation. In practice it appears that this limitation will not be approached soon, due to practical considerations of interconnections and supporting structures plus the trend to lower power circuitry.

Stability of resistors, conductors and insulators is currently being evaluated under conditions of temperature, humidity, applied voltage, shock and vibration. Data obtained on various batches of elements tested up to 1,000 hours without hermetic sealing indicate that, as expected, a combination of high temperature, high humidity, and normal power dissipation is most detrimental. Environmental protection for film structures can be attacked at the device level, the circuit level, the sub-assembly level or the equipment level. Actually each of these is receiving consideration. Shock and vibration resistance is a function of the substrate and its mounting, and not a function of the films employed.

A careful choice of compatible materials, plus a detailed investigation into the fine structure of the film and the rates of diffusion of various materials in films, provide a basis for optimism concerning the ultimate reliability. The problems of reproducibility and yield are being attacked through the use of high definition masking techniques, and in process rate and thickness monitors incorporating feedback controls of the sources. Various means of trimming resistor and capacitor values are also feasible.

Design fabrication cycle time was originally measured in months due to the many steps involved and the requirement for checking at each step. As more experience has been gained in the layout of circuits and interconnections, and as knowledge of mask fabrication and registration techniques has improved, this time is now measured in weeks. This is still radically different from the rapid breadboarding which was possible in previous technology. It appears to be quite feasible, however, to automate further the cutting of artwork, or the punching or machining of masks. The actual fabrication time is principally limited by the rate at which substrate and sources can be heated and cooled inside a vacuum system. This, too, is undergoing study and improvement. The near term goal is to reduce the design fabrication cycle to not more than five days. In terms of procuring compatible semiconductor *chips* it is obvious from the intensive efforts throughout the country that the solution cannot be too far off. When this is achieved, it should be feasible to eliminate most, if not all, of the fine wire connections presently used.

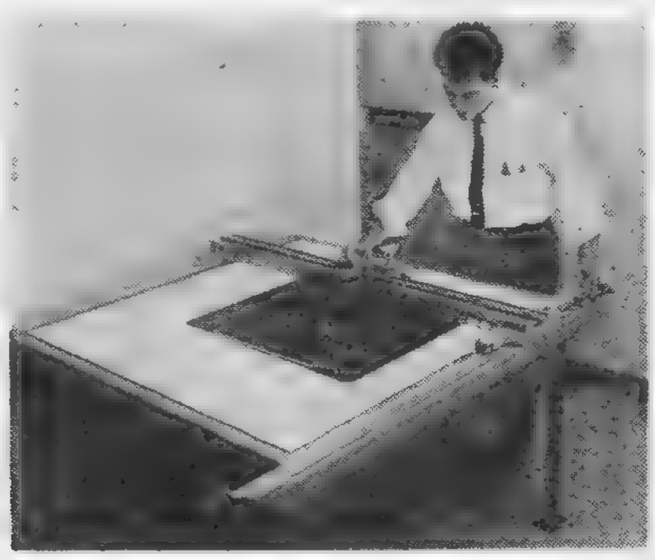


**Figure 1—Cutting mask artwork on ruby red plastic film with coordinatograph. Artwork is prepared 6 to 20 times size and goes through several photo reductions. Precision artwork is essential for good line definition.**

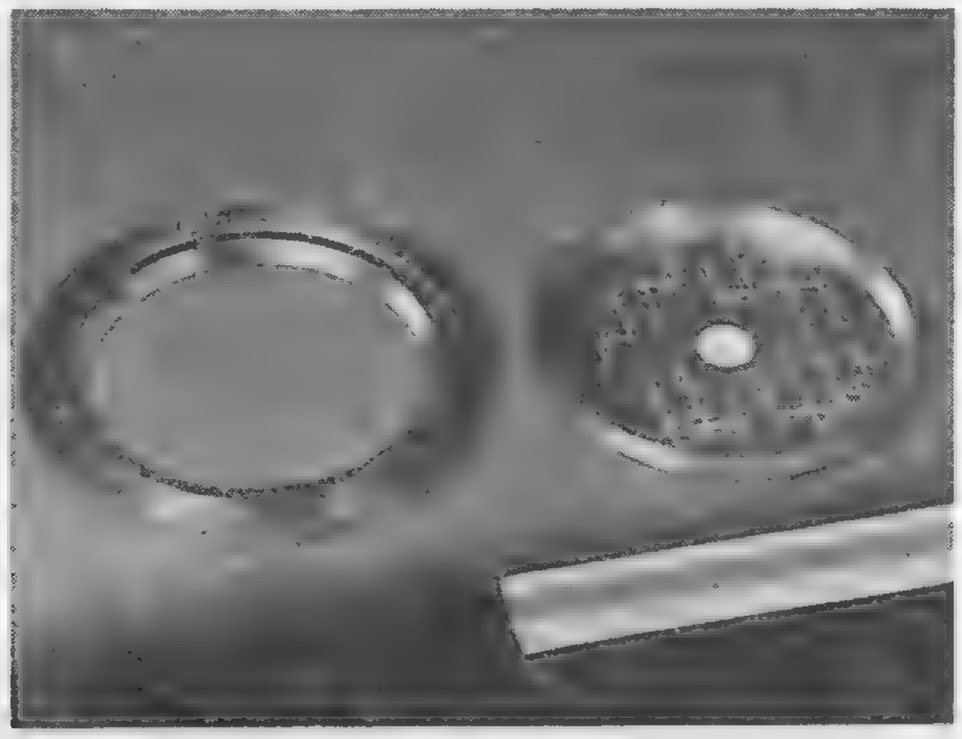
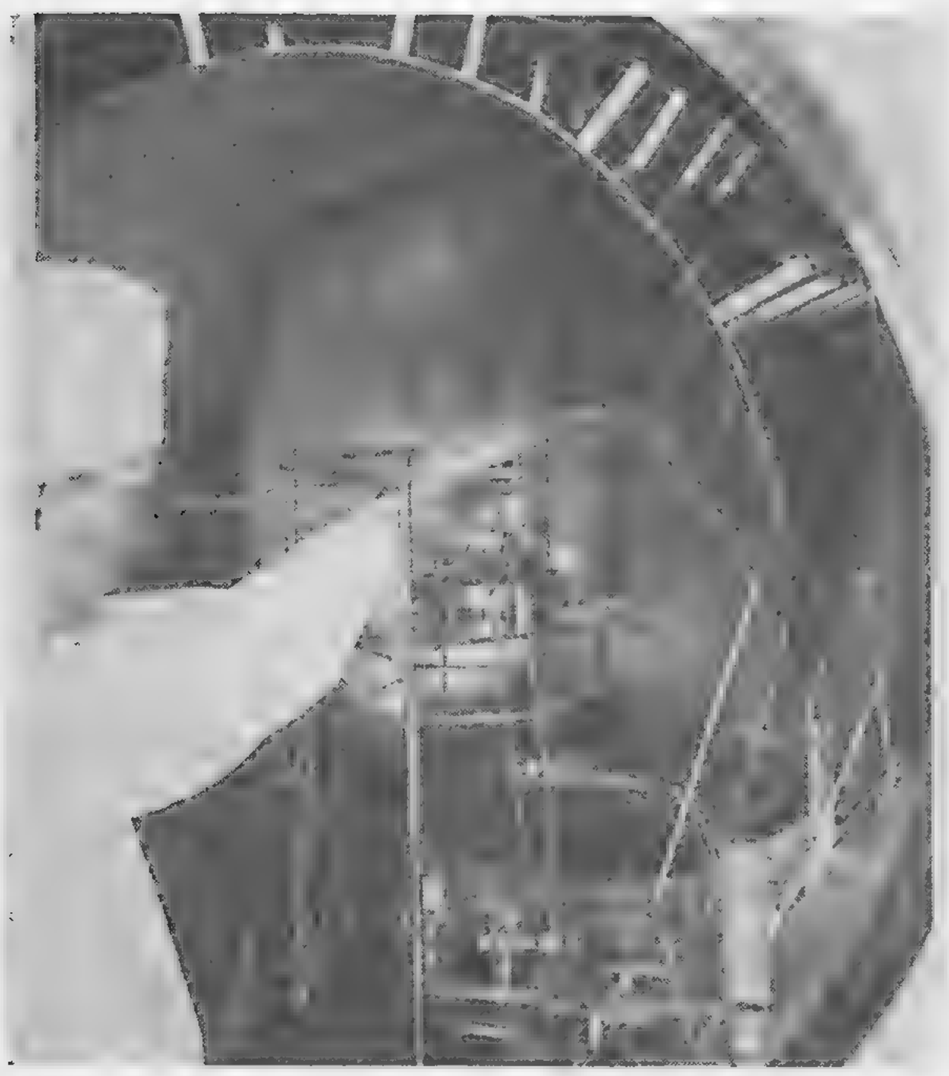


**Figure 2—Mask ring and holder assembly. Part on left shows the mask ring and holder assembly; at right is a mask ring with mask. This assembly allows for manual interchange of masks without disturbing the substrate.**



*(Above)*
**Figure 3—Internal view of vacuum chamber from clean-room side. Operator is making the final adjustment to the thermocouple location after mounting the substrate and mask holder assembly from the *clean-room* (controlled atmosphere lab) side of double-ended 36-inch tank vacuum chamber.**

*(Above)*
**Figure 4—Apparatus for automatic handling of multiple masks and sources within a single vacuum system.**

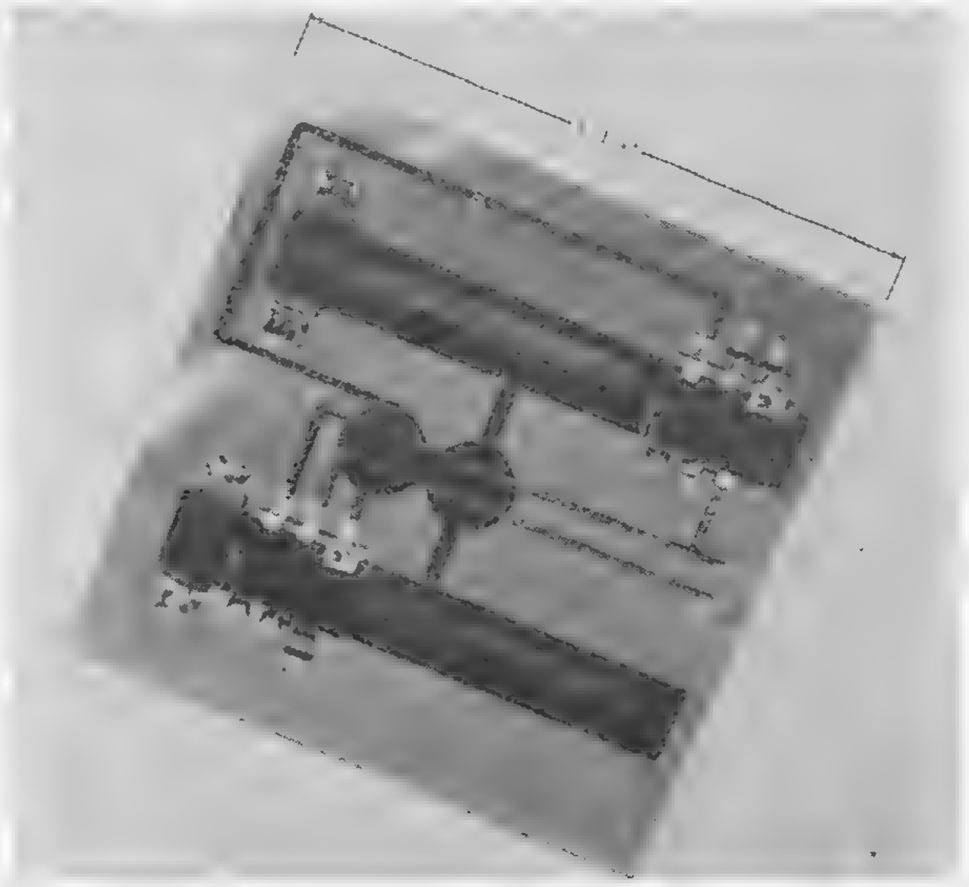


**Figure 5—A latch circuit; flip-flop consisting of two logic blocks containing resistors and transistors mounted on an interconnection plate containing power distribution and signal interconnection paths.**

## SESSION V: New Technologies

### 5.3: Investigation of a Thin-Film Thermal Transducer

J. G. Gottling

MIT

Cambridge, Mass.

THIS PAPER WILL PRESENT the performance characteristics and limitations of a thin-film thermal transducer operated as a signal-power amplifier. Results of an experimental verification of the theoretical study will be described.

The thermal transducer is a four-terminal, two-element electrical device which utilizes heat flow created by electrical power dissipated in an input resistor (heater) to control the resistance of an output element (sensor). Fabrication of this device in the form of thin, multilayer films by means of vacuum evaporation and deposition offers the possibility of small, high-speed units and can provide considerable reduction in its transient response time. Also, signal power gain is shown to be physically realizable. When operated with appropriate input and output circuits this device can perform mathematical analog operations of arithmetic (including multiplication), trigonometry, and calculus[1, 2, 3, 4].

An incremental analysis establishes the low-frequency and dynamic performance characteristics of the thermal transducer operated as a signal power amplifier.

For a slowly-varying incremental input signal the transducer can be represented by the incremental resistance model of Figure 2. In terms of this model, signal power gain is realizable within the bounds of stability[5] if certain conditions on the bias power are fulfilled. Figure 3 illustrates possible regions of gain and stability for two different sets of heater and sensor parameters. The largest maximum available power gain is given by the ratio of sensor to heater temperature coefficient of resistance ($\alpha_2/\alpha_1$) and occurs for combinations of bias power defining an operating point on the line separating the regions of stable and unstable operation.

An estimate of the dynamic performance of a planar thermal transducer is obtained by assuming the heat flow to be one-dimensional. The resulting dependance upon frequency of the maximum available power gain for a unilateral thermal transducer is shown in Figure 4. The bandwidth decreases as the sensor bias power is increased as a consequence of a self-heating, feedback effect at the sensor.

The product of the low-frequency maximum available power gain and the bandwidth is taken as a figure of merit for the thermal transducer. This gain-bandwidth product is

$$\beta_m \omega_b = \left(\frac{\alpha_2^2}{ck}\right)\left(\frac{P_1}{A}\right)\left(\frac{P_2}{A}\right)$$

where $A$ is the surface area of the thermal transducer. Limitations on this figure of merit, imposed by practical considerations as well as by physical and electrical properties of materials used to construct the transducer, are considered. These limiting features include: Allowable operating temperatures of materials, total bias power considered economically feasible, and dielectric breakdown strength of insulator materials. The transducer area is assumed to vary as the square of the chosen heat flow path length, $L$, so that at any thickness there will be no fringing of the heat flow path. Consequently, if the performance is limited by the operating temperature of the materials, the gain-bandwidth product varies inversely as the square of the heat flow path length. When the bias power limitation is applicable, the gain-bandwidth product varies inversely as the fourth power of the path length, but the dielectric limitation on the gain-bandwidth product is independent of the thickness.

#### *Construction Techniques*

A thin-film thermal transducer was constructed using vacuum deposition techniques to obtain metal, insulator, and semiconductor films. Such a transducer is shown in Figure 6; it consists of a nichrome heater film, a silicon monoxide insulator film, and a cadmium sulfide sensor film. The gain-bandwidth product of the experimental transducer is of the order of 1 radian per second. If a transducer were fabricated with the smallest area practical using the present technique (1 *mm* square), a gain-bandwidth product of the order of 30 radians per second could be achieved. Because the analysis shows that the gain-bandwidth product is inversely proportional to the transducer surface area over a certain range of values, a significant increase in this figure of merit depends on the development of new techniques for producing transducers having smaller surface area.

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[1] Savet, P. H., "Analog Computing by Heat Transfer," *Tele Tech*, p. 101-102; February, 1954.

[2] Davidson, F., "Thermal Elements Simplify Computing," *Electrical Manufacturing*, p. 86-88; June, 1954.

[3] Davidson, F., Djinis, W., and Savet, P., "Subminiature Thermal Computing Elements," *Electronic Equipment*, p. 16-19; June, 1955.

[4] Archer, G. R, "A Thermal Transducer for Application to Servomechanisms," *Master's Thesis*, Servomechanism Laboratory, MIT, Cambridge, Mass.; Aug. 22, 1955.

[5] Shekel, J., "Reciprocity Relations in Active 3-Terminal Elements," *Proc. of the IRE*, p. 1268-1270; August, 1954.

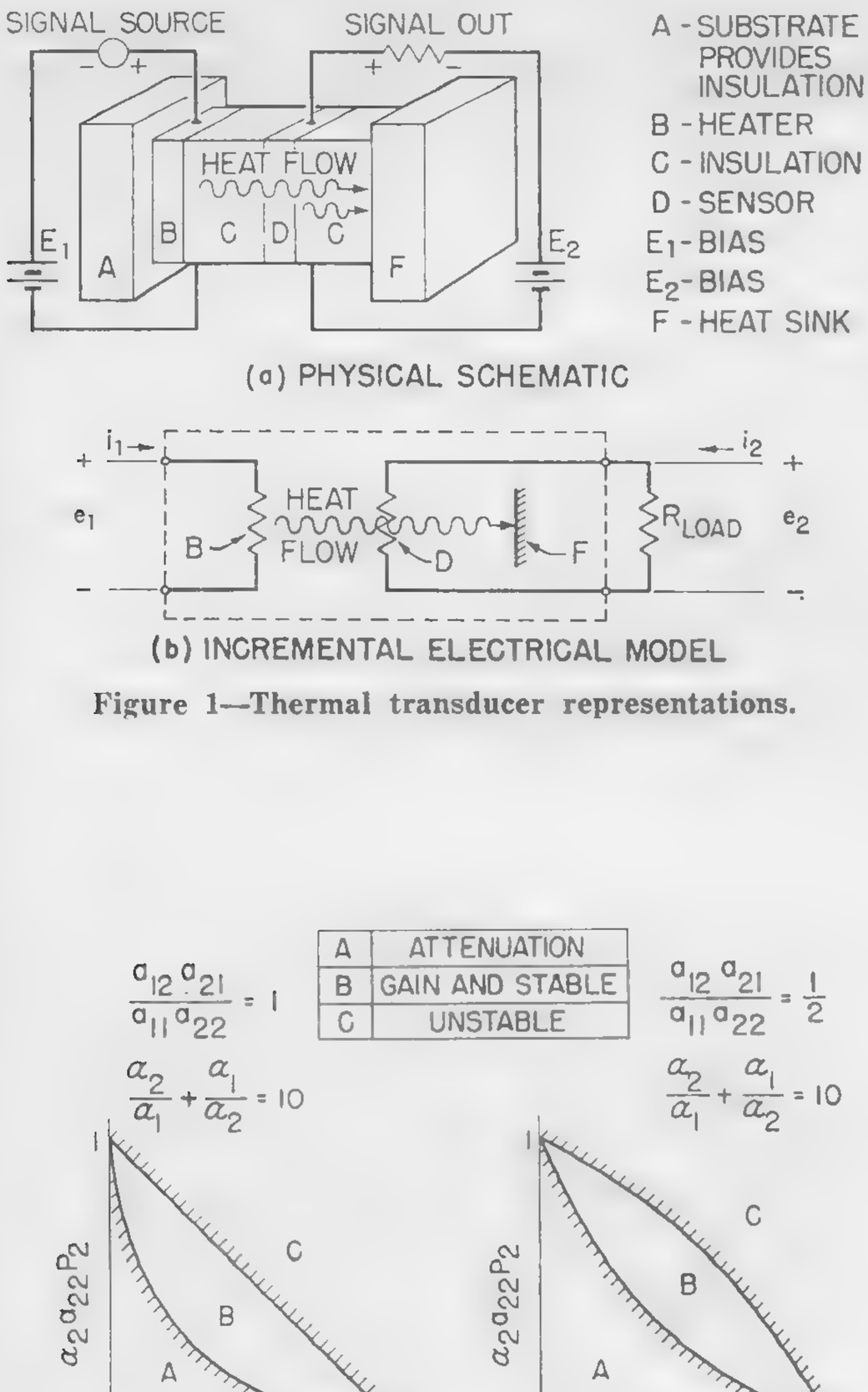


**Figure 1—Thermal transducer representations.**

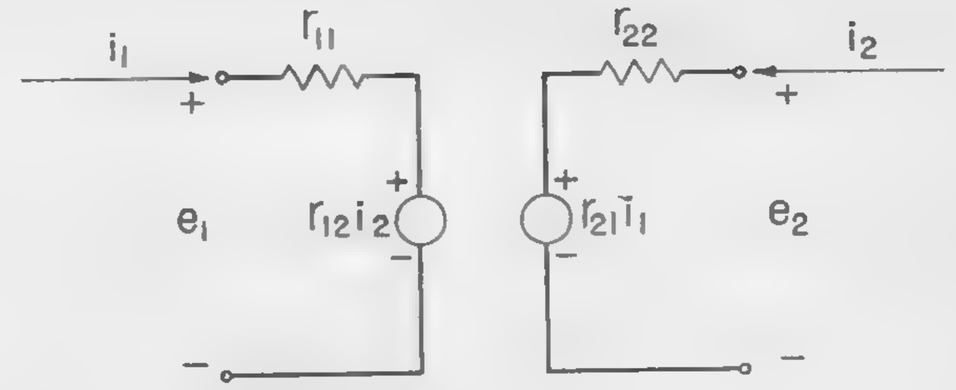


**Figure 2—Network representation of thermal transducer incremental relations. The thermal transducer is nonreciprocal when $r_{12}$ is not equal to $r_{21}$, as is the case when the heater and sensor temperature coefficients of resistance are unequal.**




**Figure 3—Typical gain and stability curves: $a_{nk}$ are thermal resistances in the linear expressions relating heater and sensor temperatures to their electrical power dissipation; $P_1$ and $P_2$ are heater and sensor bias powers.**

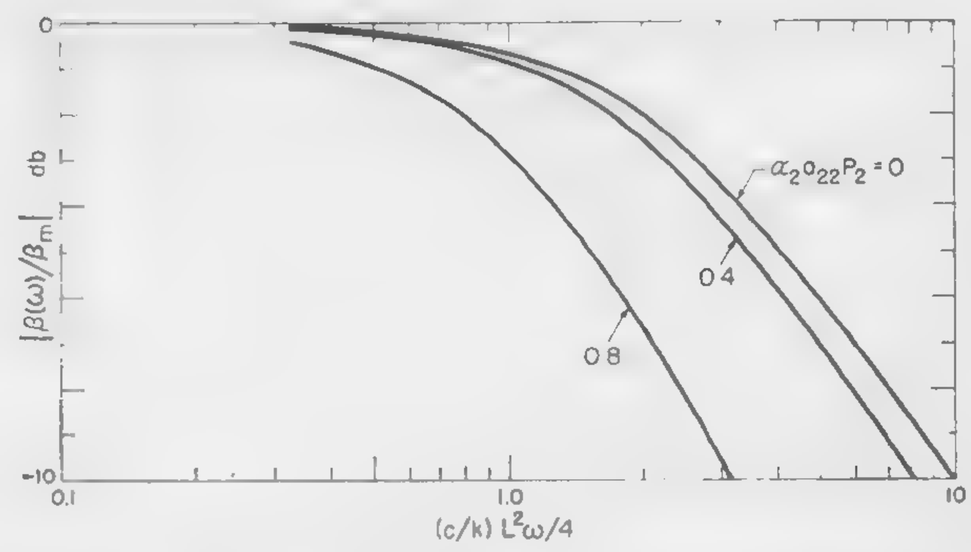


**Figure 4—Ratio of signal power gain to low-frequency maximum available power gain as a function of normalized angular frequency. The parameters $c$ and $k$ are specific heat and thermal conductivity of the heat-conducting media.**

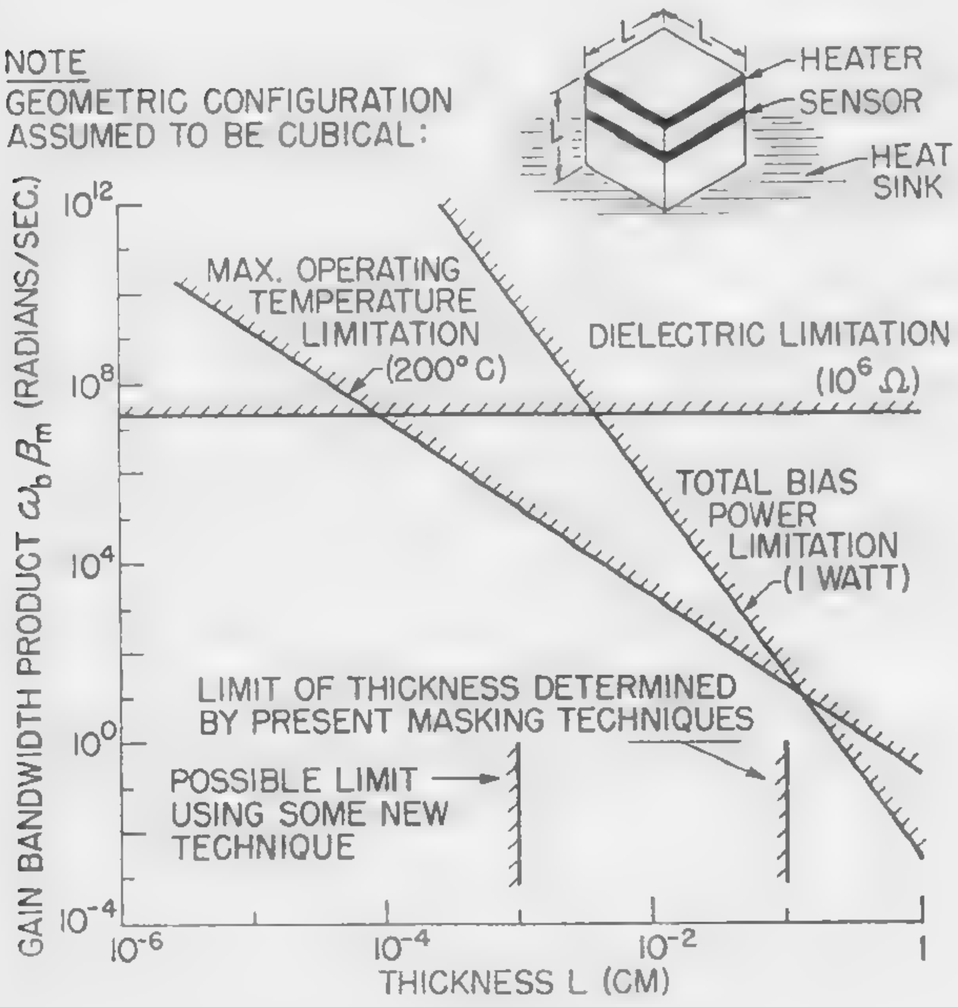


**Figure 5—Limitations affecting gain-bandwidth product.**

*(Left)*

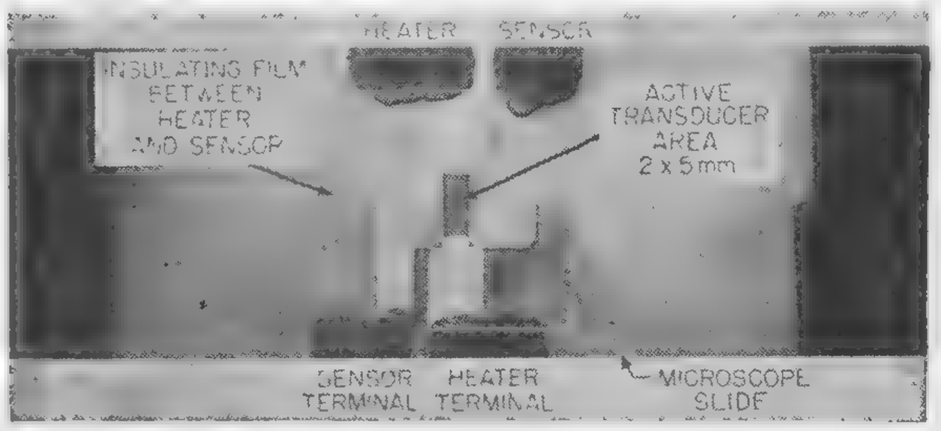


**Figure 6—Photograph of experimental thermal transducer. For operation transducer is mounted in a jig providing water-cooled heat sinks.**

*(Above)*

## SESSION V: New Technologies

### 5.4: Properties and Applications of Diffused Silicon Transistors Using Epitaxial Techniques

**W. B. Cagle*, H. J. Patterson and H. E. Talley**

Bell Telephone Laboratories, Inc.

* Whippany, N. J. and Allentown, Pa.

THIS PAPER WILL DISCUSS the electrical properties and possible circuit advantages of mesa-type *npνn* silicon transistors using epitaxially-grown material. Such transistors are constructed by conventional techniques of oxide masking and diffusion into a high-resistivity layer which has been epitaxially grown by vapor deposition on a low-resistivity substrate[1]. A cross-section sketch of a transistor of this type is shown in Figure 1.

Devices of this sort have many of the remarkable properties predicted for *npin* and *pnip* transistors by *Early*[2] several years ago. These derive primarily from the great device design freedom which is made possible by the presence of the *ν* layer. The addition of this layer to a transistor results in an increased collector breakdown voltage and lower collector capacitance, while at the same time allowing, through the use of a very low-resistivity substrate, low saturated $V_{CE}$ drops and low storage in the collector region. The simultaneous achievement of these properties provides transistors which are more nearly *universal* for both switching and linear circuit applications than were heretofore possible with diffused mesa transistors.

The properties of such transistors may, of course, be varied considerably by changing the epitaxial layer thickness and resistivity, the base width and sheet resistivity, carrier lifetime in the material, etc. The properties of one such class of units is shown in Figure 2, compared to similar but conventional switching and amplifier transistors. It is obvious that the epitaxial version has sufficiently good characteristics to be substituted for either unit and, hence, more nearly approaches being a *universal* type. The collector output characteristics of the conventional amplifier transistor and the epitaxial transistor are compared in Figure 3 to point out further the improved voltage characteristics of the epitaxial units.

For logic circuit applications, the low $V_{CE}$ drops and the parameters influencing switching speeds will be more important than the higher breakdown voltages. The lower $V_{CE}$ drops will increase noise margins and reduce the *dc* voltage shifting problems. Higher $F_T$, lower $C_{OB}$, and increased gain will improve rise and fall times. Devices optimized for such applications might be designed to trade breakdown for even higher frequency cutoffs by reducing base thickness. Also, some reduction in gain could be traded for lower storage times by using one of the standard methods of degrading carrier lifetime. Results obtained using gold diffusion for this purpose are shown in Figure 4. These curves illustrate how the storage time of a standard unit can be improved by gold diffusion and the further improvement possible with the epitaxial unit.

In many switching applications, the higher gain may be more desirable than lower storage times. For example, microminiature *DCTL* circuits with silicon transistors could be designed to operate with the same fan-out at much lower power levels, since the gain at low currents is better in epitaxial units; Figure 5.

In some switching applications and in most linear amplifier applications, the achievement of higher breakdown voltages without degradation of other parameters will result in substantial circuit improvements. In switching circuits, considerably more power can be switched for about the same average device dissipation; also, higher collector voltages can be used without danger of *locking-up* at the $BV_{CEO}$ level.

In linear applications, the wider operating range of collector voltage will increase design flexibility. This, in combination with the improved gain-bandwidth due to lower $C_{OB}$, higher $F_T$, higher gain, and lower series collector resistance, could result in greatly improved circuit performance.

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[1] Theuerer, H. C., et al, Correspondence, *Proc. of the IRE*, p. 1642-43; September, 1960.

[2] Early, J. M., "PNIP and NPIN Junction Transistor Triodes," *BSTJ*, p. 517-533; Vol. 33, 1954.

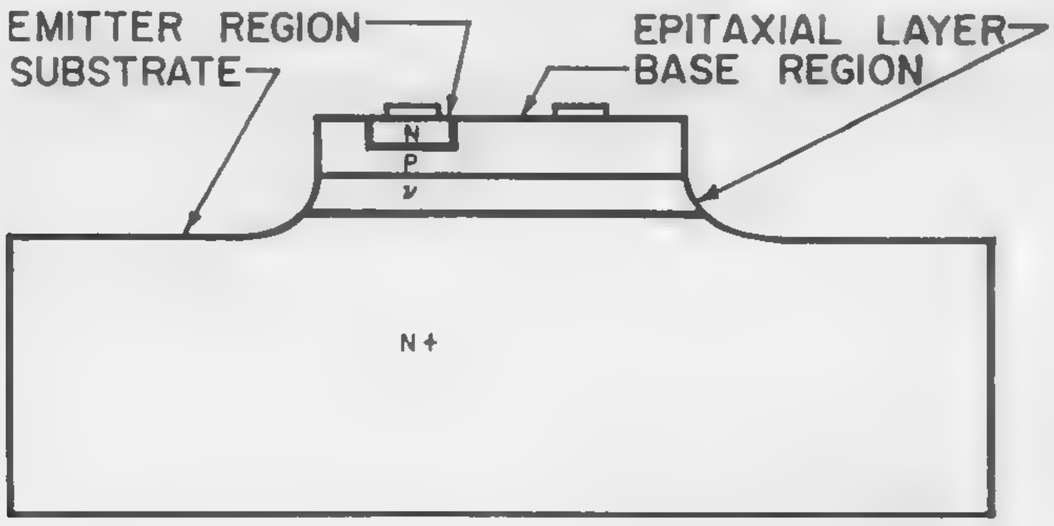


**Figure 1—Epitaxial mesa cross-section.**

| PARAMETER | CONVENTIONAL SWITCH | CONVENTIONAL AMPLIFIER | EPITAXIAL TRANSISTOR | UNITS |
|---|---|---|---|---|
| $BV_{CBO}$ (10 μA) | 50 | 77 | 120 | V |
| $BV_{EBO}$ (10 μA) | 8 | 8 | 8 | V |
| ALPHA (10MA) | .975 | .980 | .990 | |
| $I_{CO}$ (15 V) | .001 | .001 | .001 | μA |
| $I_{EO}$ (5 V) | .002 | .002 | .002 | μA |
| $V_{CE}$ ($I_C$=35MA, $I_B$=15MA) | .40 | .80 | .30 | V |
| $C_{OB}$ (5 V) | 5.3 | 35 | 1.8 | μμf |
| STORAGE TIME CONSTANT | 20 | 250 | 25 | ns |
| $F_T$ | 250 | 250 | 330 | mc |

**Figure 2—Comparison of typical parameter values for diffused silicon transistor.**

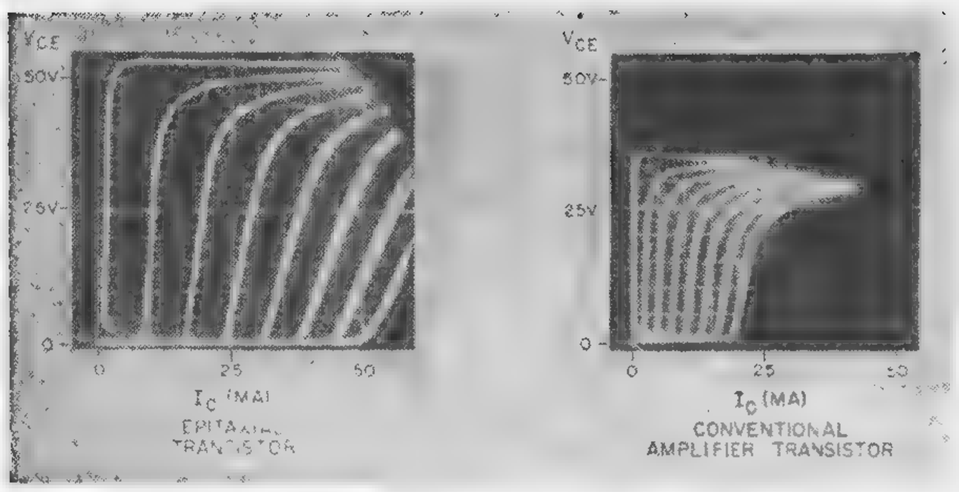


**Figure 3—Comparison of common emitter output characteristics; the $I_B$ varies from *0* to *0.14 ma* in *0.02 ma* steps.**

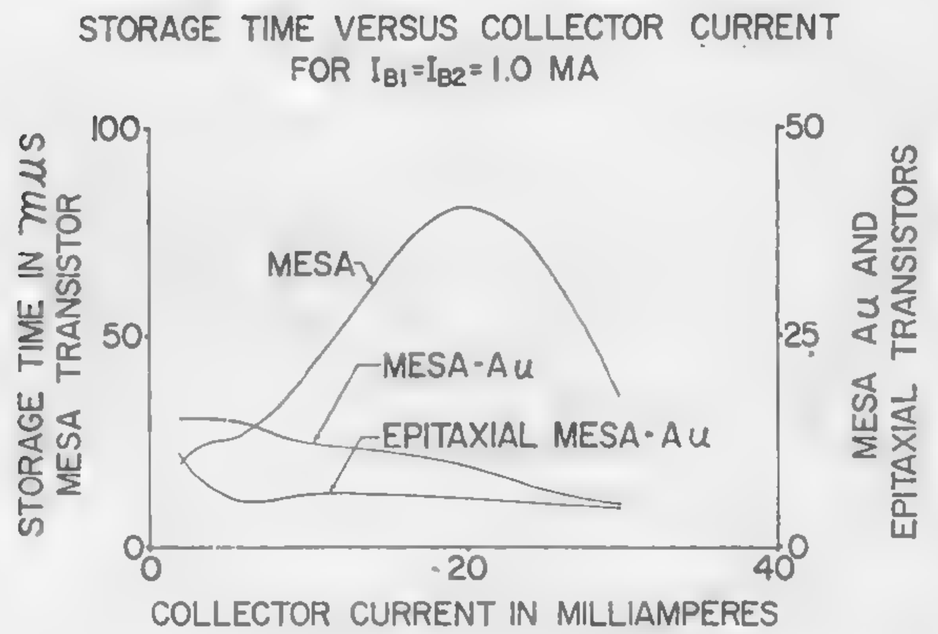


**Figure 4—Illustration of the anomalous storage time characteristics of some silicon mesa transistors and the improvements obtained from gold diffusion and the epitaxial process.**

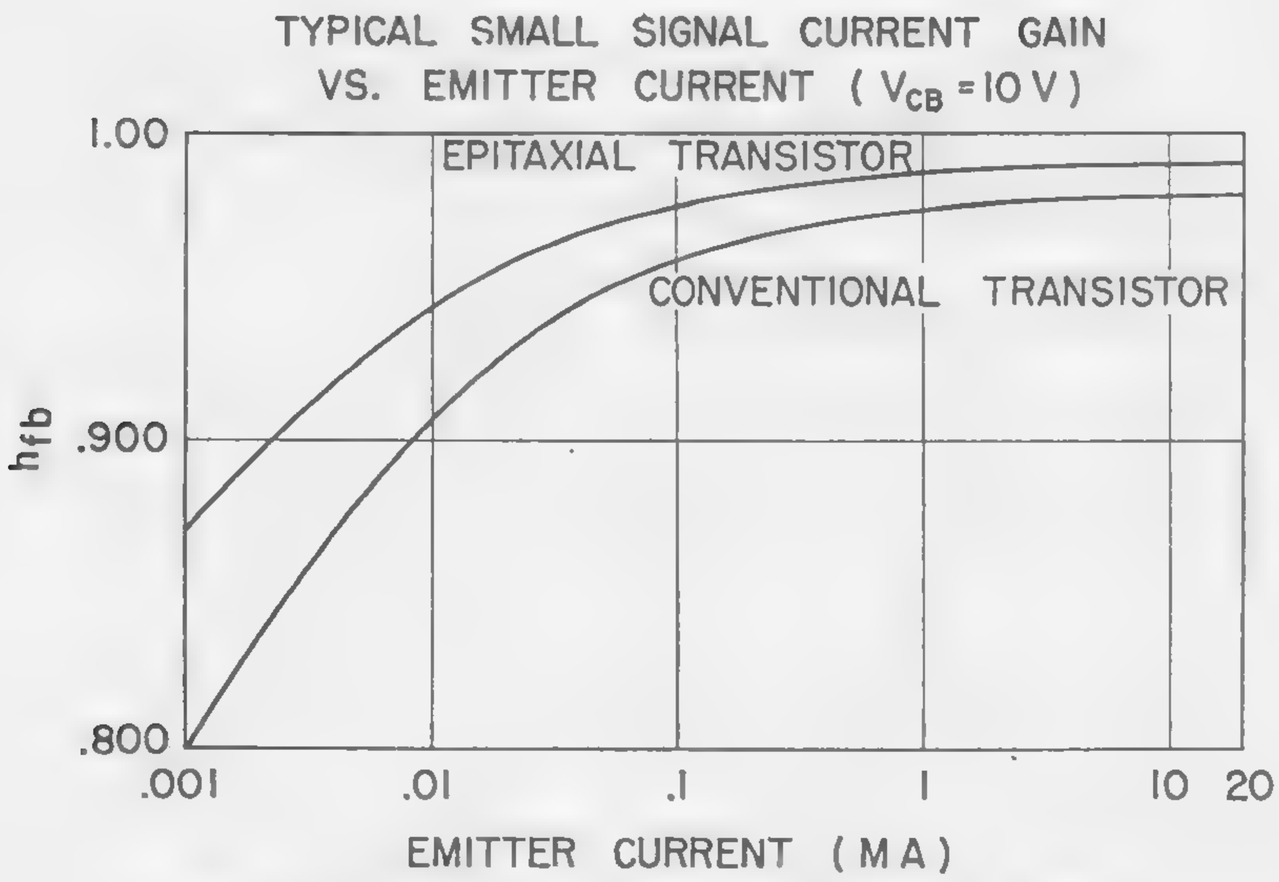


**Figure 5—Typical small signal current gain versus emitter current ($V_{CB} = 10$ *v*).**

## SESSION V: New Technologies

### 5.5: KMC Planar Transistors in Microwatt Logic Circuitry

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Mountain View, Calif.

THE CHARACTERISTICS OF ULTRAHIGH FREQUENCY silicon planar transistors currently under development make them ideally suited for use in very low current logic. These devices are characterized by an $f_{max}$ of greater than 1 *kMc* and an $f_T$ of approximately 800 *Mc*. The collector capacitance, excluding the capacitance of the header, is approximately 0.6 *pf*. Typical $h_{FE}$ and $I_{CBO}$ characteristics are shown in Figures 1 and 2, respectively. The holdup of $h_{FE}$ down to collector currents of 1$\mu a$ and the extremely low leakage (three orders of magnitude below this value) make such circuits feasible, and in addition the very low capacitance and high $f_T$ make it possible to operate them at reasonably high speeds.

One interesting application of such circuits would be in lightweight airborne or space equipment where low power dissipation and simplicity would further determine the choice of logic. Diode transistor logic is considered especially attractive from this point of view, because of the way in which fan-in and fan-out are conserved at a given current level. The simple form using backward diodes, shown in Figure 3, is considered especially interesting. It is seen to offer advantages over conventional diode logic, since there is no necessity for the voltage translating or compensating devices usually used in series with the base to compensate for the higher voltage drop of the conventional diode. Also, only one supply is required. The resulting circuit is nearly as simple, physically, as *DCTL*, but is capable of much higher fan-out, at a given current level. Fan-in is limited principally by leakage of the diodes. The *NOR* configuration of Figure 4 is also possible.

The *dc* criteria under which these circuits will operate is of primary concern in establishing their feasibility. The *dc* beta and a *current source factor* are seen to be the determining factors for fan-out. The current source factor is largely dependent upon supply voltage, but voltages as low as 1 *V* can be used while retaining a fan-out of 3 or 4. It is found that there is some loss of speed below a certain optimum voltage, however. For these devices this was found to be about 3 volts.

So far we have assumed no leakage through a path such as that shown in Figure 5. The criterion for minimum leakage indicates that high $V_{CE(s)}$ for the transistor and high $V_t$ and $V_d$ for the diode are desirable for turn on, while low $V_{CE(s)}$ and $V_t$ are desirable for turn-off. The circuits are feasible if the proper balance can be achieved between the two.

Variations of parameters with temperature, while always a problem, are seen at least partially to be in a favorable direction. That is, while $V_{BE}$ increases with decreasing temperature, $V_d$ also increases. $V_t$ remains very nearly constant with temperature, since it is due to a tunneling effect.

If the foregoing criteria cannot be met, compensation is possible using circuits such as those shown in Figure 6. Both effectively raise $V_{CE(s)}$. The first scheme is straightforward, while the second scheme puts the main burden of satisfaction of the criteria on the diodes.

#### *High-Speed Requirements*

Figure 7 shows propagation time versus current for a developmental transistor and backward diode, as compared with that of *DCTL*. These are found to be nearly identical, since below about 1 *ma* the speed is limited by capacitance and not storage effects. Low capacitance in the transistor and diode are thus mandatory for high-speed operation.

It is found that feedthrough becomes a problem at these levels, and this is another reason to keep capacitances low. Also due to the high impedance levels used, noise pickup can be a problem.

It appears that practical circuits of this type can be designed for operation in the 1-10 $\mu a$ range. This means that a 10,000-transistor computer would require a total of around 100 *ma* of current, and would operate in the 100 *kc* to 1 *Mc* range.

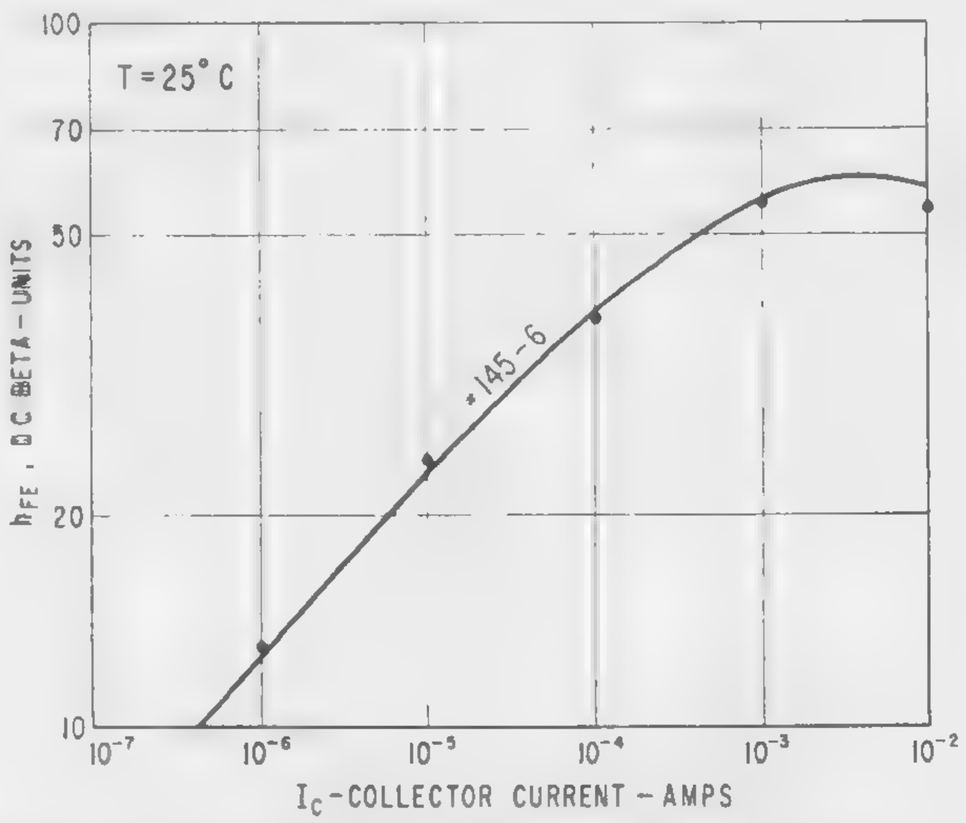


**Figure 1—Plot of $h_{FE}$ versus collector current for a developmental planar transistor.**

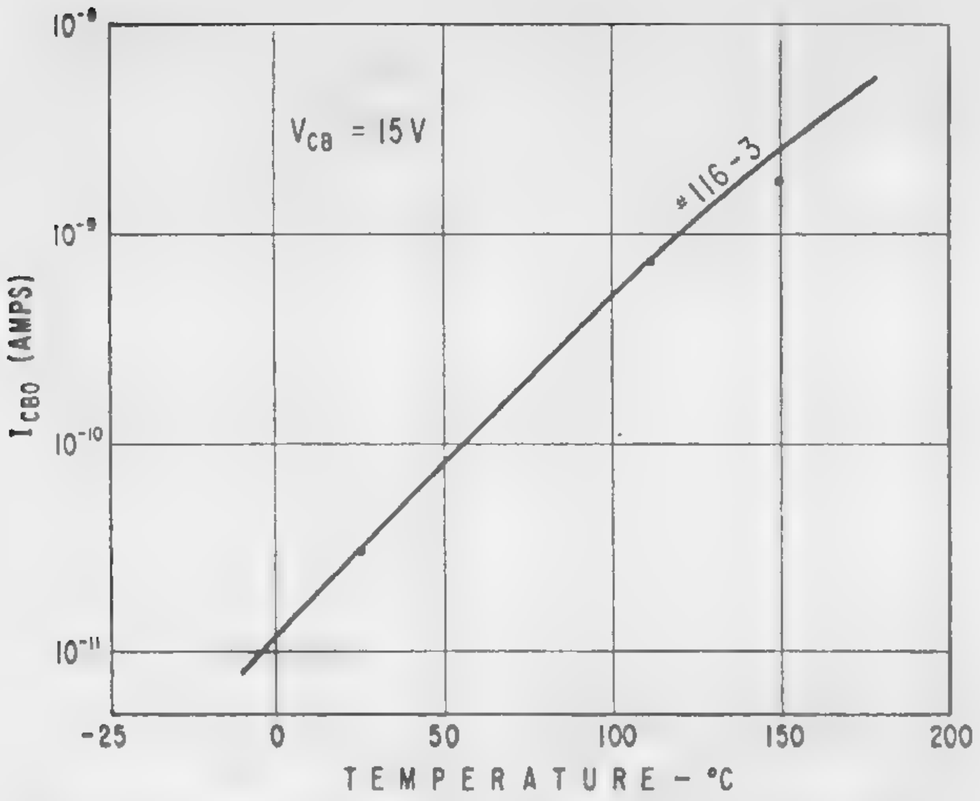


**Figure 2—Plot of collector leakage current versus temperature.**

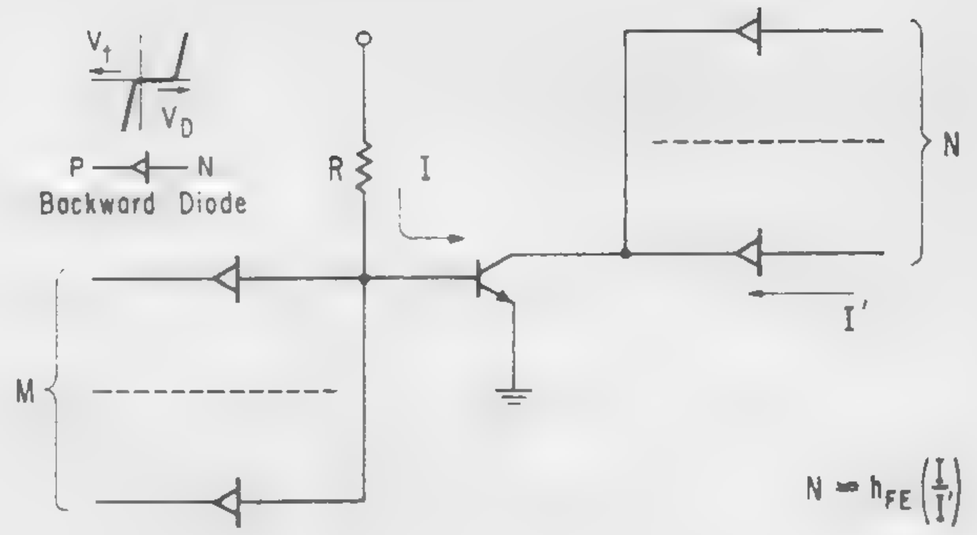


**Figure 3—Backward diode-transistor *NAND* logic circuit. The arrow points in the *easy flow* (low voltage or tunnelling) direction.**

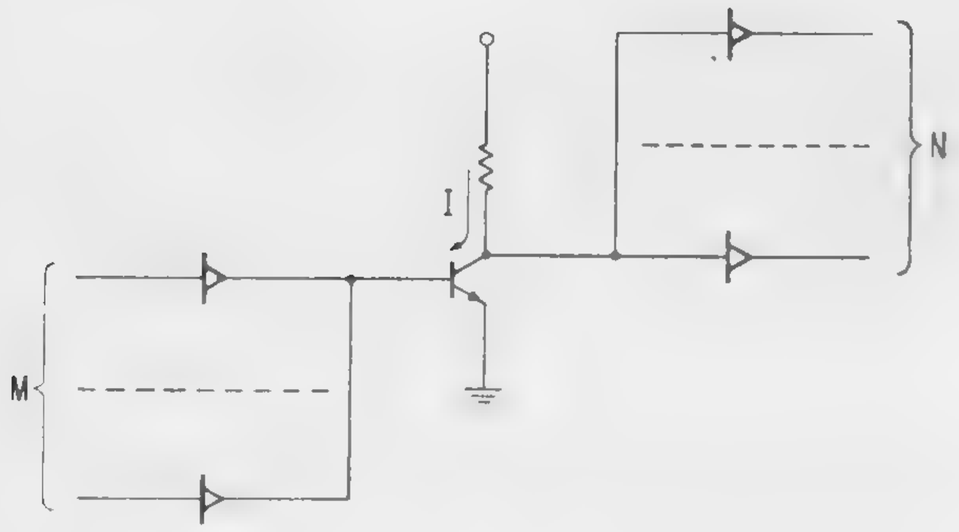


**Figure 4—Backward diode-transistor *NOR* logic circuit.**

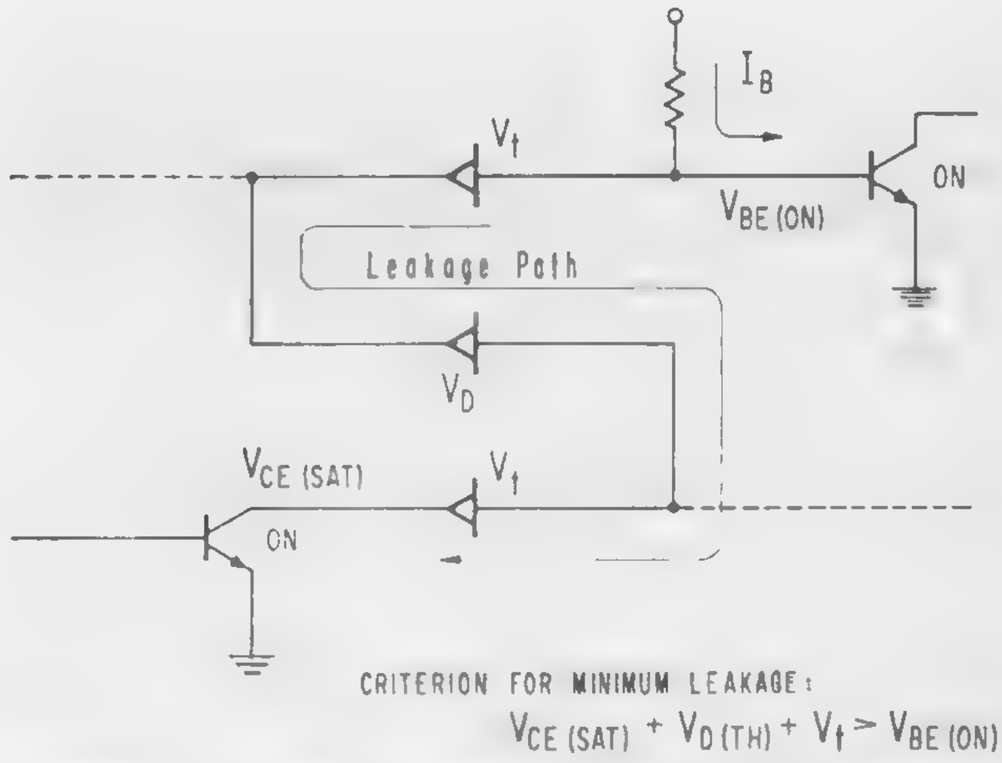


**Figure 5—Possible leakage path and necessary criterion to keep leakage to a minimum.**

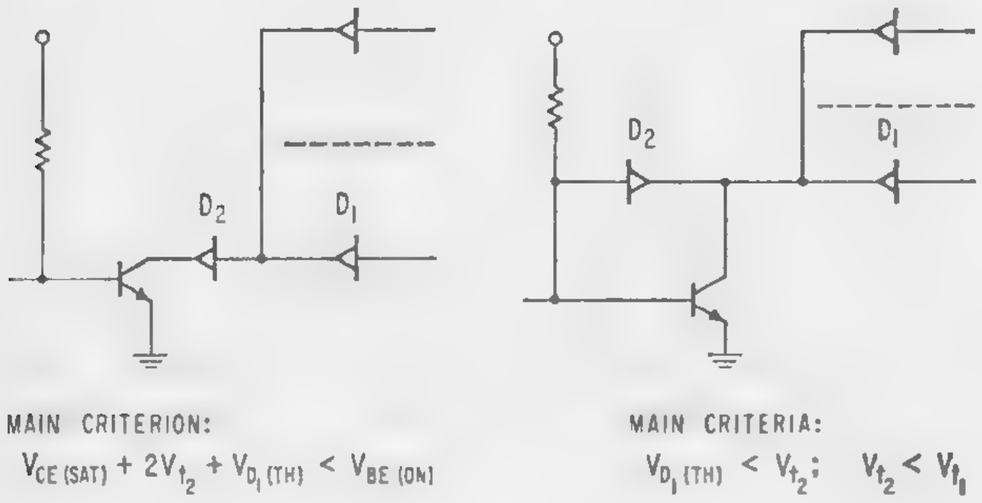


**Figure 6—Compensated circuits for the *NAND* configuration. $V_{CE}(s)$ is effectively increased to meet minimum leakage criterion of Figure 5.**

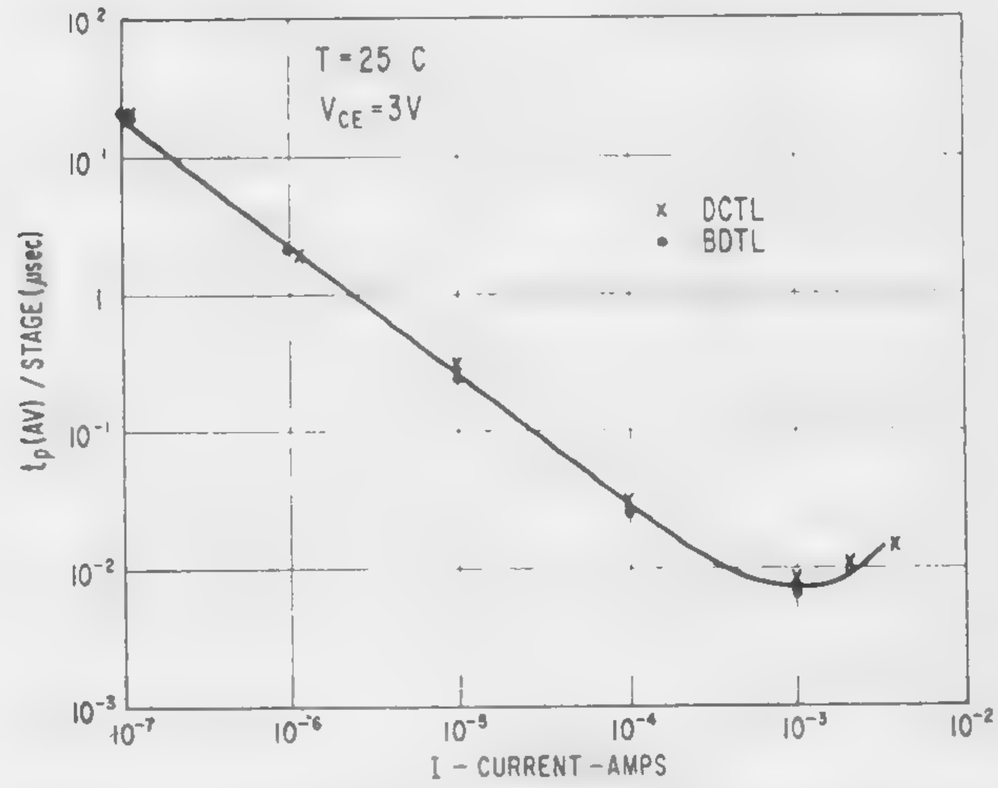


**Figure 7—Propagation time versus collector current for backward diode and direct-coupled transistor logic circuits. Below about 1 *ma*, speed is capacity limited.**

## SESSION VI: Computer Magnetics

Chairman: R. H. Baker
MIT Lincoln Laboratories, Lexington, Mass.

### 6.1: The Application of Domain Wall Motion to Storage Devices*

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Laboratory for Electronics, Inc.

Boston, Mass.

THIN MAGNETIC FILM STORAGE DEVICES described in the literature to date have taken the form of switching element arrays[1] and shift registers[2]. This paper will discuss the application of controlled domain wall motion to computer storage devices. A specific device employing this principle will be described as an example, along with experimental results.

An example of a device using controlled wall motion consists of a thin magnetic film, a tapered conductor which produces a time varying field whose magnitude varies monotonically along the film, and a readout means. By controlling the sense and magnitude of the magnetic field in accordance with the information to be stored, a linear array of rectangular domains representing this information may be placed on an initially saturated film. The stored information may be detected by observing the voltage induced in a pickup loop when the film is sequentially restored to a single domain condition. This is accomplished by means of the tapered-conductor's field which causes a domain wall to sweep across the film, and which successively reverses those portions of the film which had been altered during the writing cycle; the information may also be detected by magneto-optic means in a non-destructive manner.

Figure 1 illustrates the arrangement of a tapered sheet conductor (field generator), a magnetic film (storage medium), and a pickup loop (readout) as employed in a device using controlled wall motion. Current flow through the field generator is along the $x$ axis, and the field may be used to move walls from the left towards the right in the film. By controlling the sense and magnitude of the current by the signal to be stored, an information-bearing pattern of rectangular antiparallel domains may be left in the film.

The method of writing is explained in more detail by reference to Figure 2. The pulses used to write are those numbered *1* through *5* in Figure 2. If the magnetization of the film is in the negative $y$ direction before applying pulse *1* and if the result of applying pulse *1* is to magnetize the film in the positive $y$ direction, the resulting magnetization pattern will be as shown in Figure 3*a*, and will be comprised of two domains. After applying pulse *2*, the magnetization pattern will be as shown in Figure 3*b* and will consist of three domains. By continuing in this manner the film will be found, at the termination of pulse 5, to contain five domains as shown in Figure 3*c*. Figure 4 shows a typical domain cofiguration as seen by using the *Kerr* magneto-optic effect. When information is stored, the writing waveforms are modulated in accordance with the information.

If now the current is set to the proper polarity and increased uniformly, as shown on the right of Figure 2, a field just exceeding the coercive force of the film will progress along the film from left to right, restoring to the original state those regions which were reversed during the store interval. The voltage produced in the pickup loop has a waveform that is representative of the information stored. An example of this is shown in Figure 5*a*. Decoding methods similar to those employed in self-clocked magnetic recording[3] are available for recovering the information stored in this manner.

Since the precision with which a wall may be positioned is affected by scratches and inclusions at the macroscopic level and structural imperfections at the microscopic level, the ultimate limit in storage density of the device described seems to be set by the magnetic material and the field gradient. To determine the feasible information density, wall position as a function of the current in the tapered strips has been examined. The results of such observations (Figure 6) have shown that a wall may be placed within 0.18 *mm* of an arbitrarily-selected position. If this determination is carried out in the presence of another wall, however, it is found that the walls approach each other when they are within 0.75 *mm* of each other.

To study the speed of operation, the slope, $\gamma$, (amperes per second) of the reading current ramp is varied. Limitation of speed will be apparent by either a saturation of the wall velocity, $V_w$, as $\gamma$ increases, or by a sudden increase in $V_w$. The latter will arise due to multiple wall nucleation. Typical experimental data are given in Figure 7.

The device may be employed as a digital register, as a pulse train generator, or as an analog memory. As described here, it is a reversing register; with the addition of another tapered conductor, it becomes a non-reversing register.

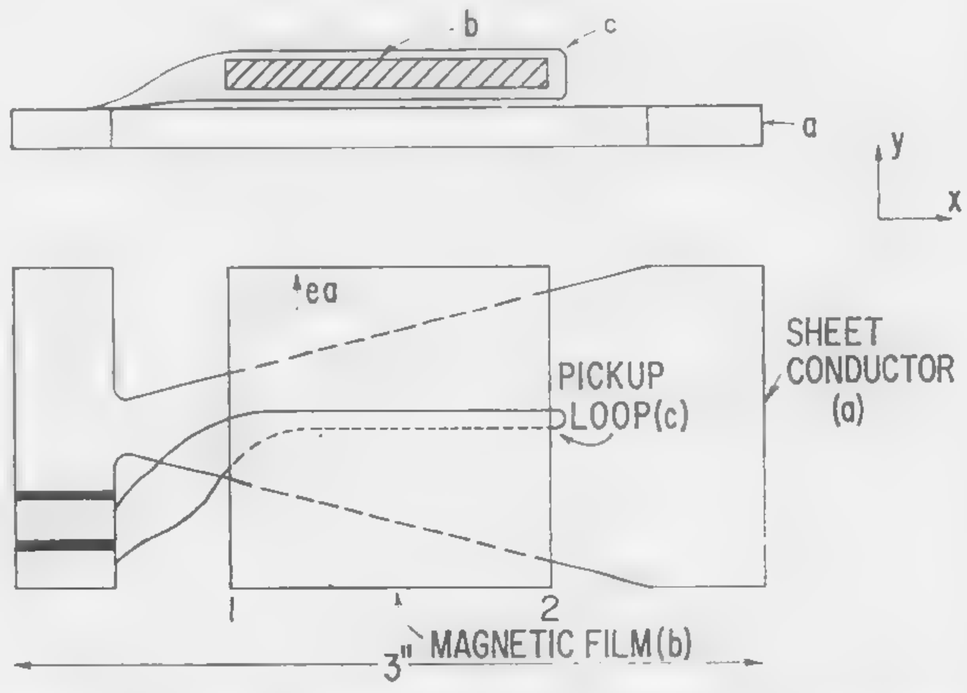



**Figure 1—An arrangement for producing controlled domain wall motion.**

* This work was supported in part by contract with the Information Systems Branch of the Office of Naval Research.

[1] Raffel, J. L., *J. Appl. Phys.*; 30, 1959.

[2] Broadbent, K. D., 1960 *International Solid-State Circuits Conference*, p. 24-25; Feb., 1960.

[3] Fuller, H. W., Woodsum, S. P., Evans, R. R., *Proceedings of the WJCC;* 1958. Also special AIEE publication T107.

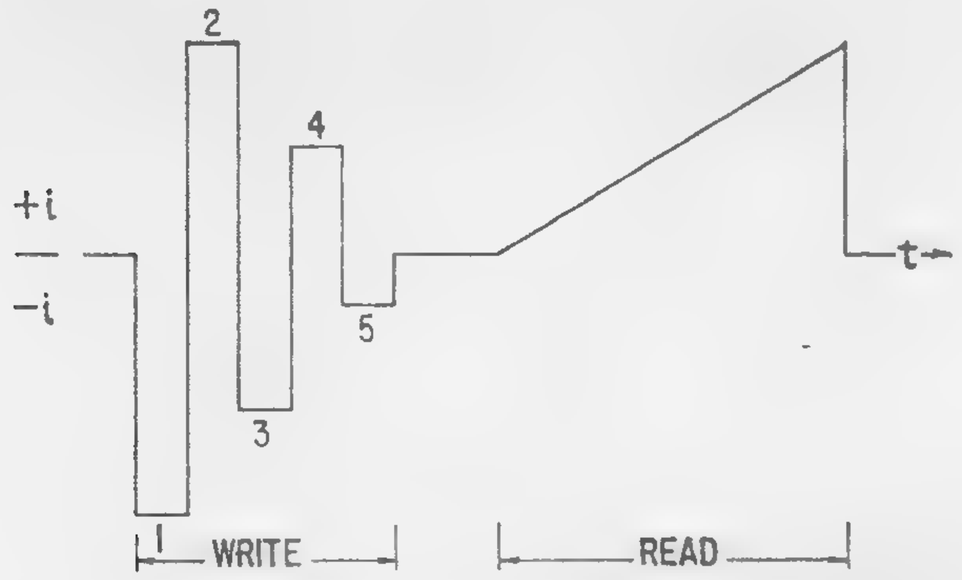



Figure 2—Reading and writing waveforms.

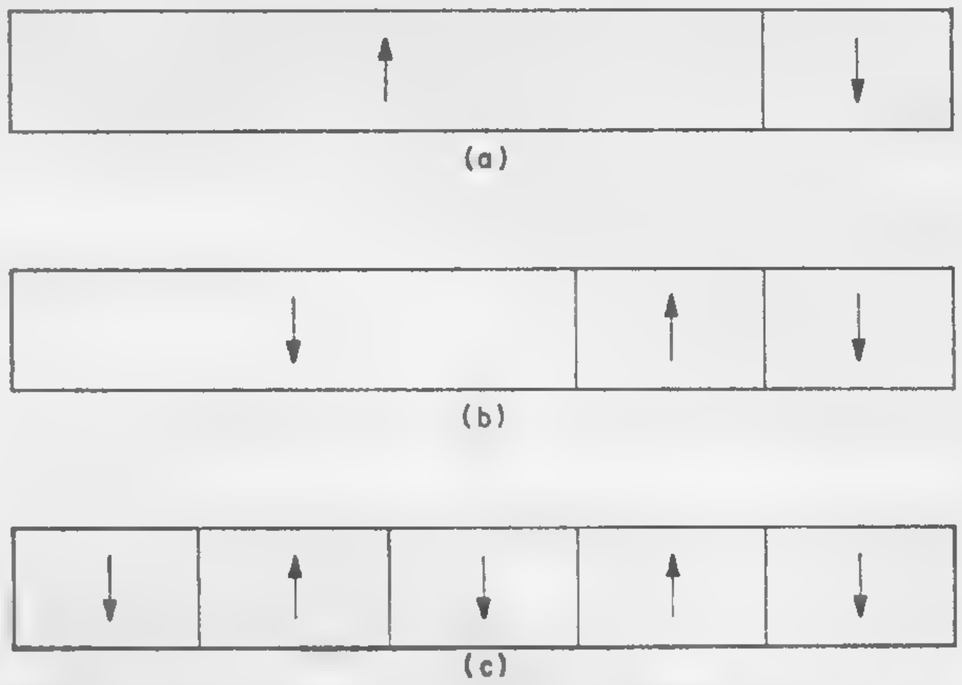



Figure 3—Magnetization states: *(a)* after write pulse *1*; *(b)* after write pulse *2*; *(c)* after write pulse *5*.

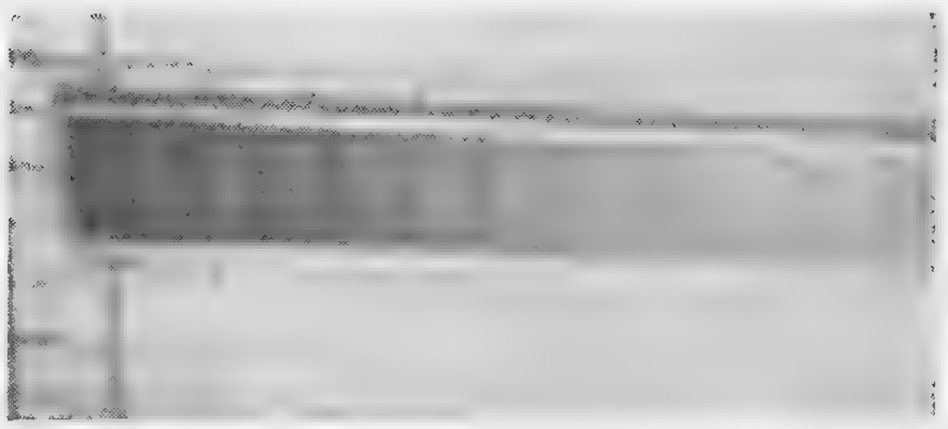


Figure 4—*Kerr*-effect photograph of a typical domain sequence resulting from writing.


Figure 5—*(a)* Waveform produced by moving a wall via control through the domain pattern shown in Figure 3. *(b)* Waveform during read in which the complete film is reversed. For the case of no reversal during read the base line noise is the only output.

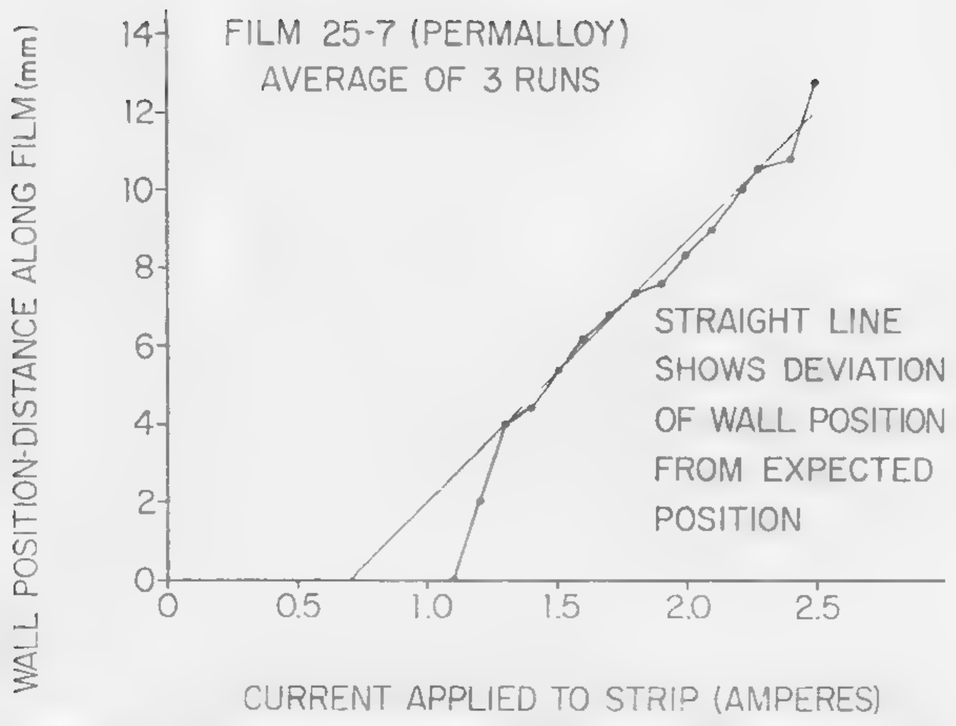



Figure 6—Wall position as a function of writing current.

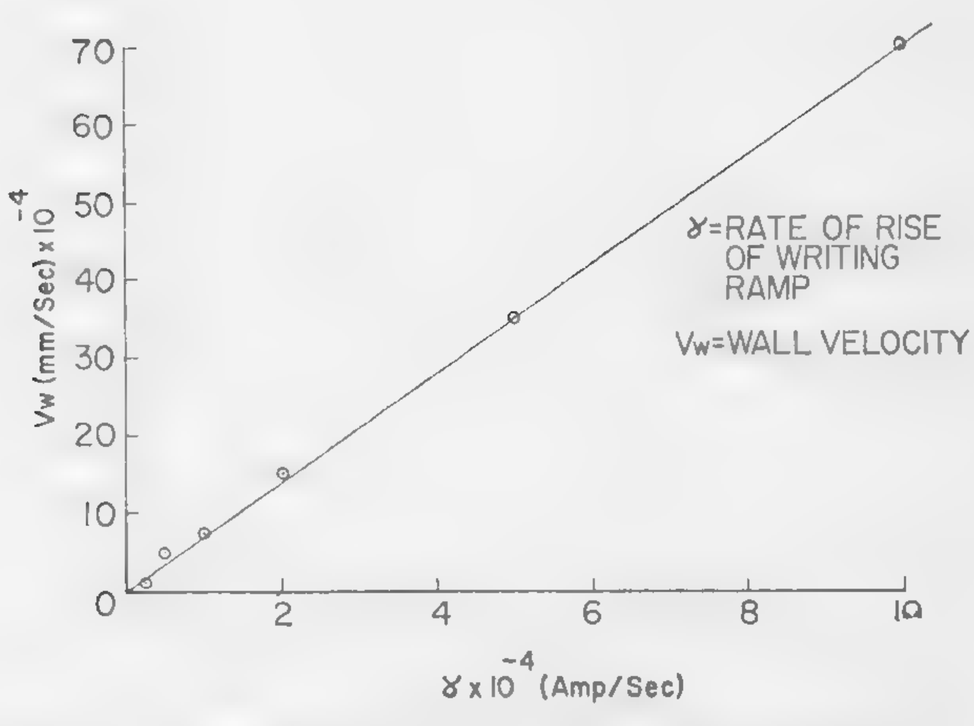



Figure 7—Wall velocity, $V_w$, as a function of slope, $\gamma$, of writing ramp.

## SESSION VI: Computer Magnetics

### 6.2: A Study of Switching in Thin Magnetic Films

W. Dietrich and W. E. Proebster

IBM Corporation

Zurich, Switzerland

THE MAGNETIZATION REVERSAL in thin permalloy films is characterized by the *dc* wall motion threshold $H_C$, by the onset of fast irreversible rotation at a field $H_{S1}$ and by complete fast rotation at a field $H_{S2}$, when a pulse field is applied[1]; Figure 1. For fast memory application, the width of the zone $(H_{S2}\text{-}H_C)$ is of utmost importance and discussed in some detail for different memory concepts.

In the conventional 3*D* memory, reading and writing is based on the coincidence of two fields, i.e., one field alone may not change the magnetization irreversibly, while the two coinciding fields have to switch the film rapidly. To this end it has been proposed to apply parallel fields to the film at a slight angle to the easy axis[2]; Figure 2*a*.

To investigate $H_C$ and $H_{S2}$ the amount of partially switched flux has been recorded for a number of films, when field pulses are applied at an angle of 45° to the easy axis. It has been found that these 45° experiments yield analogous results as those for smaller angles.

For a study of $H_{S2}$, field pulses with a risetime of $< 0.35$ *nsec* and a length of 20 *nsec* have been employed. In a first experiment the film was reset to the single domain state prior to each switching pulse. All switching measurements reported in the literature are based on this experimental condition[3,4]. In a second experiment a large number of pulses of alternating polarity, but of equal amplitude and length, were applied to the film. In Figure 3, the partially switching flux, consisting generally of reversible and irreversible parts, is plotted versus field amplitude for four typical film samples. Below a field slightly larger than $H_K/2$, only reversible flux changes occur.

These results clearly show that the threshold field $H_{S2}$ is larger than $H_{cr}$ and increases considerably for bipolar pulses. The increase can be explained by the splitting up of the film into many small domains, which impede complete switching[5].

The wall motion threshold $H_C$ was examined by applying a large number of field pulses at 45° to the easy axis. Figure 4 shows the amount of flux which has switched after a number of pulses of various risetimes, lengths and amplitudes has been applied. These results indicate that even at pulse field amplitudes well below the *dc* wall motion threshold $H_C$, small irreversible flux change occurs. This creeping increases with increasing risetime, length, and amplitude of the pulses. It is assumed that creeping is due to the open flux configuration of thin films.

If we consider a word-organized memory in the parallel field concept, only the write operation is based on field coincidence. During the read operation the single domain state can be rapidly restored by a short pulse of large amplitude. This allows avoidance of the increase of the necessary write fields according to Figure 3. However, the required restore pulse amplitude was found to be quite large and averages between 4 to 6 times $H_{C45}$. Moreover, creeping also represents a serious obstacle here.

The perpendicular field memory[6,7] is word-organized. The word field $H_W$ is applied in the hard direction, the bit field $H_B$ in easy direction; Figure 2*b*. Pulse experiments have shown that for this case complete or partial flux reversal is fast, regardless of whether the initial state is split or single domain[4]. In addition it has been found that the required tolerances with respect to easy axis alignment are not stringent; Figure 5. Also creeping is negligible, even when numerous bit pulses with amplitude almost equal to $H_C$ are applied.

### *Summary*

Summarizing, it can be stated that fast magnetic film memories of the parallel field concept are hard to realize, while for memories of the perpendicular field concept no restrictions by partial switching and creeping exist.

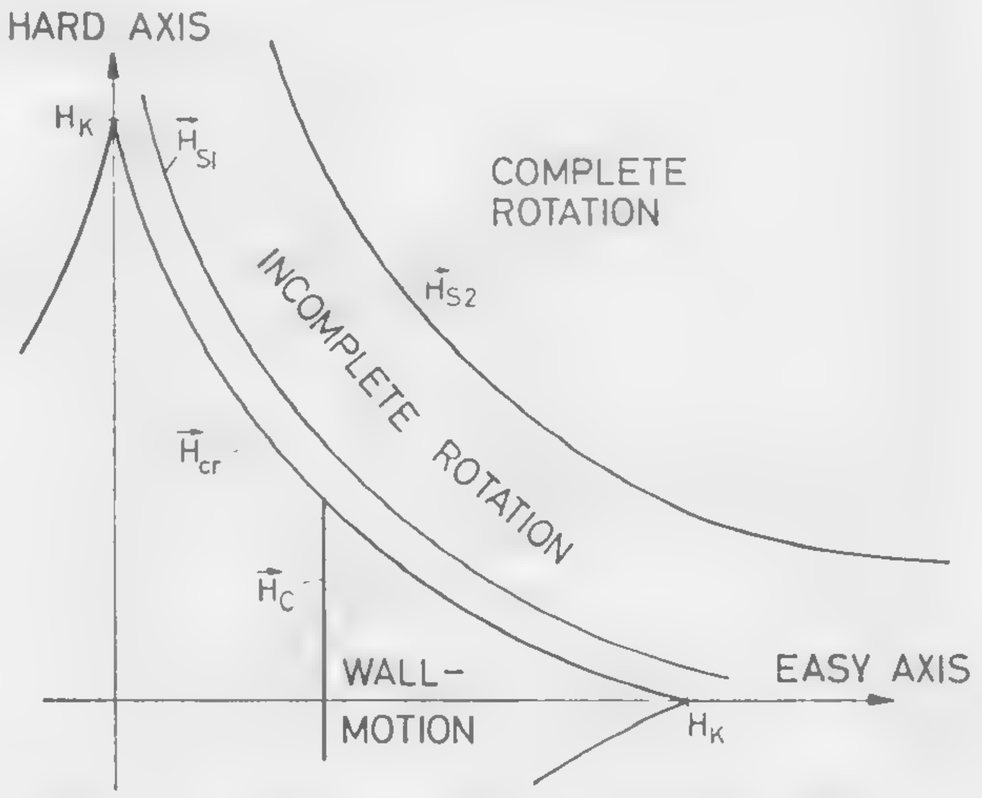



**Figure 1—Threshold fields in permalloy films. $H_C$ indicates the *dc* threshold for wall-motion, $H_{S1}$ the onset of irreversible rotation, $H_{S2}$ the threshold for complete rotation and $H_{cr}$ the theoretical rotational threshold; $H_K$ = anisotropy field.**

[1] Pohm, A. V., Mitchell, E. N., "Magnetic Film Memories, A Survey," *IRE Transactions*, p. 308; EC 9, 1960.
[2] Pohm, A. V., Rubens, S. M., "A Compact Coincident-Current Memory," *Proc. Eastern Joint Comp. Conf.*, p. 120; 1956.
[3] Olson, C. D., Pohm, A. V., "Flux Reversal in Thin Films of 82% Ni, 18% Fe," *J. Applied Physics*, p. 274; 29, 1958.
[4] Dietrich, W., Proebster, W. E., Wolf, P., "Nanosecond Switching in Thin Magnetic Films," *IBM Journal R & D* 4, p. 189; 1960.
[5] Methfessel, S., Middelhoek, S., Thomas, H., *J. Appl. Phys.*; in press.
[6] Raffel, J. I., "Operating Characteristics of a Thin Film Memory," *J. Applied Physics*, p. 605; 30, 1959.
[7] Bittmann, E., "Thin-Film Memories," *IRE Transactions*, p. 92; EC 8, 1959.

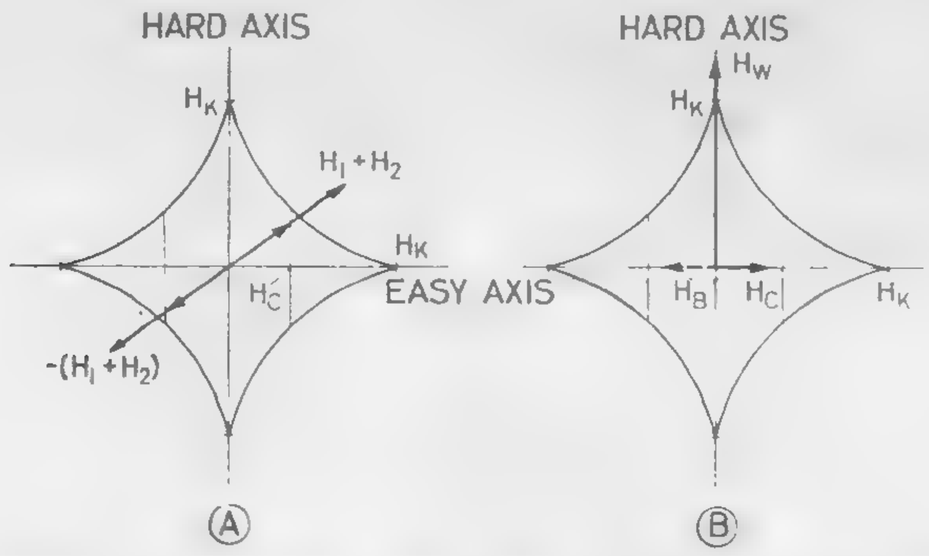



**Figure 2—Magnetic film memory concepts: Parallel field mode *(a)* and perpendicular field mode *(b)*.**

PULSE DURATION: 20 nsec
SOLID LINES: SINGLE PULSE APPL. TO SINGLE DOMAIN FILM
DASHED LINES: AFTER LARGE NUMBER OF BIPOLAR PULSES

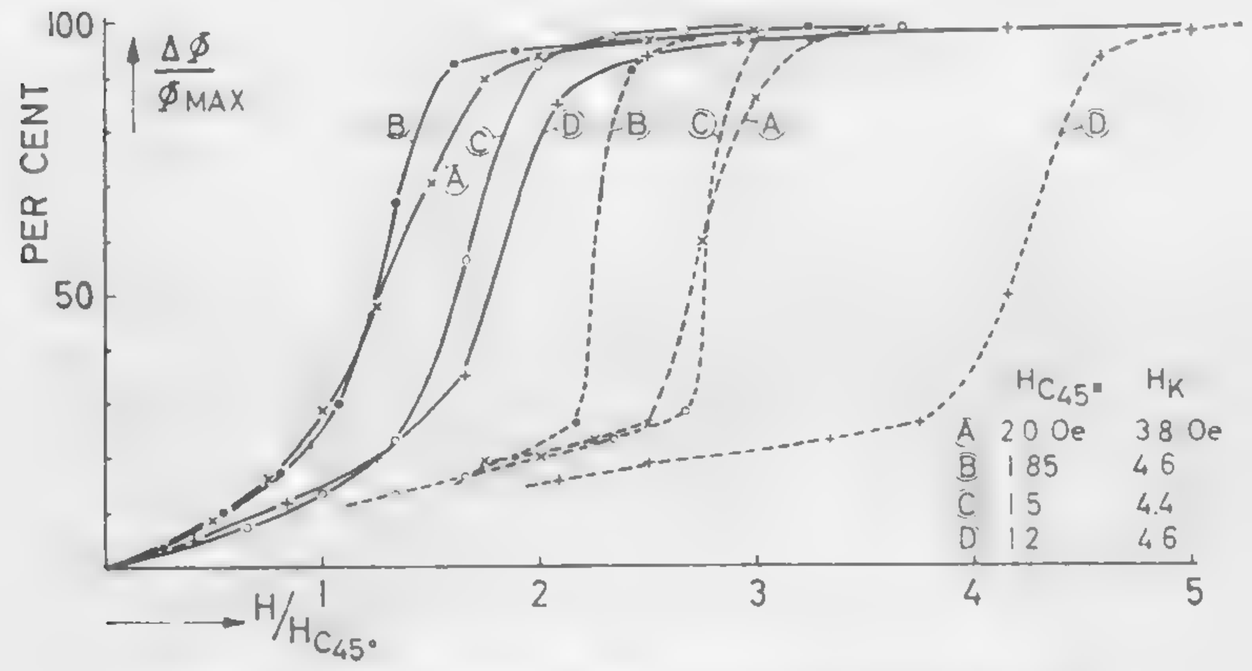



**Figure 3—Fast rotating flux for the parallel field concept. The pulse field $H$ is applied at 45° to the easy axis. The flux change $\Delta\phi$ and the *dc* wall motion threshold are measured in the same direction.**

| | A | B | C | D | E | F | G | |
|---|---|---|---|---|---|---|---|---|
| $\tau_R$ in nsec | <.3 | <.3 | <.3 | <.3 | 20 | <.3 | 1.2 msec | PULSE RISE TIME |
| $\tau_L$ in nsec | 200 | 30 | 200 | 30 | 30 | 30 | 5.0 msec | PULSE LENGTH |
| $h=H/H_{C45°}$ | .88 | 88 | .5 | 5 | .88 | .88 | 88 | NORMALIZED AMPLITUDE |

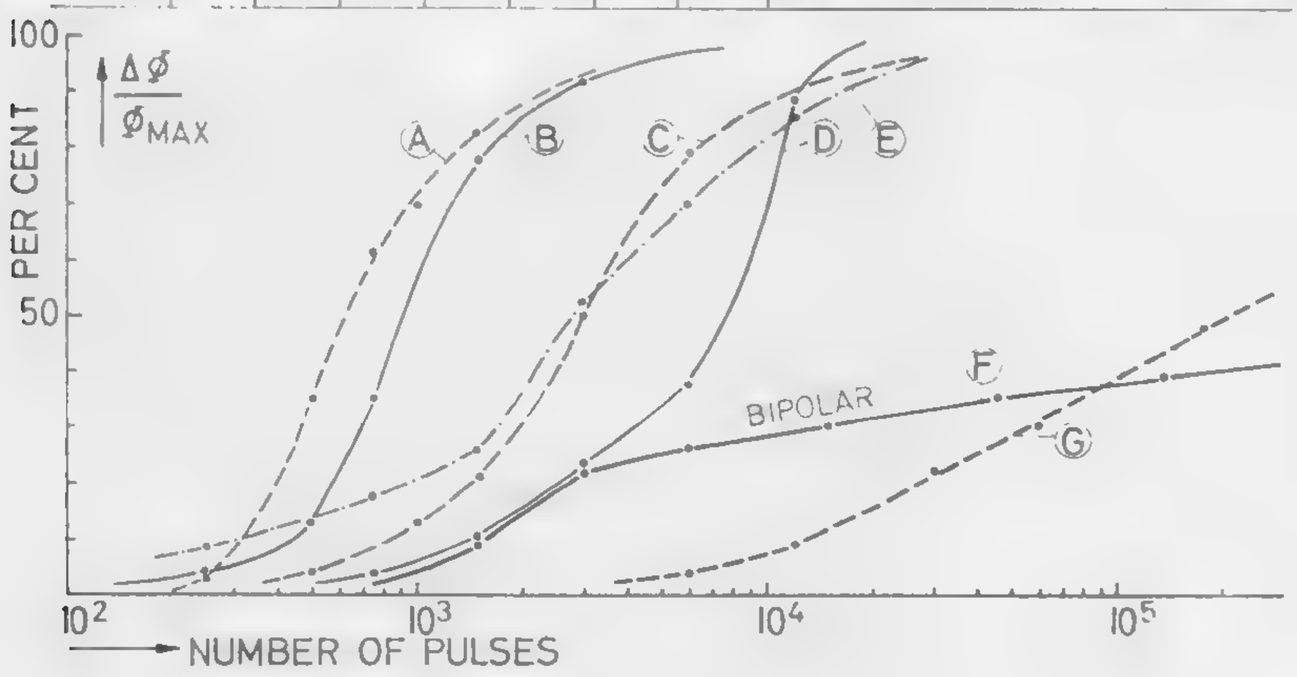



**Figure 4—Creeping effect for the parallel field concept. The flux change $\Delta\phi$ is plotted after a number of unidirectional or bipolar pulses are applied at 45° to the easy axis.**

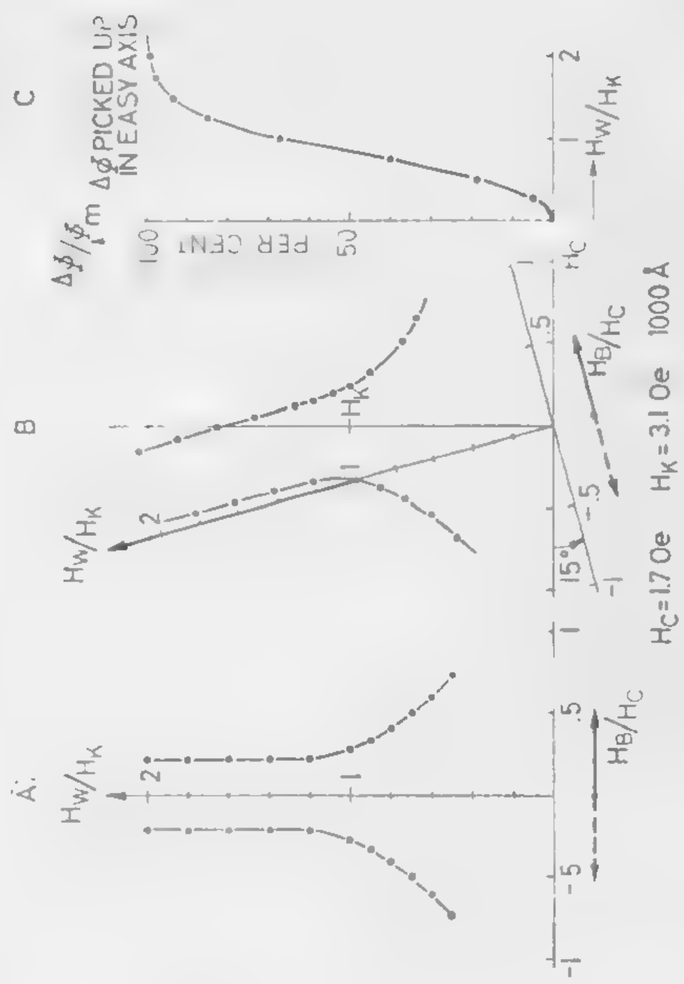



**Figure 5—Tolerance requirements for the perpendicular field concept. The minimum field $H_B$ is plotted versus $H_W$ for exact alignment *(A)* and 15° misalignment *(B)*. For each field $H_W + H_B$ the same amount of flux switches as for single domain switching at $H_W$ alone *(C)*.**

## SESSION VI: Computer Magnetics

### 6.3: AC and Impulse Switching Techniques for Fixed, Random Access, and Analog Memory Use*

**R. E. McMahon**

MIT Lincoln Laboratory

Lexington, Mass.

By combining a high-frequency sine wave drive with impulse or partial switching to ferrite cores, several useful memory techniques have been developed.

Figure 1 illustrates the characteristics obtained by combining the partial switching and *ac* drive.

The core is switched by the set and reset drive currents from a saturated state in one direction to a saturated state in the opposite direction. This normal mode of core operation results in the familiar core outputs, as shown below the drive currents in Figure 1.

If a high-frequency (5-100 *Mc*) sine wave drive is applied, in addition to the set and reset current, the result is a modulation of the core output that is maximum at the peak of the normal core output and minimum during the time the core is saturated. Figure 2 is a photograph of the normal core output and the modulation effects of the *ac* drive.

#### *Partial Switching Effect*

By partially switching the core to a point where the *ac* modulation is maximum, it is found that this large value of *ac* continues beyond this time after the partial set currnt is terminated. Figure 1 shows schematically the *ac* output continuing at a high level after the core is partially switched, while Figure 3 is a photograph of the partially switched core output with and without the *ac* drive current. In both photographs, the *ac* drive is reduced to a low value so that the *ac* modulation will not obscure the normal core output due to the set current, but for most applications the *ac* output is very much larger than shown.

Figure 4 is a photograph of the maximum *ac* output obtained and the minimum *ac* output that exists at saturation. Using one core per bit gives a signal-to-noise ratio based on this maximum and minimum *ac* signal of about *3:1*, while two cores per bit increases the signal-to-noise ratio to about *20:1*. By taking some care in the winding of the core it has been possible to obtain a *s/n* ratio of *80:1*.

#### *Important Aspects of the AC Characteristics*

The *ac* drive, if above 5 *Mc*, will not disturb the core either during the switching that occurs due to the set or reset current, or during th time that only the *ac* current is being applied. This non-disturbing effect continues even though the *ac* drive current amplitude is increased to 10 amp-turns for *80-50* mil cores having a normal threshold current of 600 *ma*. It is believed that this corresponds to the *Newhouse* region[1] where the domain walls are unable to reach a condtion of irreversible stability at current frequencies above 5 *Mc*.

The temperature stability of a core partially switched, but having only the *ac* drive applied is unusual and restricts the *ac* technique in some respects. The *ac* output is reduced at a rate much less than the normal core output by lower temperatures and if subjcted to liquid nitrogen temperatures recovers to its initial value when the temperature is returned to the starting value. When the temperature is raised, it appears that the low or *ZERO* (saturated) *ac* output is more sensitive than the high or *ONE ac* output.

#### *Applications*

An application that will illustrate the practical use of the *ac* and partial switching is shown in Figure 5. The audio input is sampled and the variable current output of the sampling circuit is used to switch partially the core to a degree depending on the sampled audio value. The *ac* output of the core corresponds to the degree of partial switching and if rectified can be used to reproduce the original audio that is stored.

A dynamic range of *60:1* for audio has been achieved in this application. Additional operational data and inverting properties of the rectified output for this and other applications will be discussed.

* Operated with support from the U. S. Army, Navy, and Air Force.

[1] Newhouse, V. L., *Proc. IRE*, p. 1484; 45, 1957.

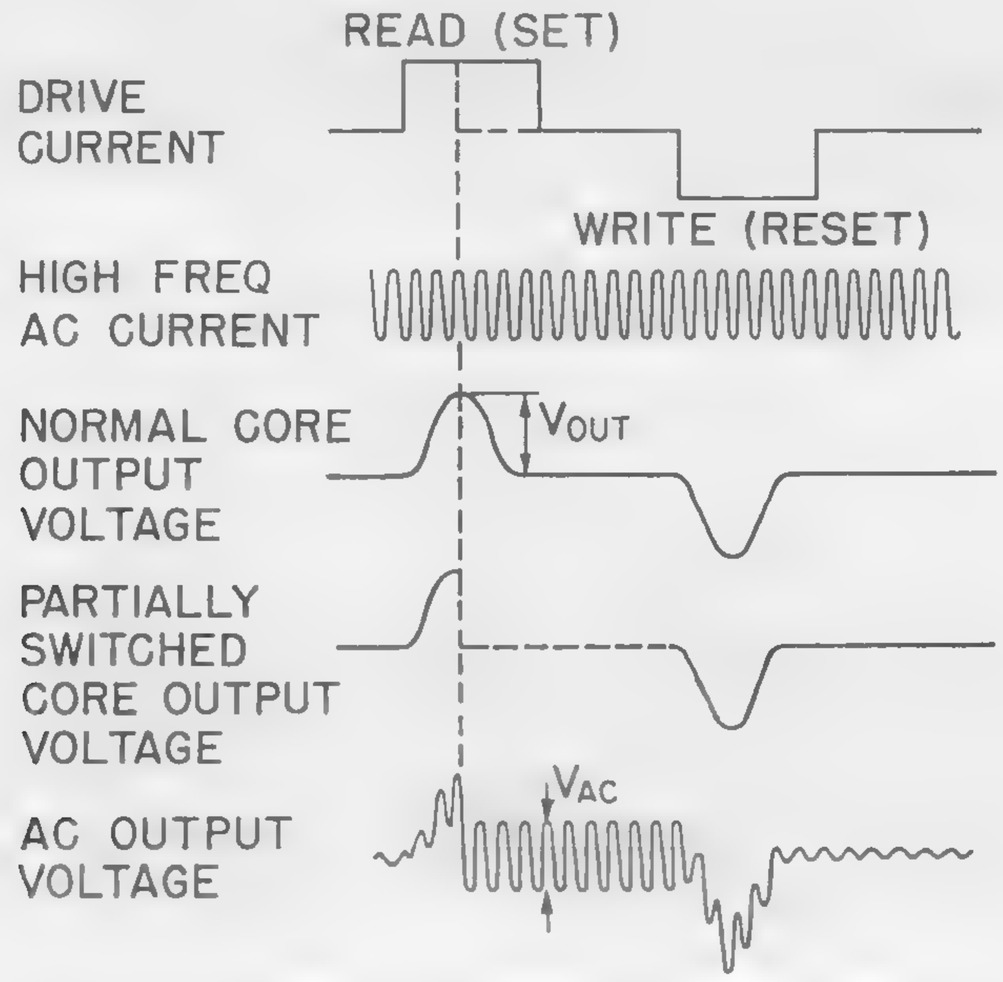



**Figure 1—Normal core switching currents and outputs, and partial switching with *ac* drive and the resulting *ac* output.**

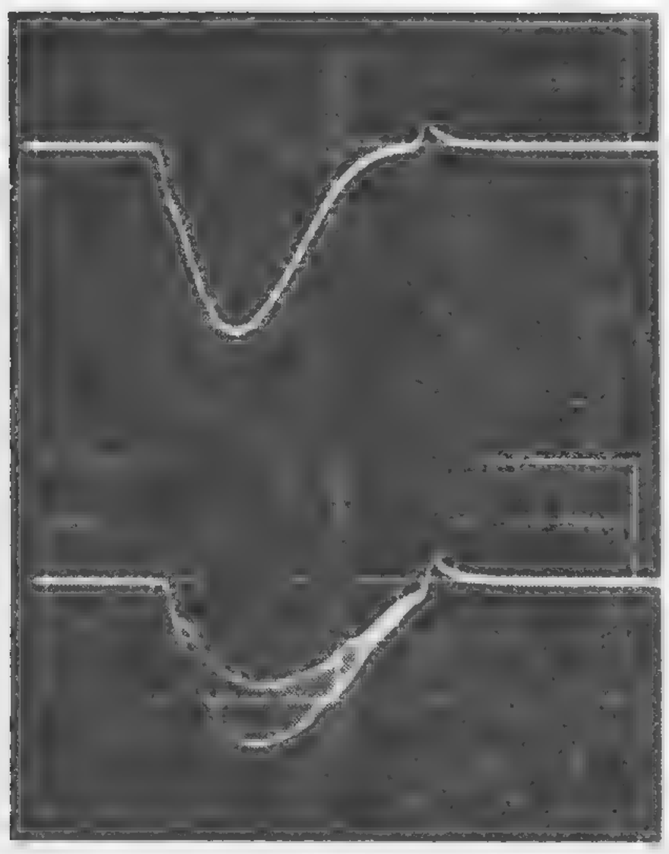


**Figure 2—At top, normal core output fully switched; bottom, normal core output with *ac* drive added.**

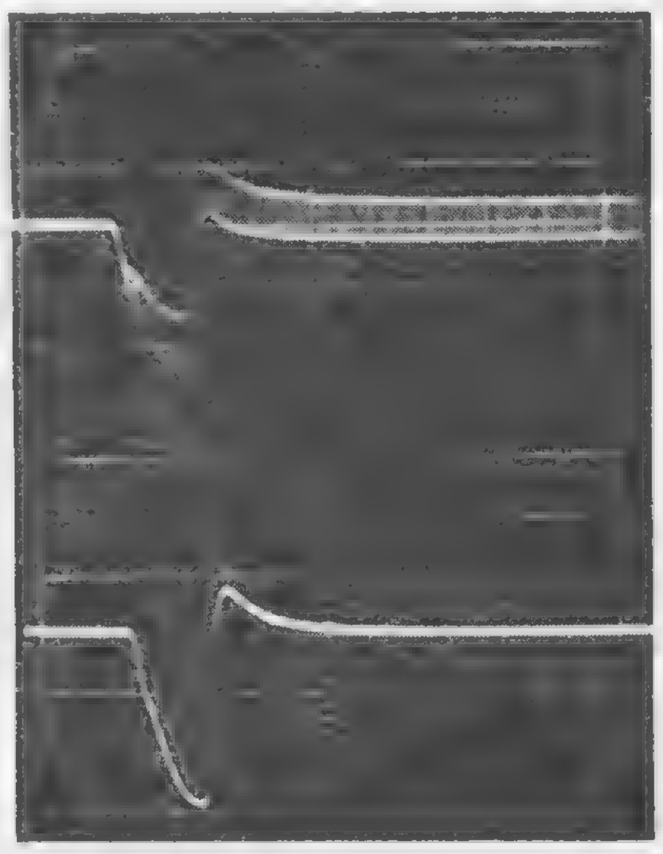


**Figure 3—Top pattern shows a partially switched core output. Bottom curves represent partially switched core output with *ac* drive added.**

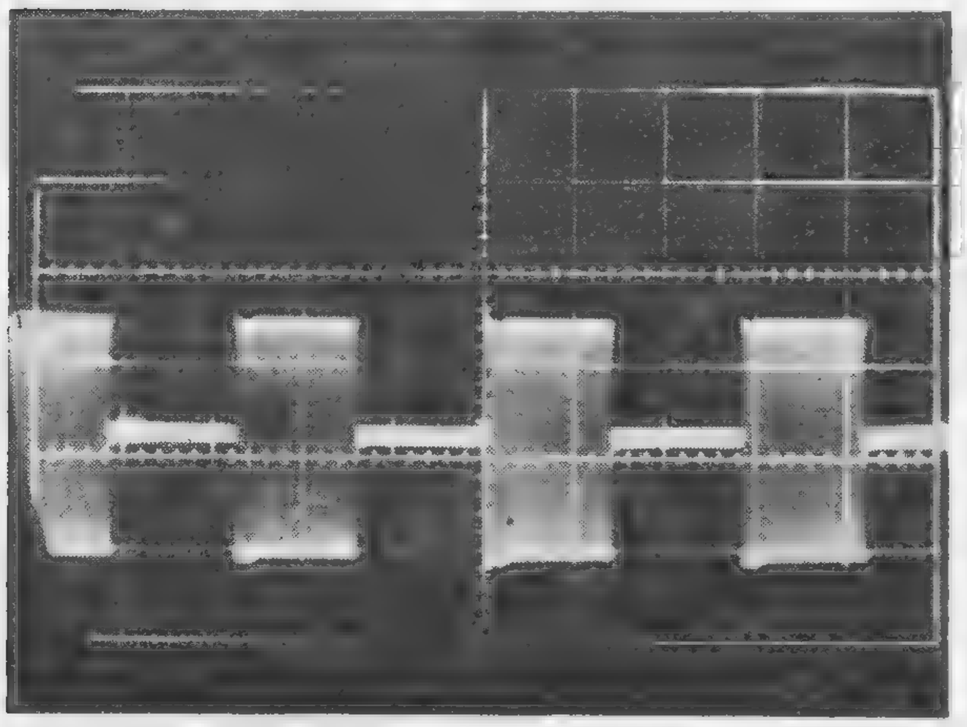


**Figure 4—The *ac* output levels for the *ONE* and *ZERO* case. The partially-switched core *ONE* has a large *ac* output (400 *mv*) while the saturated *ZERO* case has a smaller *ac* output (about 20 *mv*).**

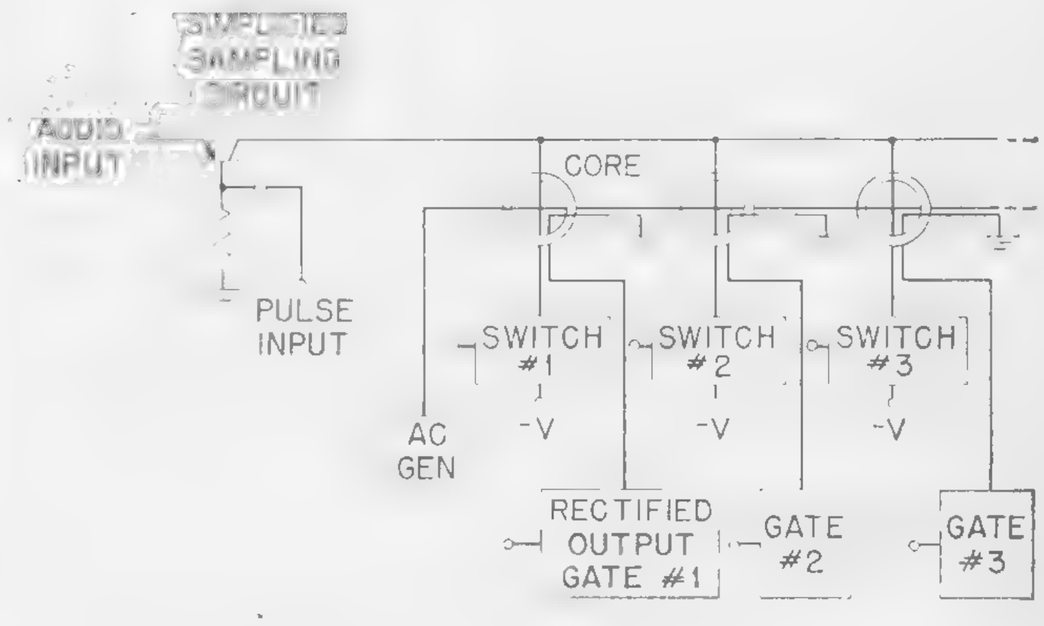



**Figure 5—Audio storage system. The stored information in analog form is selected from each core by the gated rectifiers.**

## SESSION VI: Computer Magnetics

### 6.4: A Word-Organized Memory Which Uses a Guided Flux for Reading and Writing

**R. M. Averill, P. S. Kopel and E. E. Newhall**

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

A SINGLE FERRITE SHEET, capable of storing a number of words, will be described.

During reading, currents in binary address wires guide the read flux to the selected word location. The bits in the desired word appear as voltages on output sense windings. The read flux may then be withdrawn from the selected word location by an appropriate reset pulse. During this reset interval, word drives are applied in a unique manner which write into the selected location only. The binary address wires are applied to the structure in such a way that a unique word location is associated with each input binary code. Thus, the structure performs address decoding. A four-word, four-bit-per-word memory, is shown in Figure 4.

Also to be described will be a scheme for stacking the single sheets to construct memory arrays larger than can be constructed on a single sheet.

Let us consider first the simple balanced magnetic circuit shown in Figure 1, with the initial flux pattern indicated. Suppose a current is applied to the reset winding at the same time a clockwise bit current is inserted. This bit current will tend to switch the left leg up and hold the right leg down. The overall effect will be to establish the flux pattern shown in Figure 1b. If the input bit current were of the opposite sense, then the resultant flux pattern would be as shown in Figure 1c. Thus, the memory location is left clockwise or counterclockwise, depending upon the sense of the input bit. It will be noted that the bit current by itself will be made insufficient to cause switching; however, in the presence of the reset drive, the bit current tips the balance one way or the other.

Now let us consider how this idea might be incorporated into a magnetic selector as shown in Figure 2; the basic gate used in this selector is shown in Figure 3. If the reset pattern is as shown, and the hold winding is energized as shown, then it is easy to see that flux cannot switch through this gate in either direction. Four of these gates are arranged in Figure 2, with binary variable $X_1$ and $X_2$ applied to the gates. It is easy to see that for any input code, one and only one leg is unheld. For example, if $X_1 = O$ and $X_2 = 1$, then it is clear that only leg 2 will be unheld. Thus, if a current is applied to the write winding at the same time the binary variables are applied, flux will switch down only leg 2. A unique leg is associated with each binary code, as shown in the table of Figure 2. The decoding scheme illustrated here may be combined with the selection scheme shown in Figure 1 in the manner indicated in Figure 4. Suppose a read flux has been guided to a selected leg, leaving this leg with the pattern shown in Figure 5*a*. Then, upon reset, suppose a clockwise *mmf* is applied to the top bit location, and a counterclockwise *mmf* to the bottom bit location. After the completion of reset, the pattern will then be as shown in Figure 5b. The pattern in bit location *1* corresponds to a ONE and the pattern in bit location *2* to a ZERO. Upon later interrogation by a read flux, the output polarity associated with bit *1* will be opposite from that of bit *2* shown in Figure 5C.

The memory appendage described suffers from the disadvantage that there are upper bounds on the bit currents. By means of an appendage modification, this disadvantage may be overcome, at the expense of decreased bit density.

*Acknowledgment*

The authors are indebted to *S. M. Neville, E. M. MacKinnon, J. R. Perucca, J. Muller* and *L. K. Degen* for assistance in preparing structures and performing experimental work; also *T. H. Crowley* for his help in evaluation.

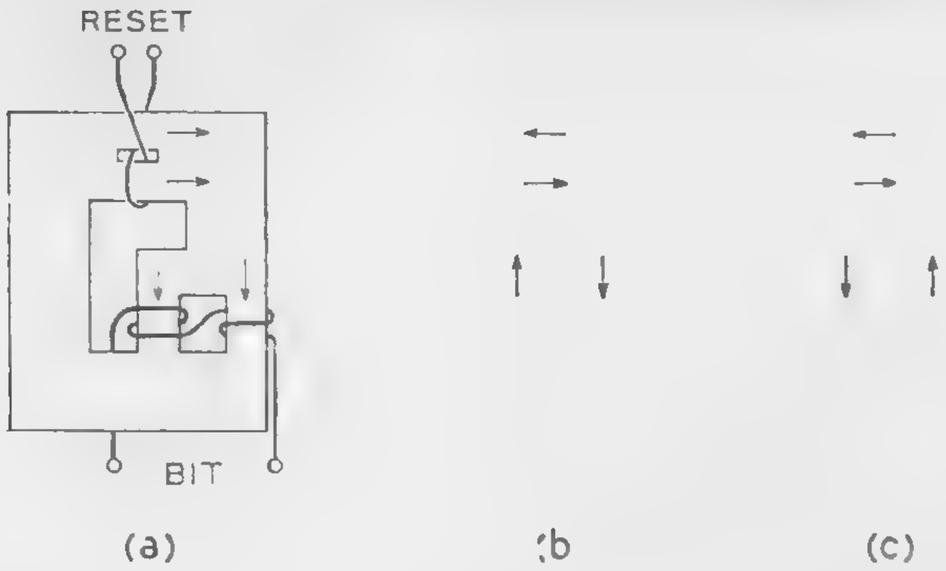



**Figure 1—A balanced magnetic circuit with parallel paths of equal path length.**

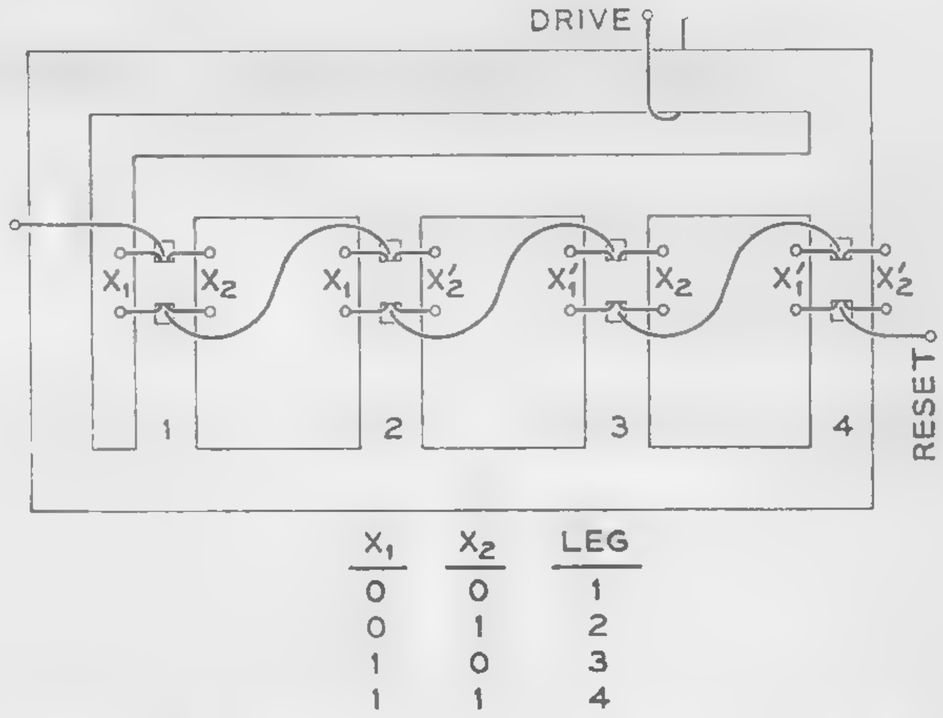



**Figure 2—A balanced magnetic circuit with four parallel legs, wired as a decoder.**

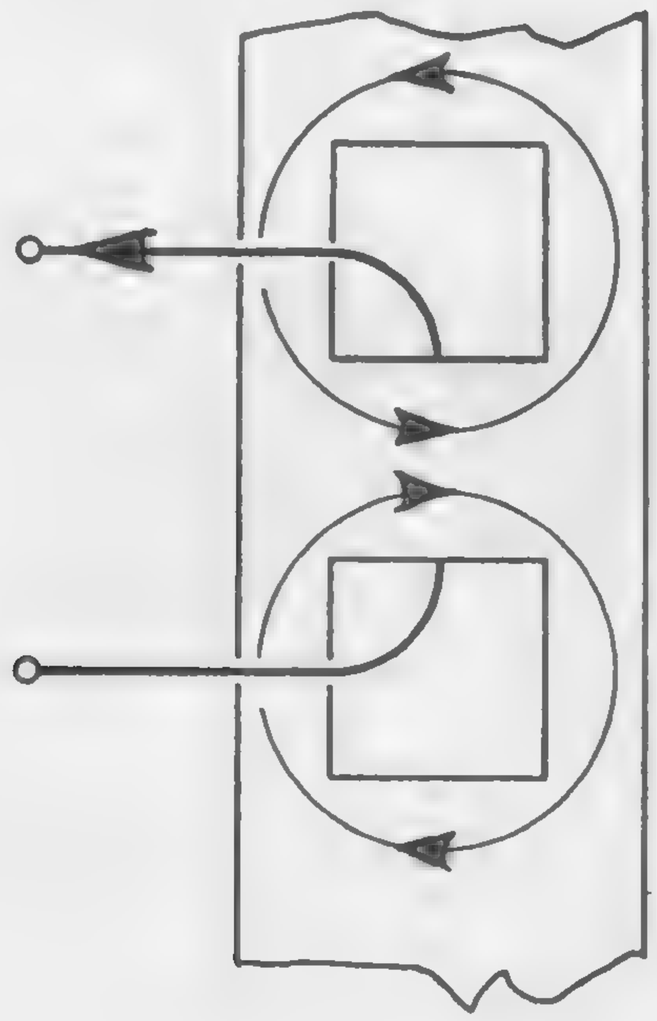


**Figure 3—A simple magnetic gate.**

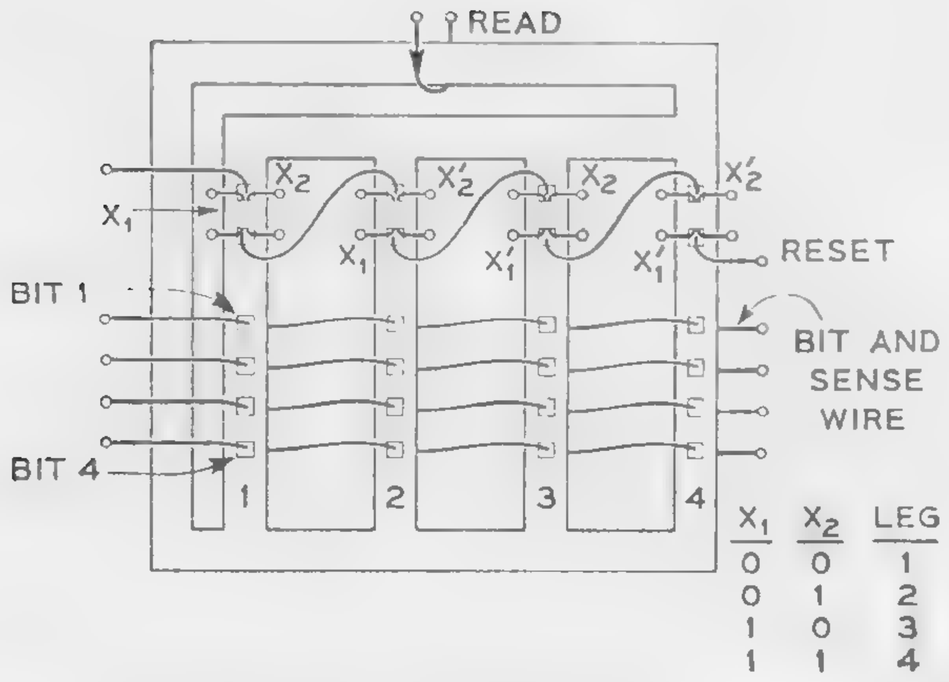



**Figure 4—One sheet, containing four words with four bits per word.**

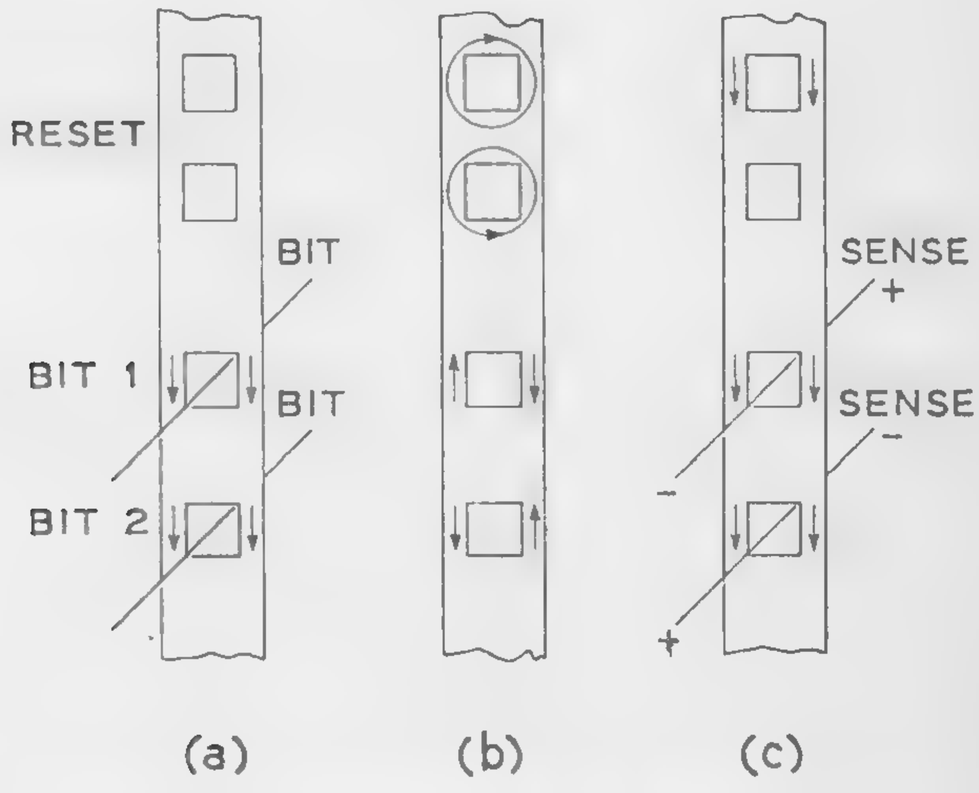



**Figure 5—Flux patterns during read and write.**

## SESSION VI: Computer Magnetics

### 6.5: Circuit Approach for an All-Magnetic Computing System*

**H. D. Crane and E. Van De Rief**

Stanford Research Institute

Menlo Park, Calif.

An all-magnetic arithmetic unit has been built and successfully operated[1,2]. It is capable of addition, subtraction and multiplication, with a product and sum capacity of three decimal digits. The system involves the use of some 650 *MAD* (multi-aperture device) elements and about 1000 toroids, each *toroid* being a stack of one to five 0.050-inch o.d. *memory* cores. The system is controlled from a manual keyboard, and readout from the machine is via incandescent lamps controlled directly from the *MAD* elements, no intermediate elements being required. The system is driven from a laboratory pulser, and the *worst case* drive-pulse amplitude range for the completed machine—i.e., varying all clock pulses simultaneously—is ± 10 per cent. Important assembly features of the system are that all coupling loops involve the use of single-turn windings, and all *MAD* elements are aligned in three dimensions, with clock windings being achieved "enmasse" by *push-through* wiring.

The sole logic building block of the system is a two-input inclusive-*OR* module with fan-out capability of three positive and negative outputs in any desired combination. The basic *MAD* transfer scheme (Figure 1) has been described in the literature.[3] Two innovations, flux doubling (Figure 2) and flux clipping (Figure 3), were added to this basic circuit to maintain the required flux gain relationships over wide tolerance ranges. The flux doubling technique involves the use of two *MAD* elements per module. These are arranged so that transfer from a module involves both elements, thereby providing sufficient flux to set a single *MAD* element of the following module, in spite of inherent flux losses. During the input phase, each element of a module is independently controlled from one of the two inputs. Before the output phase it is therefore necessary to ensure that both elements are in the same state. This is accomplished by the *internal* transfer labeled $A \leftrightarrow B$. By this process, the inclusive-*OR* function is generated. (The flux-doubling effect cannot be accomplished simply by a turns ratio in the coupling loop, since this would decrease the *mmf* available for receiver switching, with a resulting smaller tolerance on the drive-pulse amplitude.)

Explicit flux clipping is used to prevent zero flux level *build-up* through a number of transfers. Clipping is accomplished by adding to each coupling loop a toroid of small flux capacity and small switching *mmf*. Since the clipper switches with low coupling loop current, any zero noise flux is transferred to the clipper rather than the following module.

Negative transfer is accomplished by using the combination *MAD* and *toroid* technique[4] of Figure 4(*a*). When the *MAD* labeled □ switches, a current flows in the output circuit to switch (*set*) the small toroid. Transfer to the next module is achieved by driving the toroid in the *set* direction. Thus, if the toroid has already been switched, then no flux transfer takes place, and vice versa. A logical negative transfer is thereby achieved. The actual negative coupling loop used in the machine is indicated in Figure 4(*b*). It will be noted that the coupling loop connects to a small aperture rather than the main *MAD* aperture. This arrangement has some practical advantages [in particular for fan-out, as in Figure 5(*b*)] since the small toroid is completely decoupled during the input phase. The transfer from *MAD* to small toroid is accomplished during the clearing of the previous module.

Arrangements for maximum positive fan-out and for maximum negative fan-out are shown in Figure 5 (although any combination—up to three—is permitted). Positive fan-out takes advantage of the inherent non-destructive readout characteristics of *MAD*'s. For negative fan-out, the toroids of the three output coupling loops are connected in parallel to a single *MAD* aperture. In either case, positive or negative, the three output circuits occur at different pulse times to achieve large drive-current tolerances.

Circuit details for positive transfer are shown in Figure 6. Negative transfer circuits are similar except for the extra output toroid of Figure 4. A complete description of the all-magnetic computing system is scheduled to appear in the June, 1961, issue of *PGEC Transactions*.[5,6]

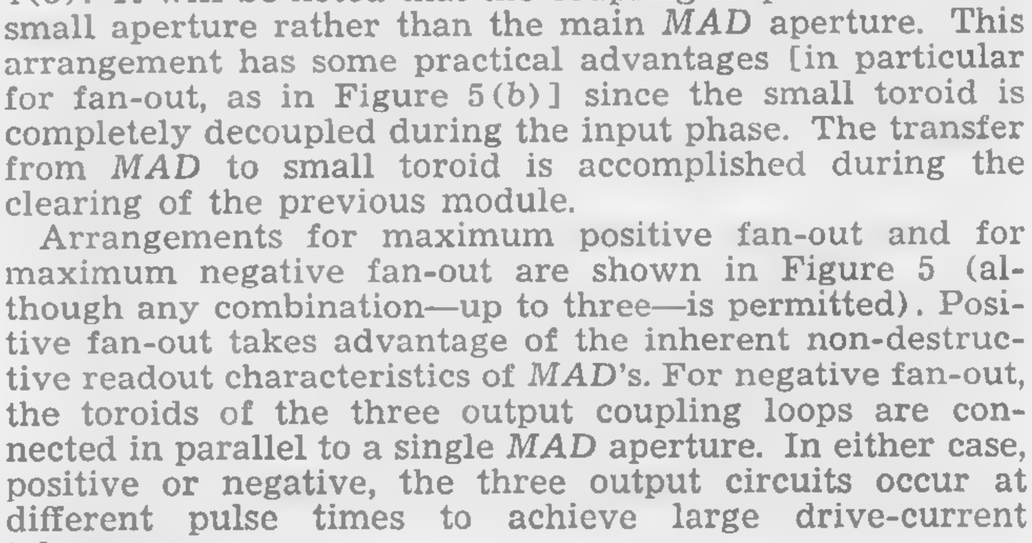



**Figure 1—Basic *MAD* transfer. Drive pulse sequence is □→○, clear □, ○→□ and clear ○.**

* The work reported here was supported by Contract AF 19(604)-5909, Air Force Cambridge Research Laboratories.

[1] Crane, H. D., "Research on the Realizability of an All-Magnetic Computing System," *Report* 1, *Contract AF* 19(604)-5909, Stanford Research Institute; October, 1959.

[2] Van De Riet, E. K. and Heckler, Jr., C. H., "Research on General Digital Logic Systems Utilizing Magnetic Elements and Wire Only," *Final Report, Contract AF* 19(604)-5909, Stanford Research Institute; October, 1960.

[3] Crane, H. D., "A High-Speed Logic System Using Magnetic Elements and Connecting Wire Only," *Proc. IRE;* January, 1959.

[4] Engelbart, D. C., "A New All-Magnetic Logic System Using Simple Cores," 1959 Solid-State Circuits Conference, *Digest of Technical Papers*, p. 68-69; Feb., 1959.

[5] Crane, H. D., and Van De Riet, E. K., "Design of An All-Magnetic Computing System — Part I — Circuit Design," accepted for publication in *IRE Transactions on Electronic Computers;* June, 1960.

[6] Crane, H. D., "Design of An All-Magnetic Computing System —Part II—Logical Design," accepted for publication in *IRE Transactions on Electronic Computers;* June, 1960.

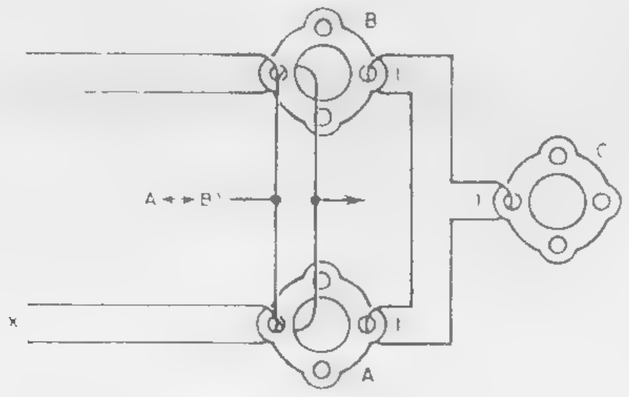



**Figure 2—Basic module. If either element *A* or *B* is *set* during input, then during the bidirectional *(A⇄B)* transfer both become set. Then, during output, flux from both elements is available for transfer to an input *C* of the following module.**

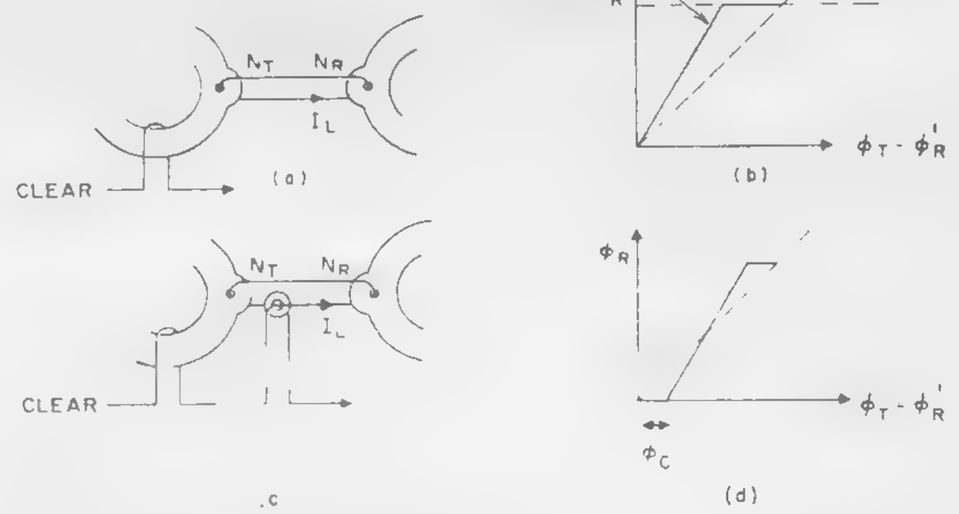
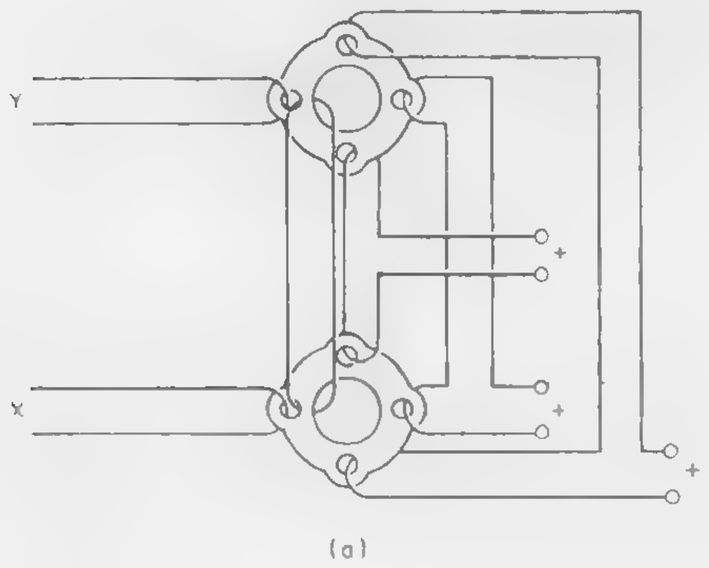
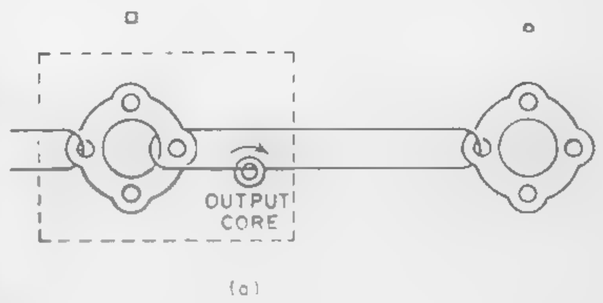


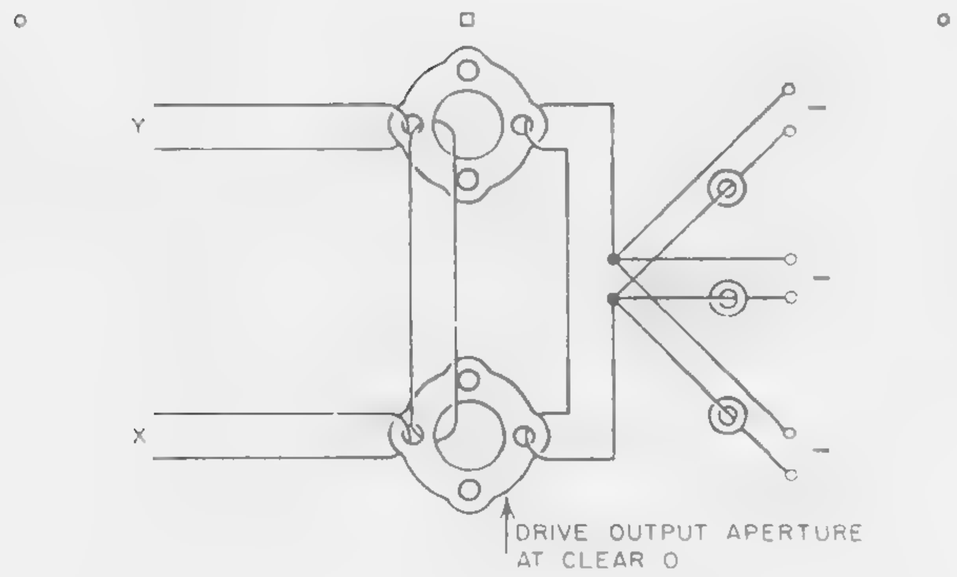

**Figure 3—Clipping. The circuit and gain curve are shown with and without a clipper core in parts *(c)* and *(d)*, and *(a)* and *(b)* respectively. The zero noise flux is in effect absorbed by the clipper core.**




*(Right)*

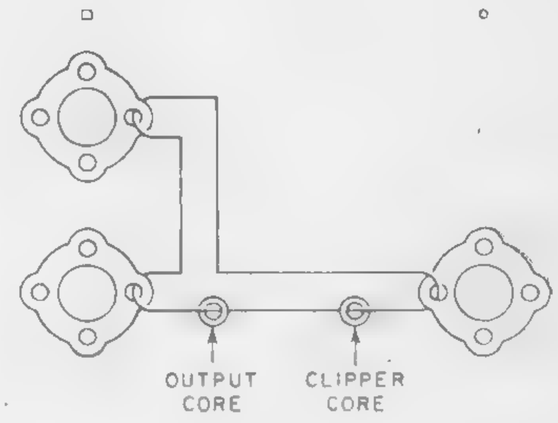
**Figure 4—*(a)* Basic negative transfer. *(b)* Actual negative coupling loop circuit. Output core is set from □ elements, then driven in *set* direction to transfer to ○ element. Thus ○ element has opposite state from □ elements.**




*(Left)*

**Figure 5—*(a)* Positive fan-out. *(b)* Negative fan-out. Positive fan-outs are taken from separate output apertures and negative fan-outs from a single one. Any combination of positive and negative is permissible up to a total of *3*.**



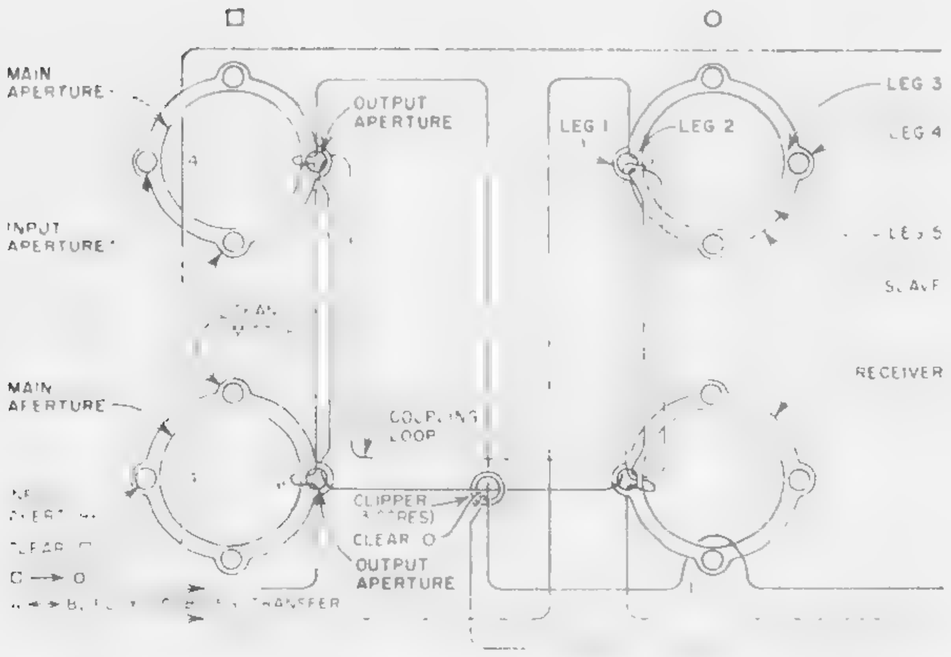




**Figure 6 — Detailed circuit. The negative transfer circuit is similar to the positive transfer circuit except for the additional output core and opposite polarity of the coupling loop on the receiver. Clear direction is clockwise in all elements. Small toroids 30-50 mil cores of S-5 material.**

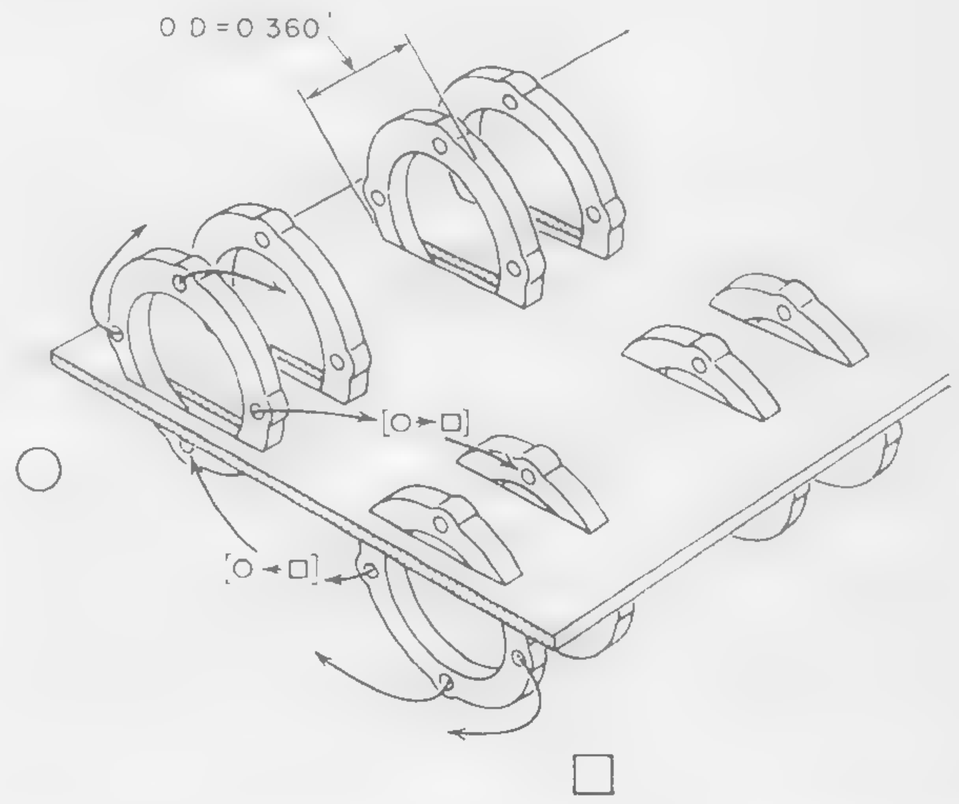



**Figure 7—Physical layout. The ○→□ transfer wiring is on one side of the board and the □→○ transfer wiring on the other. Note three apertures are available for maximum positive fan-out on each side of the board.**

## SESSION VII: Logic II

Chairman: G. B. B. Chaplin
Plessey Co., Ltd., Hants, England

### 7.1: 100-Mc Nonsychronous Esaki-Diode Computer Circuitry

J. R. Turnbull

IBM Corporation

Poughkeepsie, N. Y.

NONSYNCHRONOUS COMPUTER CIRCUITRY offers certain advantages over synchronous circuitry. Packaging problems are simplified since there are no phase relationships between *ac* supplies which dictate the physical relationships of circuits. In addition, the problems concerned with the design of *dc* power supplies and distribution systems are much simpler than those associated with multi-phase, high-frequency supplies.

One method of providing an *Esaki* diode circuit with a bilateral propagation characteristic is, of course, to use multi-phase power supplies. In lieu of this, we must employ some other circuit element, such as the transistor. When high speed is a fundamental objective, the choice of transistor configuration must be made with an eye to transient performance. The emitter follower is the fastest transistor configuration and, in addition, it provides much needed current gain. When an Esaki diode is driven by an emitter follower, as shown in Figure 1, we can achieve voltage gain and level setting action. The regenerative action of the negative resistance will improve rise times.

The voltage shift from input to output requires compensation, hence the compatible pair of circuits in Figure 1 uses two types of transistors. Since identical *npn* and *pnp* transistors are not easily obtained, another scheme would be advisable.

Figure 2 shows the *pnp* transistor replaced with an *npn* transistor and an appropriately chosen switching diode. The result is a block which provides an *AND-OR* function. The choice of *Esaki* diode is based primarily upon transient response requirements. However, since power dissipation is an important consideration, the best diode for this application will have a good $C/I_p$ ratio coupled with a low peak current. The resistor $R_1$ is chosen so as to optimize the gain.

In addition to the single *Esaki* diode shown in Figure 2, certain multiple diode combinations may be used. Figure 3 shows the *V-I* characteristic which may be obtained with a pair of diodes; note the improved linearity and greater voltage swing possible as compared with a single diode. Both these features make this combination attractive for use in the logic circuit described in Figure 2.

The inverter needed to build a complete system is shown in Figure 4. The basic inverter is formed by the *Esaki* diode as a load on resistor $R_1$. The emitter follower provides current gain, and resistors $R_2$ and $R_3$ provide compensation for the voltage drop through the transistor.

The severest problem with *Esaki* circuits is the tolerance buildup. To achieve more workable and practical circuits, a more realistic and less conservative design philosophy than an end-of-life approach is necessary. A statistical method of analysis, which chooses the parameters randomly, permits a reliable design without undue restrictions on device tolerances. Such a method has been used to obtain the parameter values used in these circuits.

*Esaki*-diode switching circuits have exhibited switching phenomena rarely seen in the past. Explanations for these phenomena are frequently best obtained from nonlinear analysis techniques using digital computers. The results of some programs* will be discussed.

In addition to the logic discussed, a unique binary trigger employing current feedback has been investigated. The elements inside the dashed line in Figure 5 form a reversible current source which is controlled by the output voltage. It flows into node *A* when the output is down, and out of node *A* when the voltage is up. This shifts the load line as shown, permitting binary operation when the input is pulsed.

Delays for these circuits have been measured in the 1-2 *ns* range, with repetition rates greater than 100 *Mc*. Fan-in and fan-out are heavily dependent on parameter tolerances. Fan-ins of 5 and fan-outs of 4 are possible under appropriate conditions.

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* IBM 704 and 610 were used for these programs.

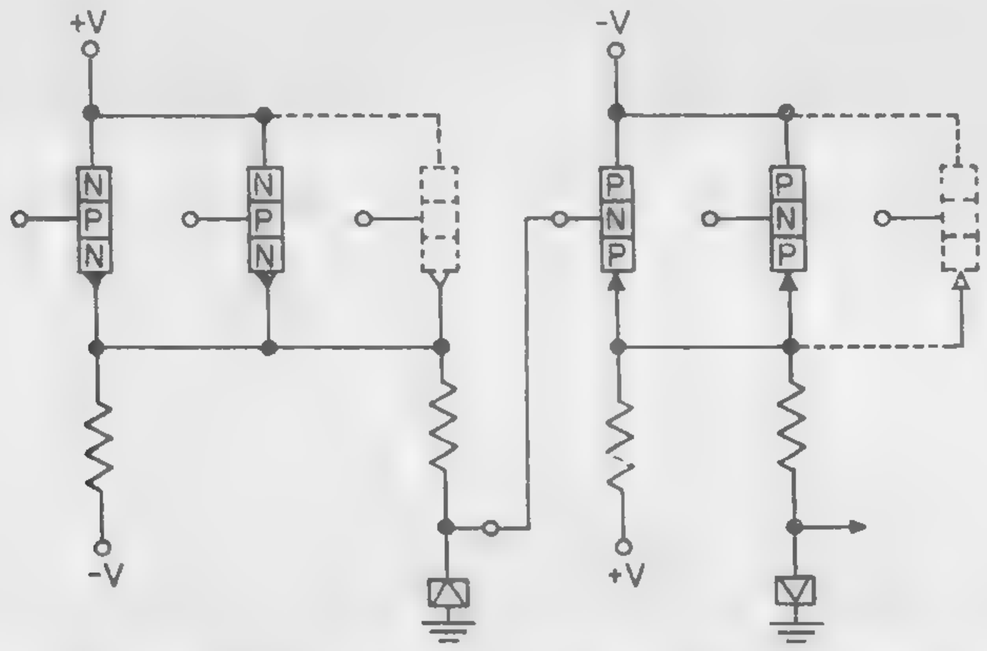


**Figure 1—Basic emitter follower *Esaki* diode logic circuit. Using two types of transistors results in compatible input and output levels.**

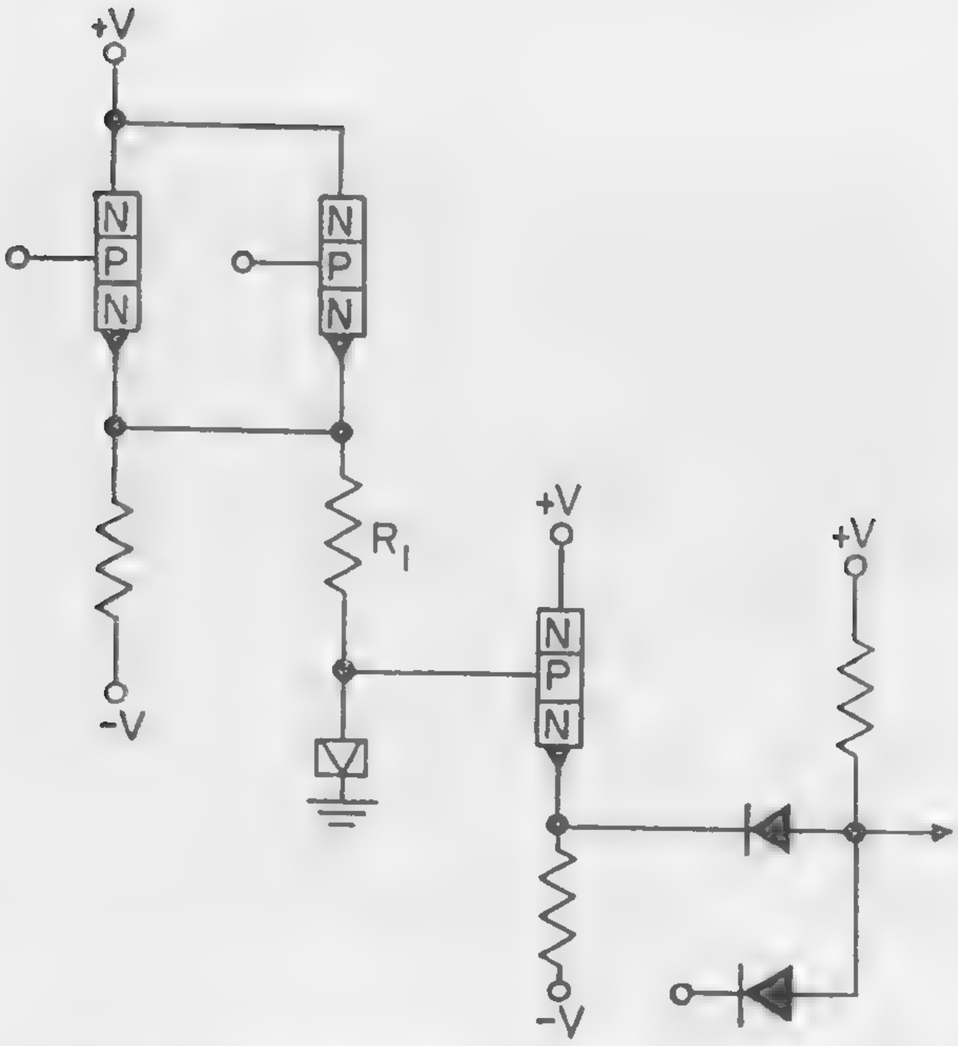


**Figure 2—Logic circuit using *npn* transistors. The *pnp* transistor has been replaced with a diode, with an emitter follower used to provide fan out to the diodes.**

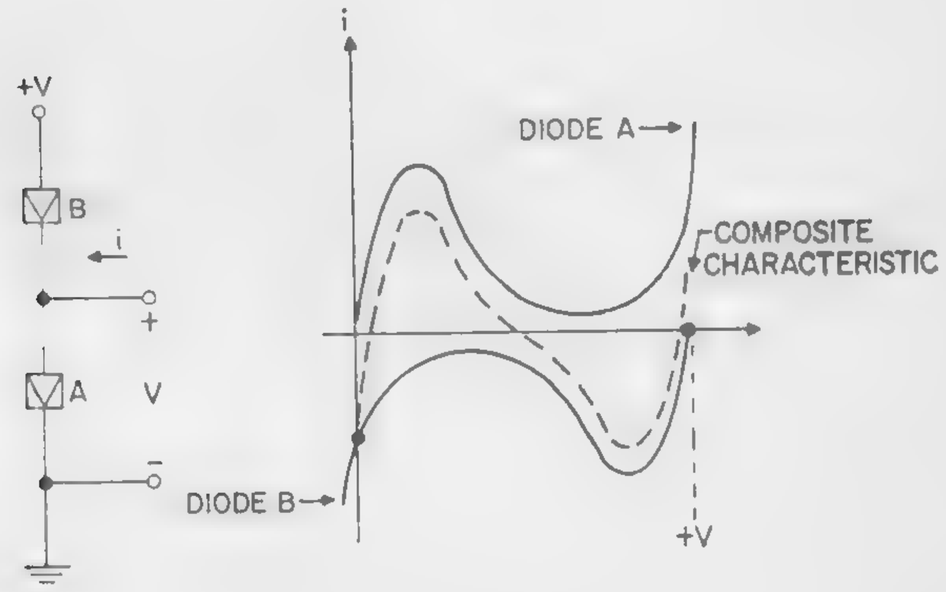


**Figure 3—The *V-I* characteristic of a pair of diodes. Note the improved linearity and greater voltage gain as compared to a single diode.**

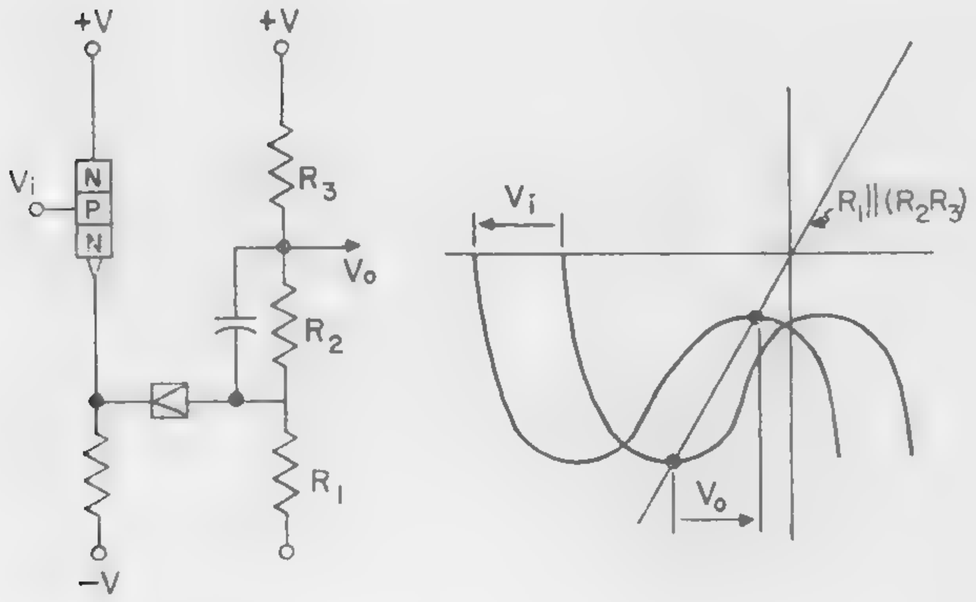


**Figure 4—Emitter follower *Esaki*-diode inverter. The load line on the resistor combination is the composite characteristic of the *Esaki* diode and the transistor.**

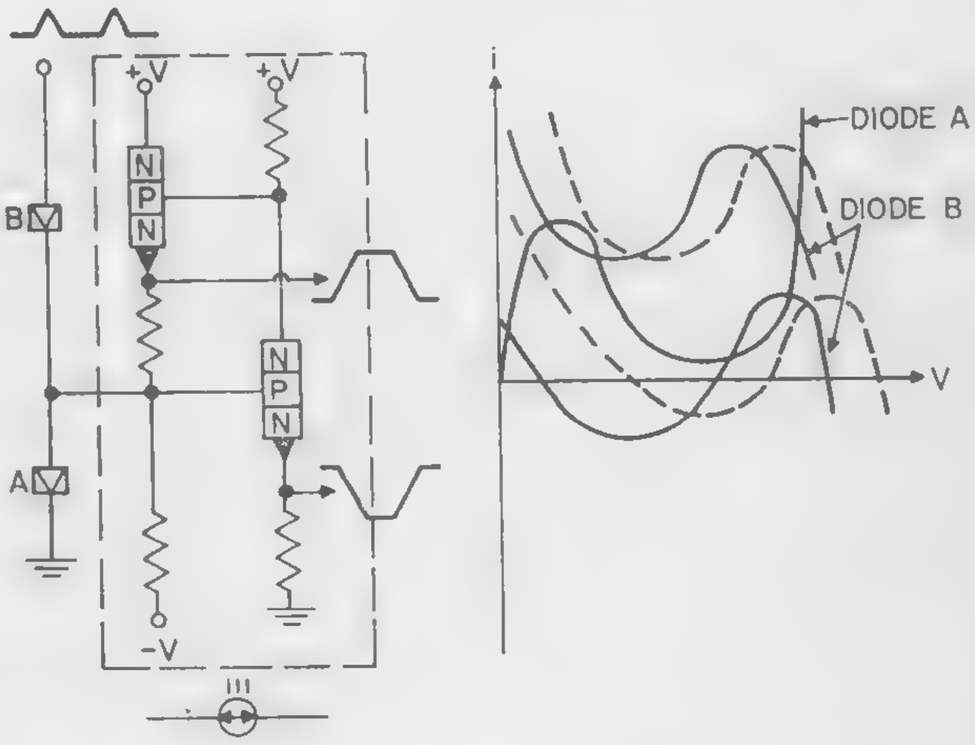


**Figure 5—High-speed *Esaki*-diode binary trigger. The elements inside the dashed line form a reversible current source which shifts the load line on the grounded *Esaki* diode so as to give binary action.**

## SESSION VII: Logic II

### 7.2: High Speed Switching Circuitry Using Tunnel Diodes

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Texas Instruments, Inc.

Dallas, Tex.

TUNNEL DIODE CIRCUITRY incorporating transistors has been used to gain advanced digital speeds while improving circuit reliability and stability. Major disadvantages in the use of tunnel diodes are: (*1*) Common input-output, (*2*) inability to obtain direct pulse inversion, (*3*) bi-directional flow of information, and (*4*) the difficulty of stage-to-stage coupling caused by loading and insufficient signal transfer. Circuitry using transistors as emitter followers accomplishes pulse steering and impedance transformation. Nanosecond pulse transformers and transistor amplifiers provide signal inversion and amplification. A combination of these techniques makes possible advances in digital circuit operational speeds.

A variable rate and amplitude clock pulser has been constructed providing pulses up to a 100-*Mc* repetition rate with an amplitude of 5 *volts* into 93 ohms at 100 *Mc*. Pulses from a 5 and 50-*Mc* pulse train are indicated in Figure 1. Pulse base width is less than *10 nanoseconds* from repetition rates less than 1 *Mc* to 100 *Mc*. Pulse width is variable from *8* to greater than *200 nanoseconds* with amplitude variable from 0 to 5 *volts*. Rise and fall times are *3* and *5 nanoseconds*, respectively. Figure 2 displays the output of a *10*, *50* and *100-nanosecond* square wave.

A binary stage capable of multistage coupling with input rates from single shot to greater than 100 *Mc* has been developed, and is shown in Figure 3. This stage, incorporating nanosecond pulse transformer signal inversion and amplification, and transistor pulse impedance transformation into the tunnel diode operating in the constant current mode, is capable of binary action in excess of 200 *Mc*. The speed limitation is dependent upon transistors and not tunnel diodes. The waveforms of a three-stage binary counter operative from an input rate of 100 *Mc* is indicated in Figure 4.

Shift registers capable of maximum shift rates of 45 *Mc* have been developed. These registers have been incorporated into ring counters of as many as ten stages. Signal inversion and amplification is accomplished by use of transformers with transistors performing steering and impedance transformation. A programmed pulse generator has been constructed based on two ring counters, one of three stages and the other of four stages, with their outputs gated in such a manner to provide twelve unique pulse times. These twelve pulses are then *OR*-gated together in any combination desired to provide a pulse envelope of the selected pulses. The output of the *OR* gate is amplified and provides a 3-*volt* maximum output into 93 ohms with approximately a 5-*nanosecond* rise and fall time. The gating is accomplished by normal transistor-diode digital logic operating at speeds up to 25 *Mc*. At present, for rates above 25 *Mc*, the gating circuits become unreliable, but with improved techniques or components the gating circuitry may be made more compatible with the maximum rates realizable in the tunnel diode circuitry. Pulse counters utilizing the 100 *Mc* binary and the ring counters described are possible, enabling one to count random pulses up to a *10-nanosecond* pulse separation.

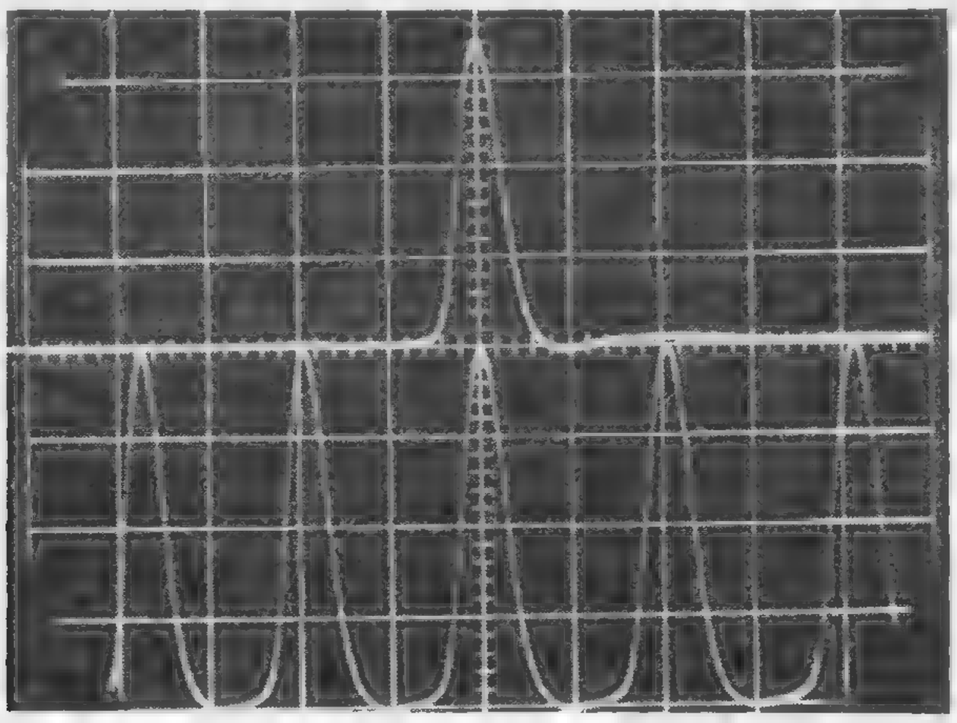

**Figure 1—Output of clock pulse generator; upper trace is 5 *Mc*, lower trace 50 *Mc*. Horizontal scale is 10 *nsec/cm;* vertical scale, 1 *v/cm*.**

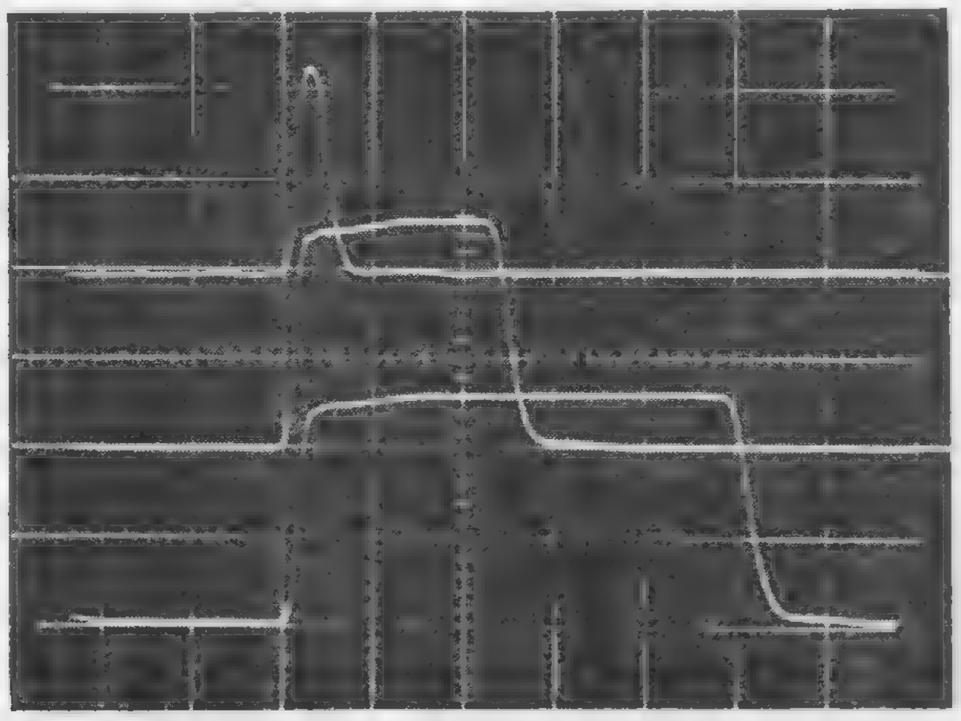

Figure 2—Output of variable pulse-width generator depicting pulse widths of 10, 50 and 100 *nsec*. Vertical scale is 2 *v/cm;* horizontal scale, 20 *nsec/cm*.

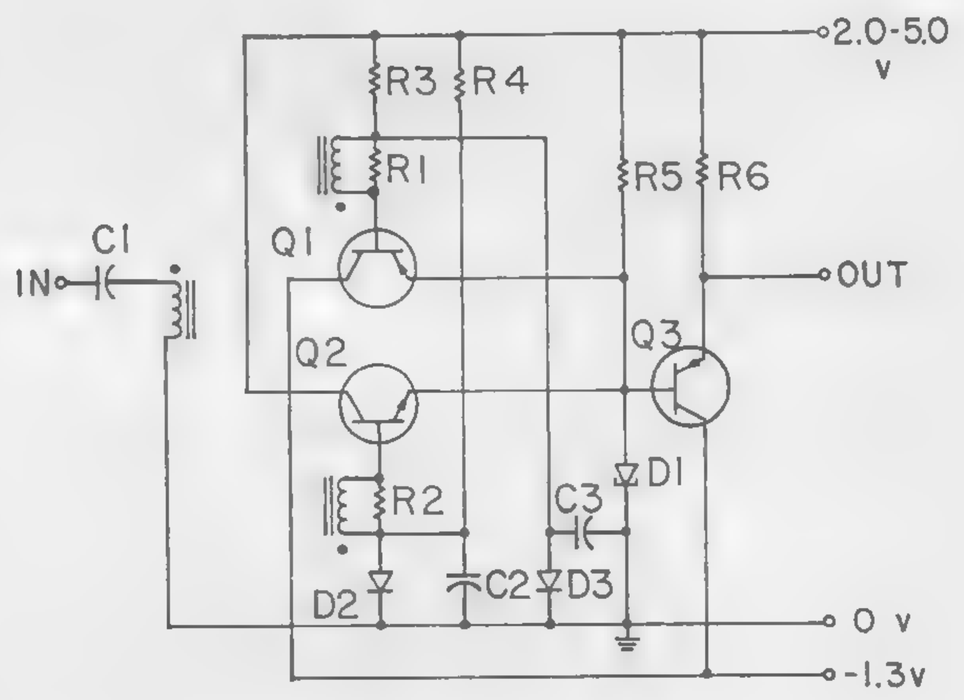


Figure 3—Circuit diagram of a 100-*Mc* tunnel-diode binary stage indicating use of transistor-transformer coupling.

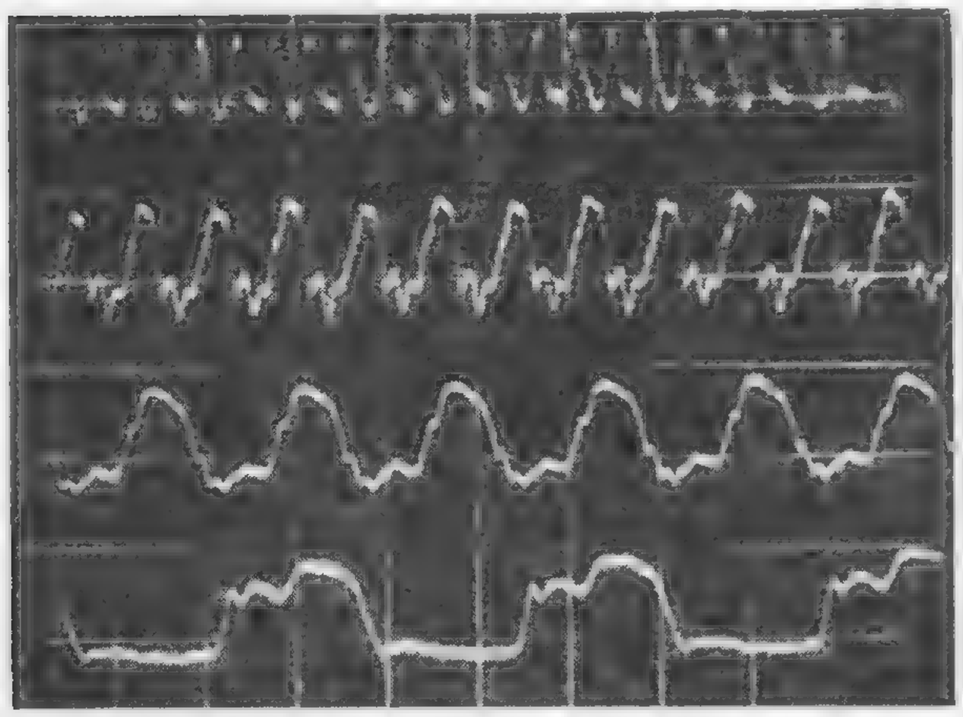

Figure 4—Output waveforms from three binary stages. Upper trace is the 100-*Mc* input to the first binary stage. Vertical scale is 1 *v/cm;* horizontal scale, 25 *nsec/cm*.

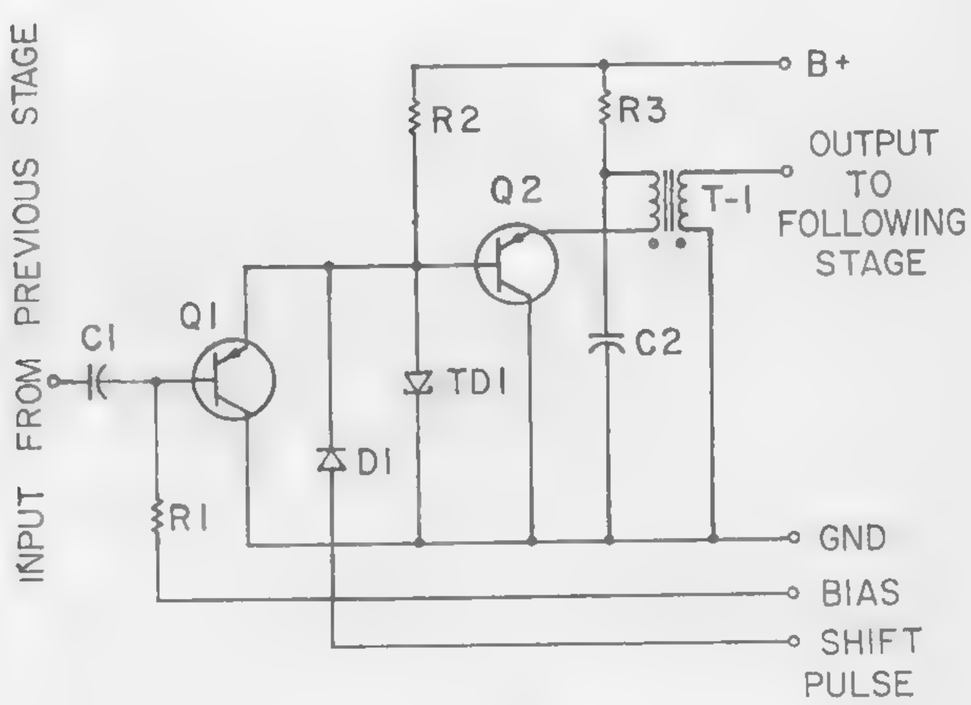


Figure 5—Circuit diagram of a single stage of a tunnel-diode shift register.

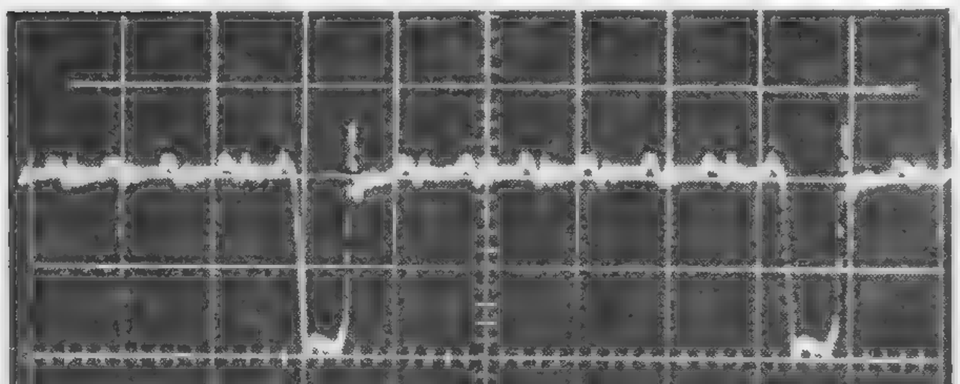

Figure 6—Output of an eight-stage shift register operated as a ring counter with the 30 *Mc.* shift pulse in the lower trace. Vertical scale is 5 *v/cm;* horizontal scale, 50 *nsec/cm*.

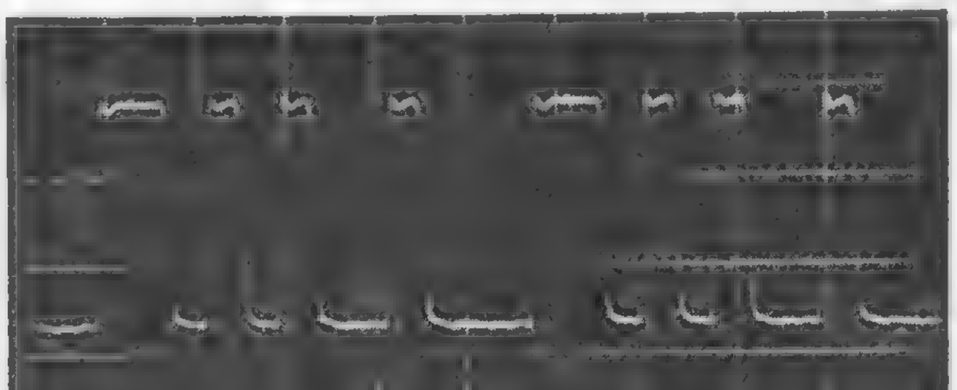

Figure 7—Output of a programmed pulse generator with twelve pulse times before repeating. The upper trace represents the two occurrences of the programmed pulse pattern with a horizontal scale of 100 *nsec/cm*. The lower trace is a single pulse output with the horizontal scale at 10 *nsec/cm;* vertical scale, 1 *v/cm*.

## SESSION VII: Logic II

### 7.3: Rapid-Transfer Principles for Transistor Switching Circuits

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Research Div., Philco Corporation

Philadelphia, Pa.

In digital systems series of binary elements are represented by continuous waveforms with inherent quantization in time and binary value. As waveforms are transmitted through logic circuits, quantization deteriorates; consequently, the waveforms must be requantized at intervals.

Figure 1 illustrates the process of requantization when binary elements are represented by signal levels. First, the poorly quantized waveform is requantized in amplitude and then combined with the clock pulse, or time standard. The resulting binary elements are stored for a clock period to provide the completely requantized waveform.

In a practical system, parallel requantization is necessary to permit combination of the requantized elements in logic circuits. Prior to requantization, parallel waveforms usually are misaligned in time as illustrated in Figure 2. Before storing the binary values, an interval of time equal to the misalignment or dispersion must elapse so that the value of each waveform will be correct. The maximum binary rate is equal to the reciprocal of the minimum binary-element duration, *M*, defined in Figure 2. For high binary rates, both the dispersion and the time to store a binary element must be small.

Current mode circuits[1] possess definite advantages over voltage-mode circuits in minimizing both dispersion and the time required to store a binary element. When only the parallel, current-mode configuration is used, however, a definite disadvantage exists, the requirement that circuits be cascaded to perform complete requantization.

A requantizing circuit using only the parallel confiuration is shown in Figure 3. Here, the clock pulse and binary elements are first combined in gates external to the flipflop; the combined elements are then stored in the flipflop in a second operation. This cascade of operations not only produces delay through the circuits but also permits dispersion to develop.

A rapid-transfer principle surmounts these difficulties by accomplishing requantization in a single stage, through the use of series-parallel gates. In the rapid-transfer circuit, illustrated in Figure 4, the flipflop transistors, $Q_1$ and $Q_2$, and the clock transistor, $Q_3$, form a three-way current switch. When $Q_3$ is *off*, the flipflop is stable; but when $Q_3$ is turned *on*, the switch current, $I_s$, is routed through one of the pullover transistors, $Q_4$ and $Q_5$, according to the applied binary inputs. Thus, complete requantization is accomplished by switching a single current. All transistors are kept from saturating by the voltage translating network, *T*, in their collector circuits.

Stability in a current-mode flipflop generally is obtained by driving a transistor into cutoff. The time required to bring a transistor out of cutoff increases both the dispersion and the time required to store a binary element. By introducing a high-speed diode into the emitter circuit of each transistor and providing a small bias current to keep each transistor conducting, as shown in Figure 5, the transistors are used as linear elements. The cutoff function is then transferred to the high-speed diodes. The input capacitance of the transistors is thus reduced and their average gain-bandwidth product increased.

A test system* was constructed employing the requantizing circuit** of Figure 5. It consists of a two-count ring counter driving a commutating switch, as illustrated in Figure 6. The commutating switch provides binary elements to remote requantizing circuits through coaxial cables.

Waveforms at the outputs of the ring counter and *circuit 3* for two binary rates are shown in Figures 7 and 8. The test system operates at clock rates up to 250 *Mc*.

* Transistors used were *MADT's*, type L-5447, made by the Lansdale Tube Division of Philco.

** The high speed diodes were silicon, type D-4121, made by Sylvania.

[1] Yourke, H. S., "Millimicrosecond Transistor Current-Switching Circuits," *Transistor and Solid-State Circuits Conference;* 1957.

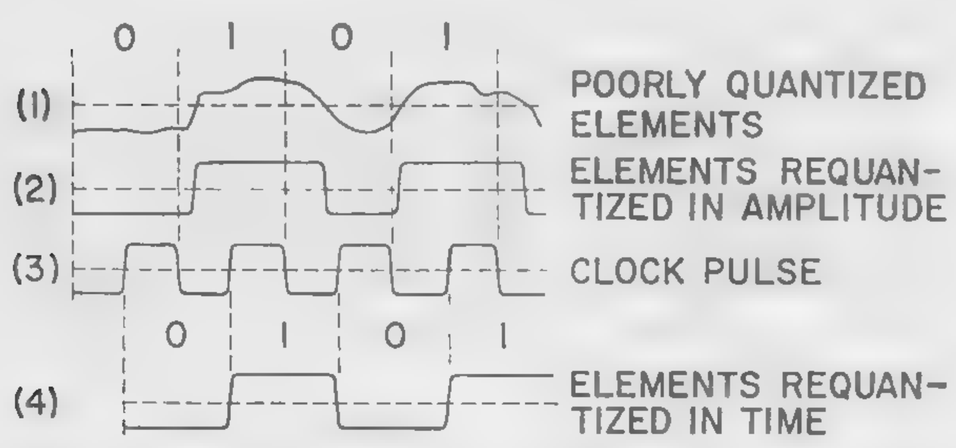



**Figure 1—Requantization of waveforms. The poorly quantized waveform in line *1* is requantized in amplitude (line *2*) and then stored by the clock pulse to produce the completely requantized waveform of line *4*.**

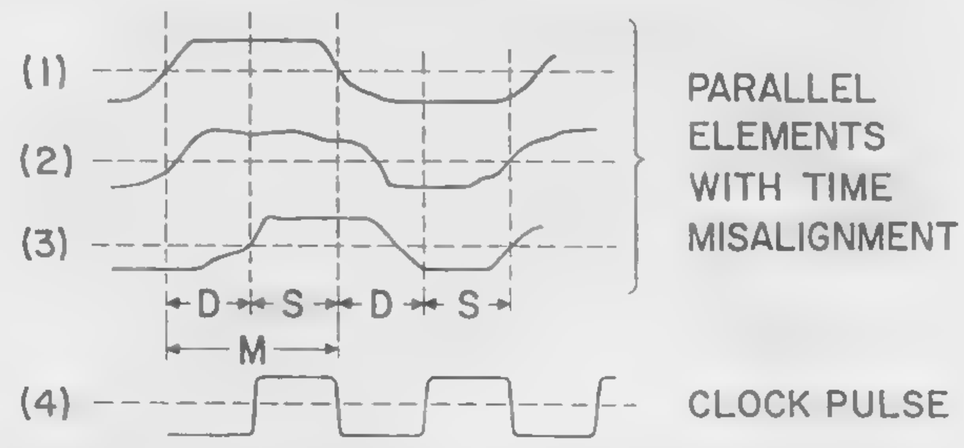



**Figure 2—Importance of dispersion in determining minimum binary-element duration.**

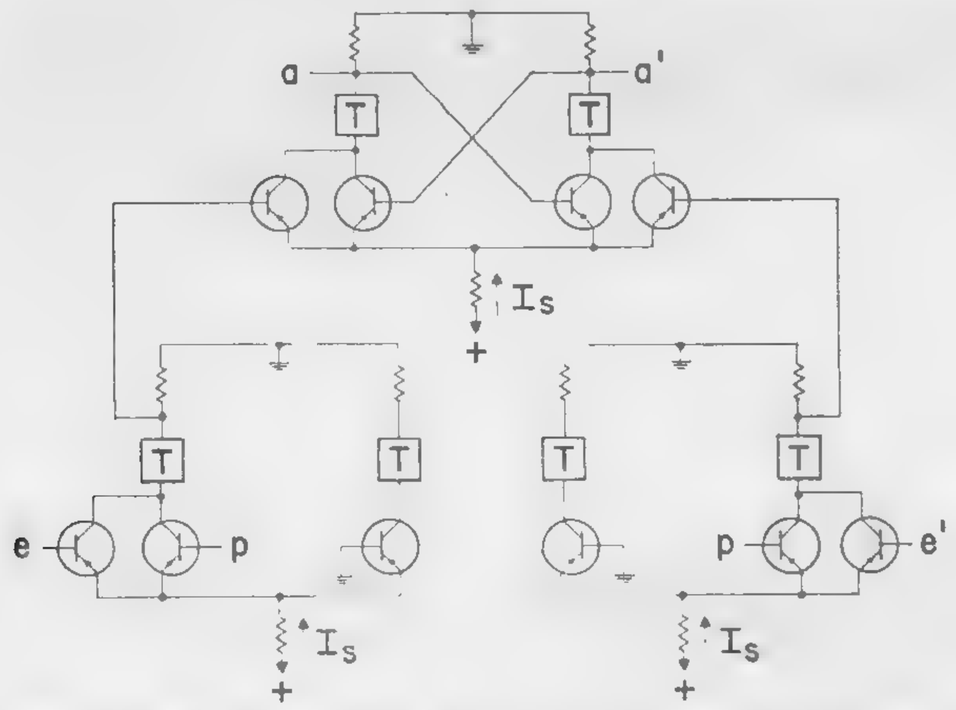



**Figure 3—Requantizing circuit using only the parallel transistor configuration.**

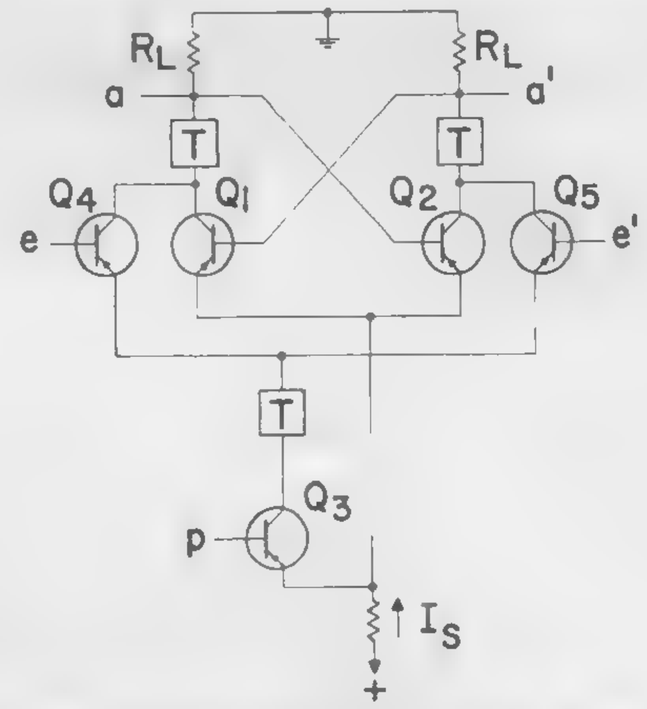
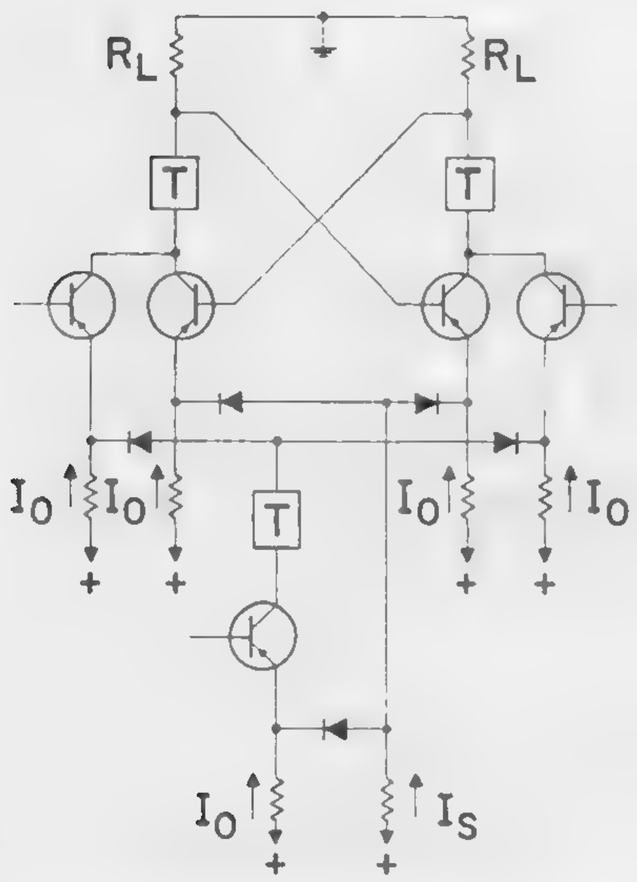



**Figure 4—The rapid-transfer circuit. Flipflop transistors, $Q_1$ and $Q_2$, and clock transistor, $Q_3$, form a three-way current switch. The clock transistor, when turned *ON*, routes the switch current, $I_s$, to one of the pull-over transistors, $Q_4$ and $Q_5$.**



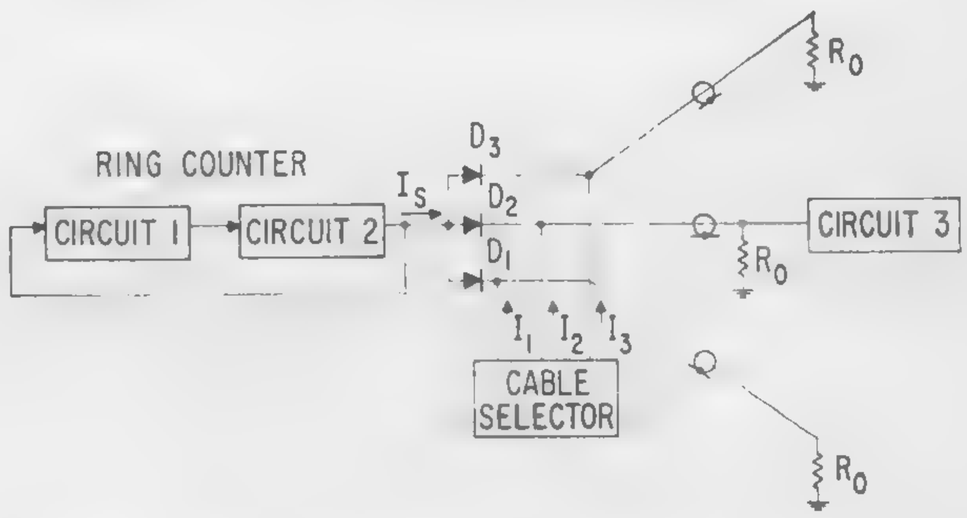




**Figure 5 (*left*)—The rapid-transfer circuit with cutoff prevention. The addition of high-speed diodes and auxiliary current sources, $I_o$, keeps the transistors in their linear regions.**

**Figure 6 (*above*)—A test system. The two-count ring counter generates alternate *ONES* and *ZEROS* which are transmitted to remote locations by coaxial cables. Circuits *1*, *2*, and *3*, are rapid-transfer requantizing circuits.**

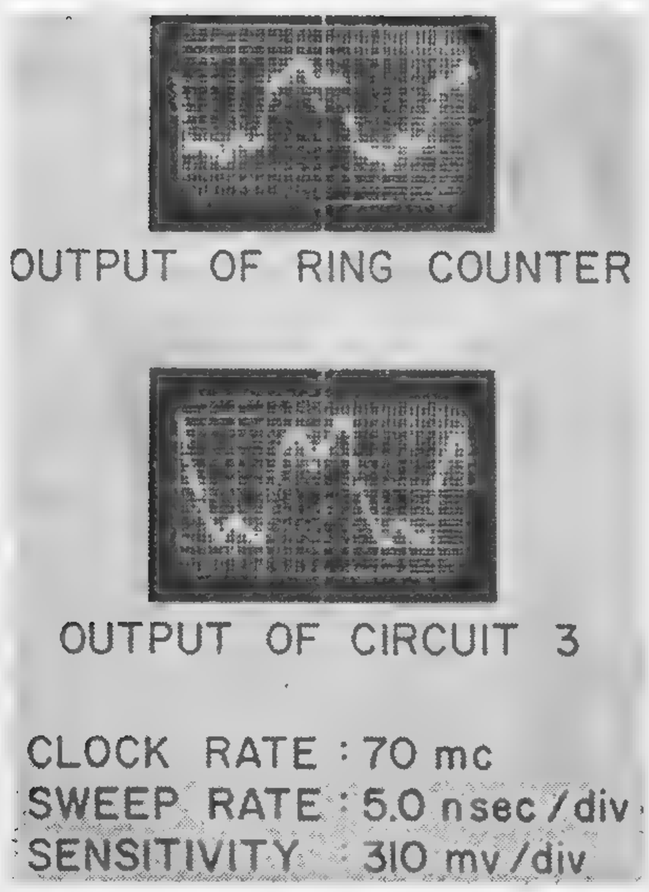



**Figure 7—Waveforms of the test system at a clock rate at 70 *Mc*. Both the output of the ring counter and the output of the remote requantizing circuit show the notch indicating transition of current from pull-over to flipflop transistors.**

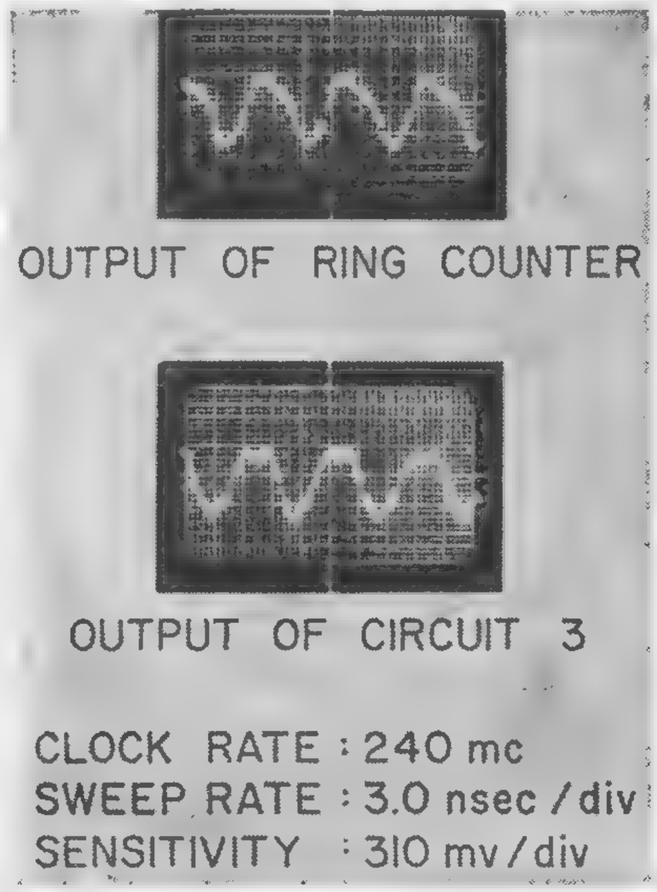



**Figure 8—Waveforms of the test system at a clock rate of 240 *Mc*. The notch, characteristic of requantization by a rapid-transfer circuit, is evident in the output of circuit *3*.**

## SESSION VII: Logic II

### 7.4: Determination of Switching Speed of Transistors by Stored Charge and Effective Lifetime

**Y. C. Hwang, D. S. Cleverley and D. J. Monsour**

Semiconductor Products Dept., General Electric Company

Syracuse, N. Y.

By postulating the equations, Figure 1, one can obtain equations relating the switching time to $T_a$, $T_b$, $Q_B$ and $Q_C$. $T_a$ and $T_b$ are the effective life times in the active and the saturated status, respectively. $Q_B$ and $Q_C$ are the charges corresponding to the current dependent base charge gradient and the voltage dependent depletion layer in the collection junction respectively. The sum of $Q_B$ and $Q_C$ is defined as $Q^*_B$. Under special conditions, the relations of rise time and storage time to the parameters can be reduced to simple forms by which the parameters $T$ and $Q$ can be measured.

*Measurement Results*

The results of these measurements substantiate the validity of the postulations fairly well over a range of bias conditions and for various types of transistors. $Q^*_B$, the total charge needed to bring a transistor to the edge of saturation, can be measured using the circuit of Figure 2. The peak of the output waveform, dependent on the amount of charge instantaneously inserted into the base, will reach saturation when the calibrated capacitor is just enough so that $(V_{in}—V_{BE})C$ equals $Q^*_B$ (100%). The same process can be used to measure $Q^*_B$ for any collector current and voltage changes. The plots of $Q^*_B$ (100%) versus $I_C$ for constant $V_{CC}$ for different types of transistors, shown in Figure 3, supply more direct information for switching prediction than do small signal parameters.

$T_a$ is measured in a circuit as shown in Figure 5*a*. In this circuit with a constant $I_B$ drive and using a low-impedance collector load[1], the collector current rises exponentially with a time constant equal to $T_a$. $T_b$ is measured as shown in Figure 6. The change of $t_S$ divided by the logarithm of the ratio of two input voltages is equal to $T_b$.

From the experimental results shown it is seen that (*1*) $Q_B$ is linearly proportional to $I_C$, (*2*) $Q_C$ approximately varies according to $V_{CB}{}^{1/n}$, (*3*) at moderate current and voltage levels both $Q_B$ and $Q_C$ are significant for medium speed transistors, while $Q_B$ is much less than $Q_C$ in very high-speed transistors, and (*4*) $T_a$ and $T_b$ for medium-speed transistors are one order of magnitude larger than those of high speed transistors. The charge stored in the emitter junction can be measured as shown in Figure 4. The emitter junction charge versus negative bias voltage is thus obtained regardless of the non-linearity of the capacitance itself.

It is evident that for improving transistor switching characteristics $Q_C$, $Q_E$, and $Q_B$ must be minimized for specified $V_C$, $V_E$, and $I_C$ changes. $T_b$ must be minimized and $T_a$ must be optimized. Specific examples are given to show the correlation of predicted and calculated values. $T_a$ and $T_b$ are the values restricting the range of application of these approximations.

[1] Tektronix current probe.

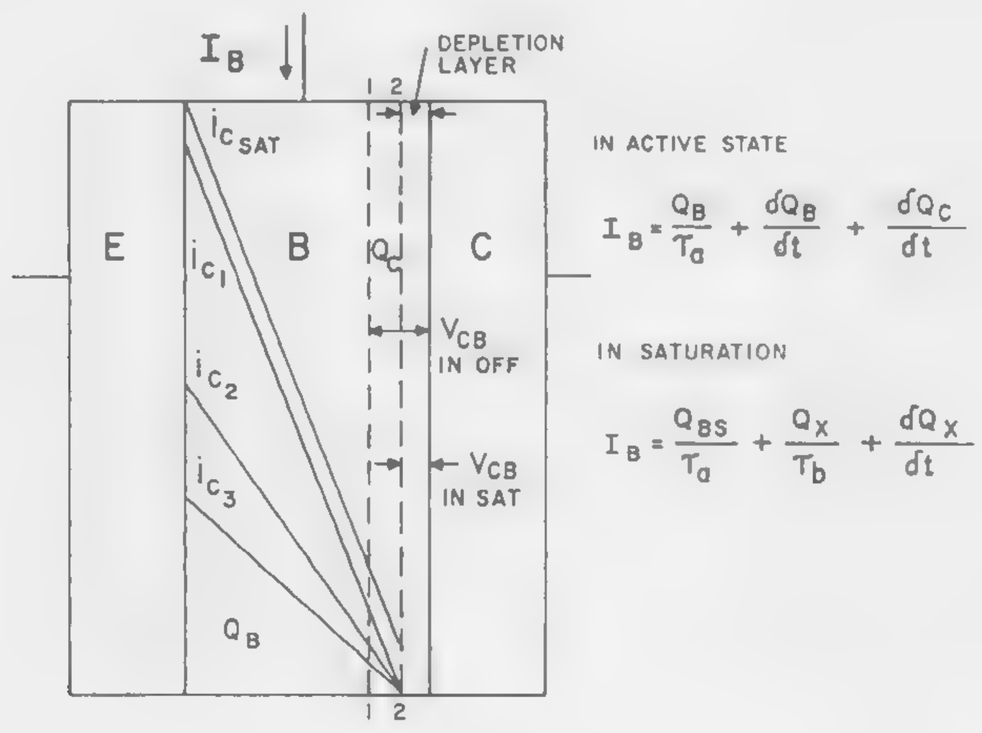



**Figure 1—Charge distribution in the base region and collector depletion layer.**

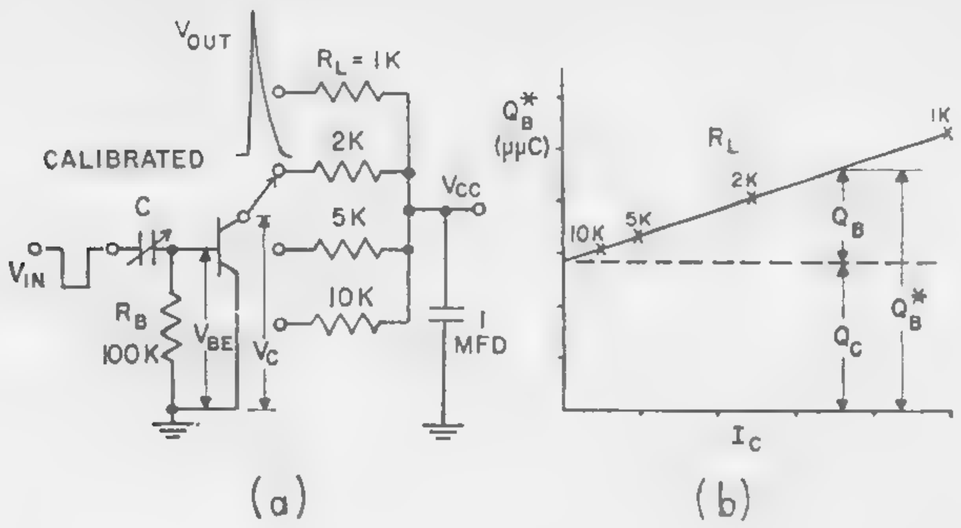



**Figure 2—*(a)* Circuit of measuring charge; *(b)* sample plot of $Q_B^*$ ($=Q_B + Q_C$) versus $I_C$.**

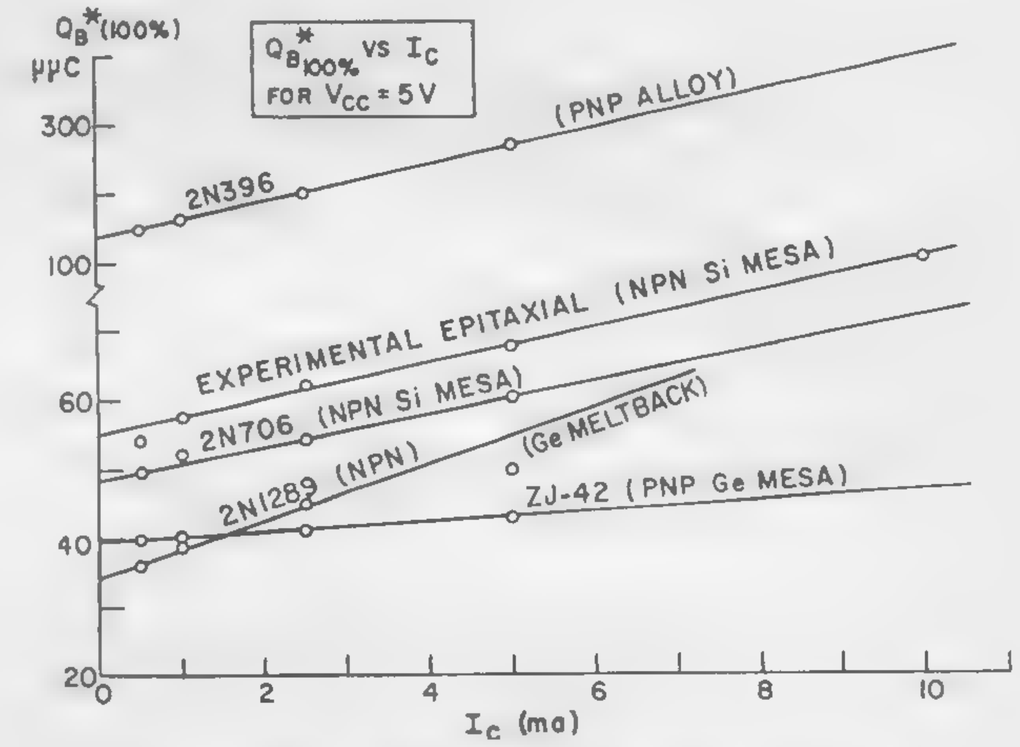
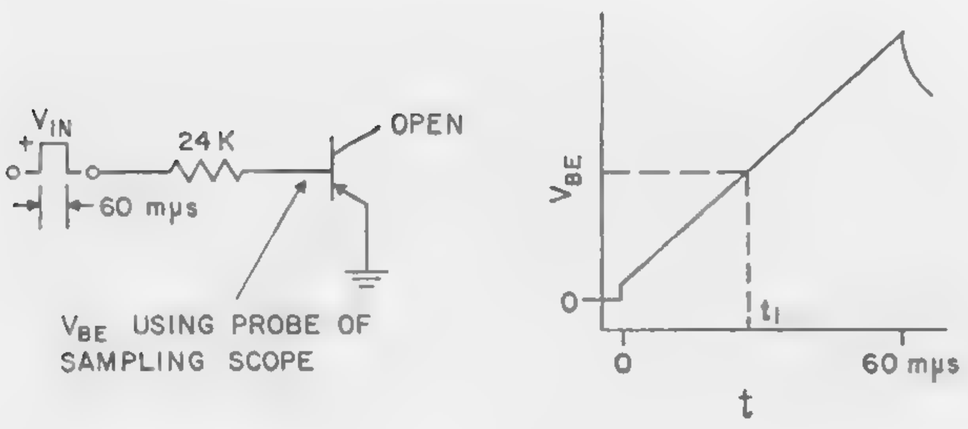



**Figure 3—Base storage charge versus collector current for typical transistors at a specified collector voltage change.**




$$Q_E \text{ (to } V_{BE}) = \int_0^{V_{BE}} C_E \, dV \cong \int_0^{t_1} \frac{V_{IN}}{R} \, dt \quad \text{if } V_{IN} >> V_{BE}$$

**Figure 4—Circuit for measurement of emitter charge and relation of $Q_E$ to $V_{BE}$.**

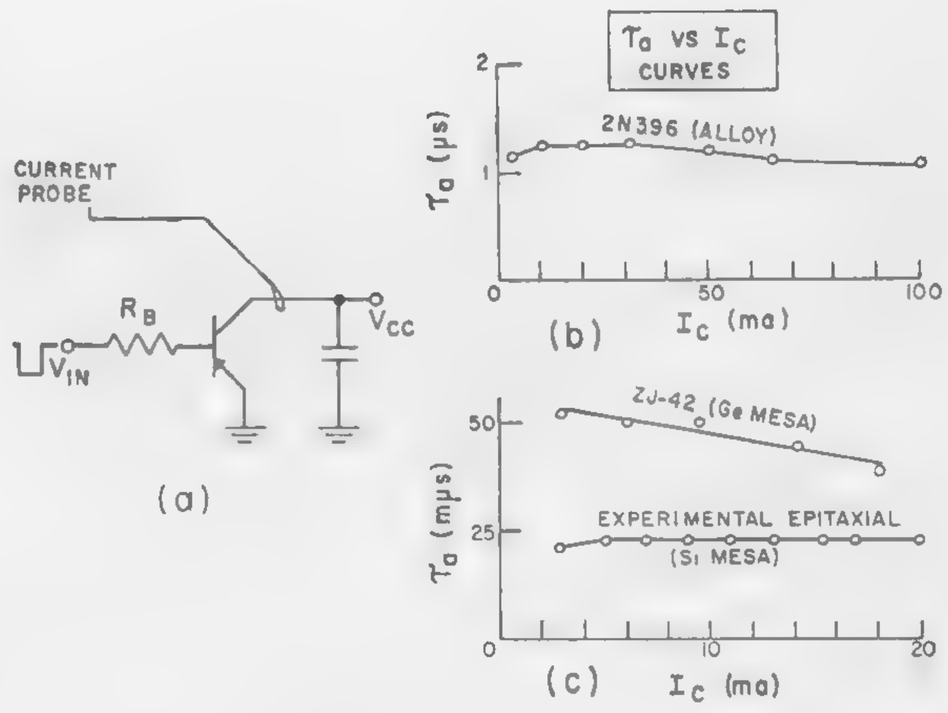



**Figure 5—*(a)* Circuit for measurement of $\tau_a$. In *(b)* and *(c)* are curves for $\tau_a$ versus $I_c$; *(b)* is for medium-speed alloy transistor *2N396*, and *(c)* for high-speed transistors, germanium mesa ZJ-42 and epitaxial silicon mesa.**

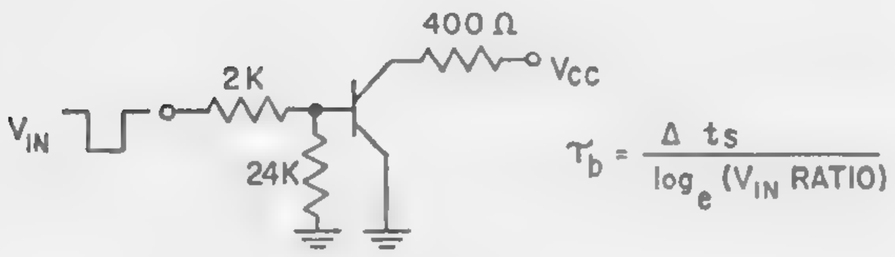



**Figure 6—A circuit for measurement of $\tau_b$ is shown in *(a)*. Plot of $\Delta t_s$ versus log (input voltage ratio). indicating that $\tau_b$ is constant over a wide range for transistors shown, appears in *(b)*.**

$$t_{d\,(\text{TO } 10\%\ I_{CS})} = \frac{Q_E}{I_{B1}} + \frac{1/9\ Q_B^*\big|_{0\%}^{90\%}}{I_{B1}}$$

$$t_{r\,(10\%\text{ TO }90\%)} = \frac{8/9\ Q_B^*\big|_{0\%}^{90\%}}{I_{B1} - \frac{Q_B}{2\tau_a}}$$

$$t_{f\,(10\%\text{ TO }90\%)} = \frac{8/9\ Q_B^*}{-I_{B2} + \frac{Q_B}{2\tau_a}}$$

$$t_s = \tau_b \log_e \left(1 + \frac{Q_x}{\tau_b (I_{BS} - I_{B2})}\right) + \frac{Q_B^*\big|_{90\%}^{100\%}}{-I_{B2}}$$

$$\text{where } Q_x = \tau_b (I_{B1} - I_{BS}) \left[1 - \text{Exp}\left(-\frac{t_{pulse} - t_r - t_d}{\tau_b}\right)\right]$$

**Figure 7—Approximate expressions for switching time with constant current base drive.**

## SESSION VII: Logic II

### 7.5: Continuous Phase Regenerative Logic*

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Philadelphia, Pa.

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THE PARAMETRIC DEGENERATIVE AMPLIFIER exhibits the property that its gain is maximum when the pump and the input signal phase have zero or $\pi$ phase difference. This binary phase preference may be used to generate a binary code whose *ONES* and *ZEROS* are represented by a continuous sine wave, each distinguished by a phase reversal. This scheme is particularly attractive, because it allows a logical bit rate as high as half the frequency of the pump source. The circuit to be described performs logic at a 100-*Mc* rate using a pump frequency of 200 *Mc*. Typical waveforms of this signal are shown in Figure 1. Obviously, considerable bandwidth is required to cause a complete phase reversal of a continuous wave within one cycle. A bandpass characteristic with a normalized bandwidth of unity allows almost complete regeneration of the second half of a bit after occurrence of a phase several in the input code.

To develop an operational logic gain element, the circuit must, in general, have all of the following properties: Ability to perform logic, retiming, thresholding, and limiting and to provide power gain, bandwidth, isolation between inputs, and directionality of information flow.

When a parametric degenerative amplifier is used to perform amplification and retiming on the described binary coded signal, it appears that the mode of operation is more precisely described as one of reactive switching. The parametric diodes used are in a state of large or small capacitance with the transition taking place within a voltage range of 0.1 volt. The reactance switch is capable of excellent retiming and has some power gain. The latter is limited by the required bandwidth.

Threshold may be obtained by performing majority logic using analog addition logic in either a resistor or transistor matrix. Figure 2 shows the resultant output obtained by adding the various combinations of three input signals. The phase of the output is the same as the phase of the majority of the input signals. The output signal has a threshold equal to the magnitude of one input.

Figure 2 also shows that a limiter is entirely indispensable to achieve standardization of output signal amplitude. Isolation between inputs and directionality of information flow may be obtained by the use of suitable transistors in the information path.

A circuit fulfilling all the necessary functions of a logic gate except limiting is shown in Figure 3. Limiting must be accomplished in an external circuit. The circuit operates with a 200-*Mc* pump and a bit rate of 100 *Mc*. A complete analysis of the circuit may be carried out making the following assumptions:

(*1*) The characteristic of the diode is that of a reactive switch, i.e., a nonlinear capacitance, as shown in Figure 4. As confirmed by experimental results, the capacitor is assumed to act predominantly as a reactive switch.

(*2*) The transformer is of the transmission-line type and is close to ideal, even if not terminated, provided the length of the windings is short compared to one-quarter wavelength.

(*3*) Each of the inputs are applied to the circuit through a transistor which acts as a constant current source loaded by the collector capacitance of the three transistors.

The circuit exhibits the following properties:

(*1*) The output voltage is half the difference of the two diode voltages:

$$e_1 = \frac{1}{2}(e_{C2} - e_{C1})$$

(*2*) The diode capacitances $C_1$ and $C_2$ are in their high-capacitance state during approximately the first three quarters of each cycle of the pump voltage. During this time the capacitor voltage is practically constant and consequently, no output is generated. The instant at which the diode capacitance returns to the small value is dictated by the magnitude of the signal charge. The polarity of the input charge dictates which diode returns to zero first. During the last quarter of the pump cycle one diode capacitance is small and one large, effectively unbalancing the circuit and gating the pump voltage to the output. Thus, the output pulse is in synchronism with the pump which causes the retiming of the output pulse.

(*3*) When the input current level is kept below a certain critical value, both diodes will return to zero charge at the end of a pump cycle; the diodes are unbiased. Otherwise, one diode will retain some charge which affects its performance during the next cycle. Interaction between pulses occurs in this case.

A representative example of circuit performance taken from a computer simulation is shown in Figure 5. Shown are pump voltage, input signal current, capacitor and output voltages for the following signal code:

*1 0 1 0*

The output indicates that, for the particular signal current level, output pulses of uniform size are generated and are properly timed.

* The work described here was performed under Bureau of Ships Contract number NObsr 81444.

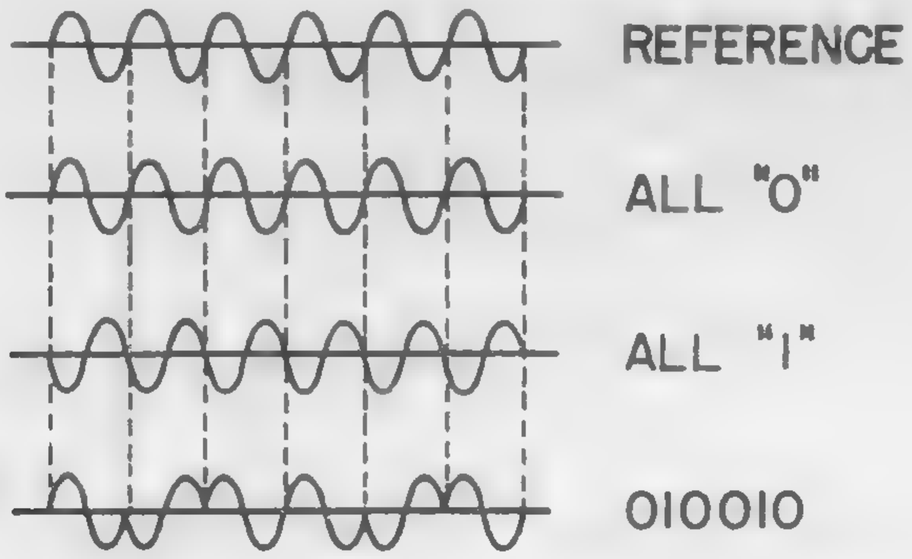


Figure 1—Waveforms illustrating signal construction.

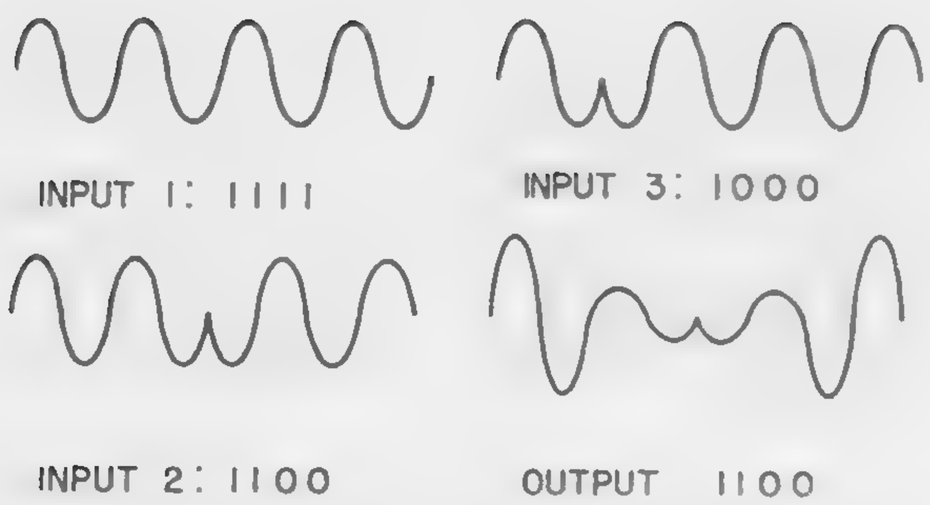


Figure 2—Majority logic by analog addition.

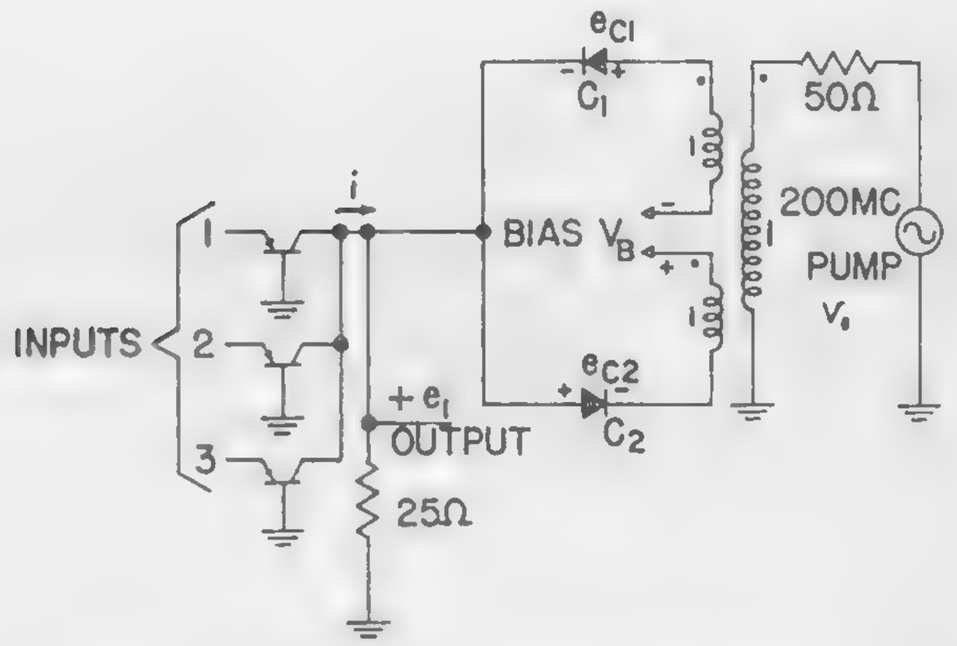


Figure 3—Continuous phase regenerated logic gate.

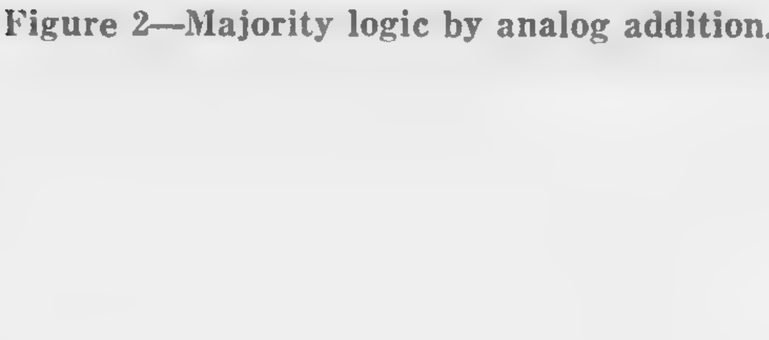


Figure 4—Characteristic of reactive switch parametric diode.

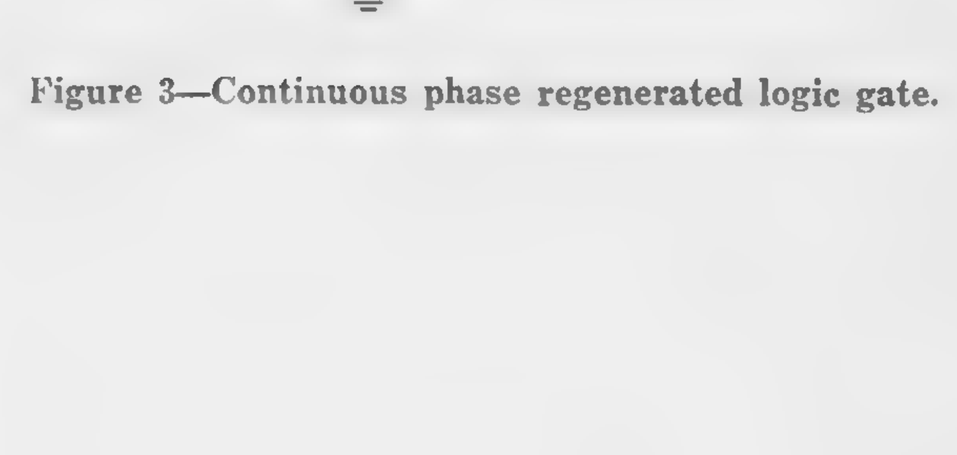


Figure 5—Circuit response of logic gate.

## SESSION VIII: Microwave Applications

Chairman: A. Uhlir, Jr.

Microwave Associates, Inc., Burlington, Mass.

### 8.1: PIN Diodes for Protective Limiter Applications*

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Murray Hill, N. J.

N. G. Cranna

CBS Electronics, Inc.

Stamford, Conn.

A *pn* JUNCTION IN A SEMICONDUCTOR has a voltage dependent microwave impedance which acts as a high-*Q* capacitor at low incident power levels, and as a low impedance at high power levels. Junction diodes are thus capable of protective limiter action[1], and properly designed devices have actually been found to limit successfully over a restricted power range (up to a few watts)[2].

Protection over a considerably larger power range can be achieved using the *PIN* structure, consisting of a high resistivity (*I*) layer between *N* type and *P* type regions; this results in low-capacitance per-unit-area, and hence at a given impedance level, permits use of larger area diodes with high-burnout power levels. Like the simple *pn* junction, the *PIN* diode acts essentially as a high-*Q* capacitor at low level. At high level the *I*-layer resistivity is greatly reduced by conductivity modulation, resulting in a low overall resistance. A practical protective limiter circuit consisting of a pair of *PIN* diodes and a shunt tuning inductance is illustrated in Figure 1, accompanied by equations for insertion loss at low and high signal levels.

The small signal characteristics of the *PIN* diode have been calculated assuming a simple step-type impurity distribution (Figure 2), in which heavily doped *N* and *P* regions, possessing a small but finite resistance, are separated by a uniform, high resistivity *P*-type region ($\pi$ layer). Because of its high resistivity, a substantial portion of the $\pi$ layer adjacent to the $N^+$—$\pi$ junction is swept free of carriers (depletion layer). The remaining unswept portion of the $\pi$ layer has a dielectric relaxation frequency of the order of 100 *Mc*, and is thus essentially capacitative at much higher frequencies, and resistive at low frequencies. Equivalent circuits corresponding to this structure and applicable at microwave frequencies are shown in Figure 3, and a low-frequency equivalent circuit is shown in Figure 5.

It will be noted that at microwave frequencies, the diode capacitance is independent of the space charge width $w$, and hence independent of bias voltage, to the extent that the high $Q$ approximation holds. In contrast, the low-frequency capacitance decreases with increasing reverse bias voltage until the $\pi$ layer is completely swept free of carriers ($w = t$).

As a direct test of the equation for low-level loss (Figure 1), measured values of *lll* are plotted against measured values of $R_0Q_0^2$ (Figure 6). The agreement with theory (represented by the solid line) indicates reasonable validity for the microwave measurement technique.

A knowledge of $\pi$ layer resistivity $\rho$, as well as of diode dimensions, is needed to calculate low level parameters by means of the equations in Figure 4. A convenient means of measuring $\rho$ in the completed unit has been developed. Referring to Figures 4 and 5, one sees that the high-frequency equivalent series resistance (henceforth written $R_{HF}$) and the reciprocal of the low-frequency capacitance (henceforth written $C_{LF}$) are both linear functions of the space charge width $w$, which is, in turn, a function of bias voltage. In a plot of $1/C_{LF}$ versus $R_{HF}$ the slope at any point on the curve equals $-\epsilon\omega^2\rho$, where $\omega$ is the angular frequency at which $R_{HF}$ is measured; thus a point by point calculation of $\rho$ can be made. Figure 7 illustrates such plots for two diodes; the calculated resistivities are approximately 2000 ohm-cm for unit (*a*), and 10,000 ohm-cm for unit (*b*).

The high level (protection) performance of limiter diodes can be measured more reliably by direct tests in the system[3].

A qualitative check on the high level equivalent circuit (Figure 1*c*) has been obtained from small signal impedance measurements on diffused diodes at 20 *ms* forward *dc* bias. The impedance is purely resistive and is of the order of 0.3 ohm. In present devices, experiments indicate that at incident pulse power levels of several hundred watts, the equivalent resistance is somewhat larger than the value quoted. Nevertheless, values of high level protection better than 27 *db* have been obtained for an incident power of 300 watts on a diffused *PIN* pair.

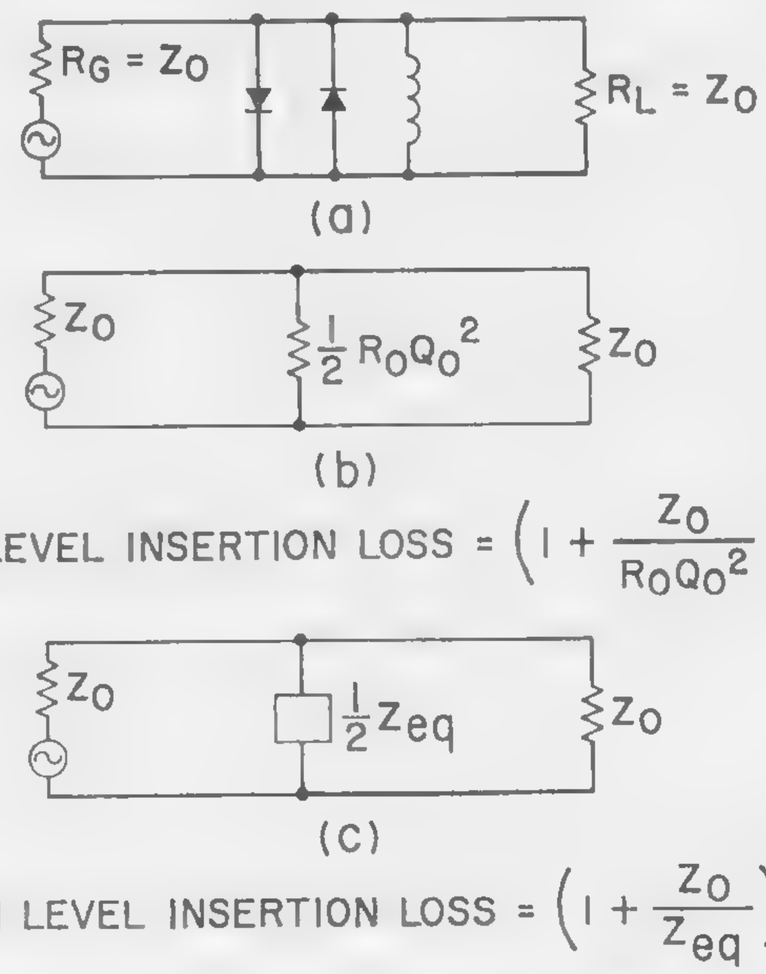



**Figure 1—*(a)* Schematic of protective limiter circuit; *(b)*, low-level equivalent circuit; *(c)*, high-level equivalent circuit.**

* This work was supported in part by the U. S. Army Signal Corps under contract DA 36-039-sc-73224.

[1] Uhlir, Jr., A., "The Potential of Semiconductors in High Frequency Communications," *Proc. IRE*, 1099-1115; June, 1958.

[2] Bakanowski, A. E., "Some Thermal Considerations in the Design of Graded Junction Silicon Varactor Diodes of the Mesa Type," *Ninth Interim Report, Microwave Solid State Devices*, U. S. Army Signal Corps Contract DA 36-039-sc-73224; May 15, 1959.

[3] Cranna, N. G., "Diffused Silicon PIN Diodes as Protective Limiters in Microwave Circuits," *Tenth Interim Report, Microwave Solid State Devices*, U. S. Army Signal Corps Contract DA 36-039-sc-73224; August 15, 1959.

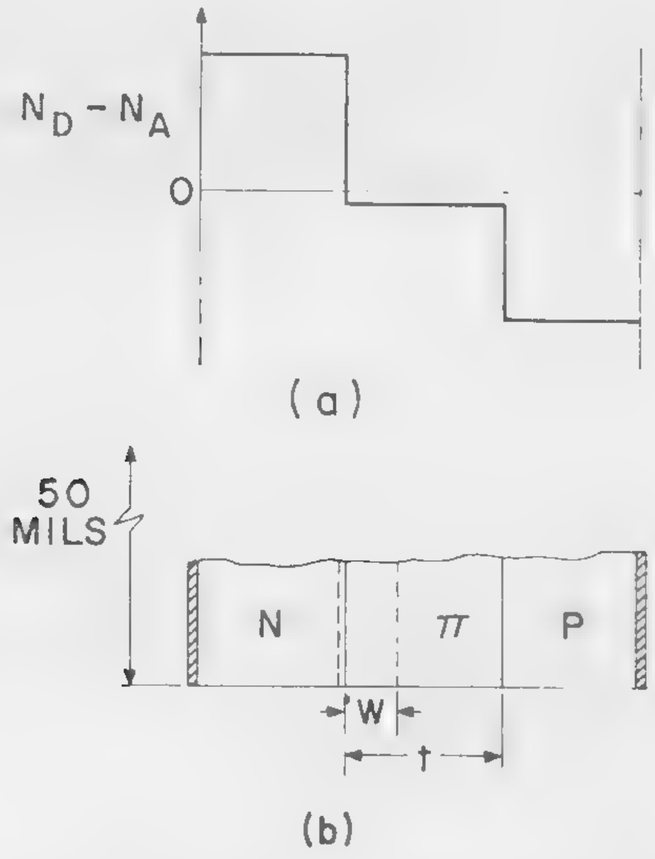



**Figure 2—*(a)* Assumed impurity distribution for *PIN* diode. In *(b)* is illustrated diode structure, showing heavily-doped regions and π region consisting of swept and neutral portions.**

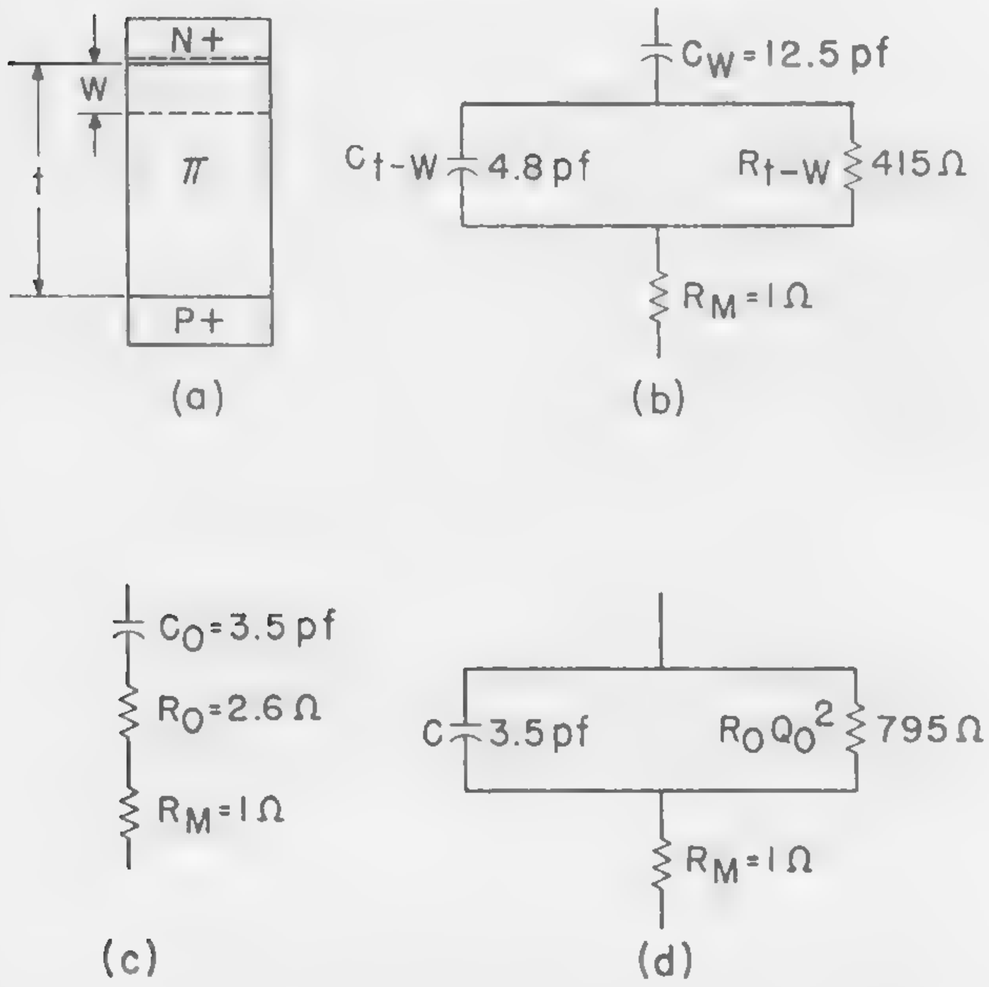
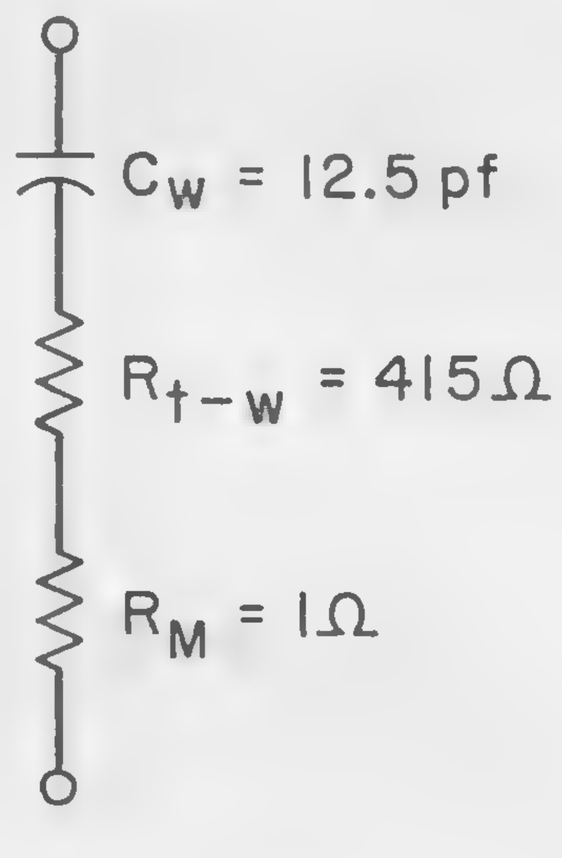



**Figure 3—Microwave equivalent circuits for the *PIN* diode. The values of circuit elements have been calculated from zero-bias impedance measurements; they agree fairly well with values calculated from the device structure assuming a π-layer resistivity in the neighborhood of 1800 *ohm-cm.***

$$C_0 = \frac{\epsilon A}{t} \qquad R_0 = \frac{t-w}{A\omega^2\epsilon^2\rho} + R_M$$

$$Q_0 = \frac{\omega\epsilon\rho}{1-\frac{1}{t}(w-\omega^2\epsilon^2 A\rho R_M)} \qquad R_0Q_0^2 = \frac{\rho\frac{t}{A}}{1-\frac{1}{t}(w-\omega^2\epsilon^2 A\rho R_M)}$$

**Figure 4—Equations for equivalent circuit parameters at microwave frequencies, in the high-Q approximation: $\omega\epsilon\rho >> 1$.**




$$C = \frac{\epsilon A}{W}$$

$$R = \rho\frac{t-w}{A} + R_M$$

**Figure 5—Zero bias equivalent circuit of the *PπN* diode for a frequency of 100 *kc;* numerical values obtained from impedance measurements at zero bias.**

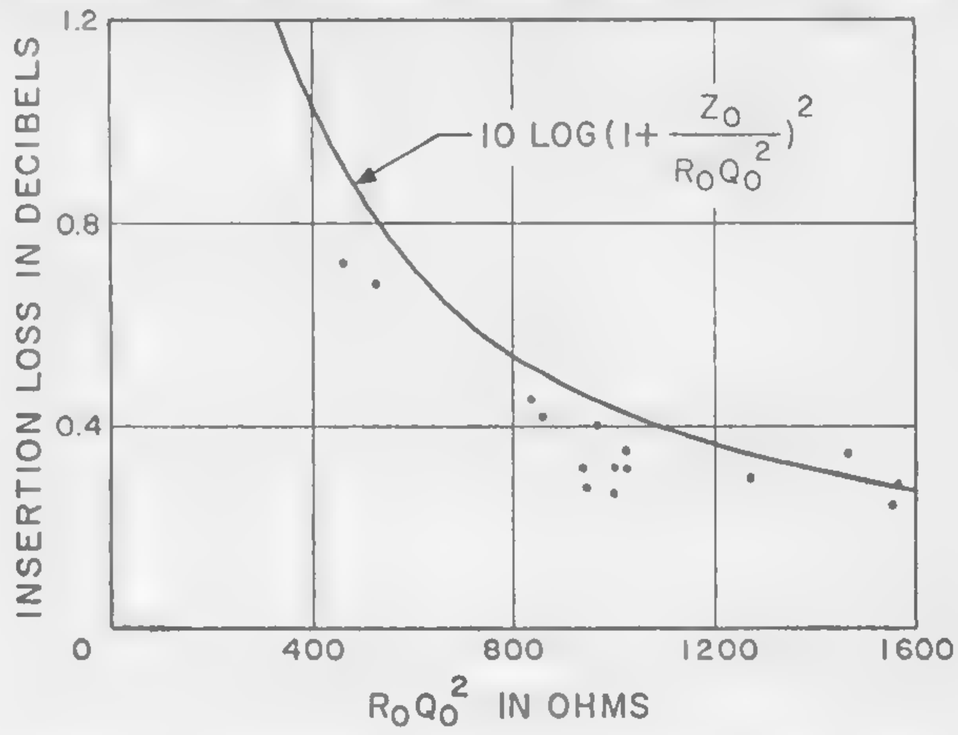



**Figure 6—Measured low-level insertion loss, for a pair of *PIN's*, versus average measured shunt resistance, $R_oQ_o^2$. Theoretical curve included for a comparison.**

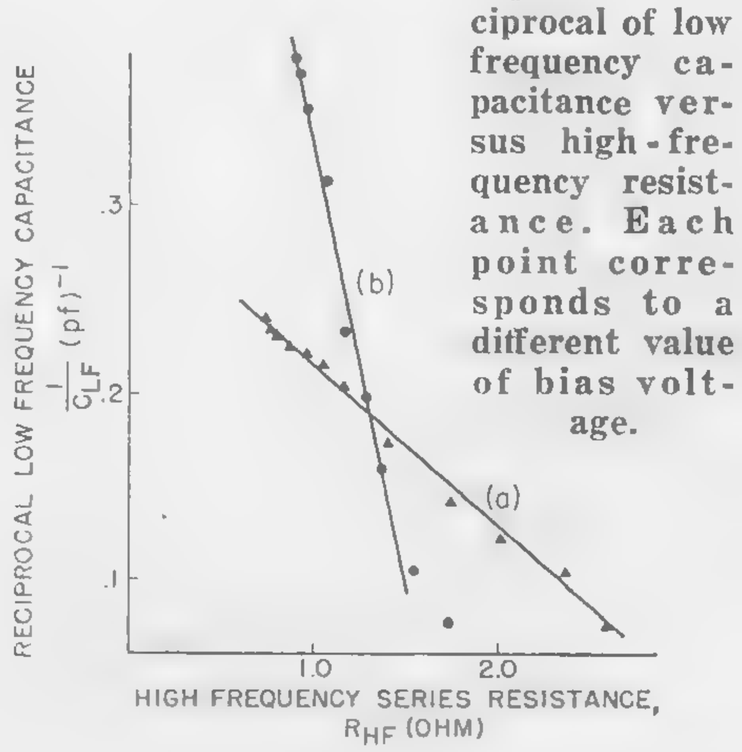



**Figure 7—Reciprocal of low frequency capacitance versus high-frequency resistance. Each point corresponds to a different value of bias voltage.**

## SESSION VIII: Microwave Applications

### 8.2: Low-Level Garnet Limiters

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Melville, L. I., N. Y.

WITH THE ADVENT of new types of low-noise microwave receivers, which saturate at relatively low power levels, new types of protective devices have had to be developed. This paper will discuss one such type of device, a garnet limiter, developed at *L*-band and *S*-band, with an exceedingly low-threshold limiting level.

A photograph of an *L*-band limiter with an adjustable permanent magnet is shown in Figure 1. The circuit arrangement follows the work of De Grasse[1]. It consists of two crossed-strip transmission-line half-wavelength resonators between common ground planes. These resonators are oriented at right angles to one another to obtain maximum decoupling between them. The resonators are open-circuited at both ends, so that there is an *rf* magnetic field maximum at the centers where the resonators cross. A 0.020-inch diameter sphere of single-crystal garnet material is placed between the strips. When the Yttrium Iron Garnet (YIG) is biased to ferrimagnetic resonance by means of the permanent magnet, it serves as the gyromagnetic coupling element between the resonators.

The driving *rf* magnetic field in the input resonator will cause the electron spins in the *YIG* to process about the *dc* field, thereby inducing an *rf* magnetic field in the output resonator. Thus, almost all the *rf* power is coupled to the output, via the tightly-coupled *YIG* sphere, which behaves as a miniature resonator having a very high unloaded *Q*. Due to the tight coupling, the bandwidth of the device is substantially greater than the linewidth of the *YIG*.

The device behaves as a triple-tuned preselector having limiting properties due to non-linear effects within the ferrite, which are enhanced by proper choice of frequency, geometry and ferrite parameters[2]; Figure 2. When the *rf* power level is increased beyond a critical level, non-linear coupling to (and hence parametric excitation of) lower-frequency spin-waves propogating within the ferrite will occur[3]. The excitation of these spin-waves prevents the increase of the precession angle of the electron spins beyond a sharply defined threshold and hence limits the power-transfer capability of the *YIG* sphere.

The limiting thresold has been found to be quite sharp and occurs in the *S*-band limiter near 3 Microwatts; the power output has a plateau that extends over more than a 25-db change in input power beyond the critical level.

Insertion loss of the S-band limiter is 0.6 db at low signal levels, and the 3 Db bandwidth is 60 *Mc*. Off-band rejection is 20 db at 40 *Mc* from center frequency. Several units can be cascaded, if desired.

As Figure 2 indicates, for low-level limiting at 1200 *Mc* using pure *YIG*, required is an oblate ellipsoid of revolution, having the following demagnetizing factors: $N_s = 0.670$ and $N_t = 0.165$. Such a geometry did not give satisfactory results.

A better approach was the use of a garnet sphere having a reduced saturation magnetization (1000 gauss), giving a limiter with a theoretical operating range from 950 to 1900 *Mc*.

Single crystals of *Ga-YIG*[4] having a saturation magnetization of 1000 gauss, which when ground and polished into spheres showed a very narrow line width. Low-level limiting was successfully obtained using this material. A plot of the magnetic susceptibility as a function of power level is shown in Figure 3. It has the same sharp break as pure *YIG*, and the decline has the $\sqrt{P}$ dependence predicted by *Suhl*[3].

The measured limiting-threshold power level was —21 dbm; 8 microwatts. The operating band over which limiting was obtained extended from 1000 to 1500 *Mc*. The characteristics of the *L*-band crossed-resonator limiter are shown in Figure 4. An insertion loss of 1.1 db was obtained at the center frequency; 1305 *Mc*. The 0.2- and 3-db bandwidths for fixed magnetic field are 8 and 43 *Mc*, respectively; *swr* is 1.06 at center frequency.

The output-power versus input-power characteristic is shown in Figure 5, and indicates a dynamic range greater than 25 db. The *swr* is also plotted as a function of the input-power level. The reflected portion of the incident power increases sharply as the input power is raised indicating good power handling capability. The remainder of the input power is dissipated in the spin waves within the garnet. A leading-edge spike 100 millimicrosecond long was also observed.

---

[1] DeGrasse, R. W., "Low-Loss Gyromagnetic Coupling Through Single-Crystal Garnets," *Journal of Applied Physics*, p. 115-156; 30, 1959.

[2] LeCraw, R. C., Spencer, E. G., and Porter, C. S., "Ferrimagnetic Line Width in Yttrium Iron Garnet Single Crystals," *Physical Review;* June, 1959.

[3] Suhl, H., "Non-Linear Behavior of Ferrites at High Microwave Signal Levels," *IRE Proceedings*, p. 1270-1284; October, 1956.

[4] LeCraw, R. C., and Spencer, E. G., "Line Width Narrowing in Gallium Substituted Yttrium Iron Garnet," *Bulletin of American Physical Society*, p. 85; January, 1960.

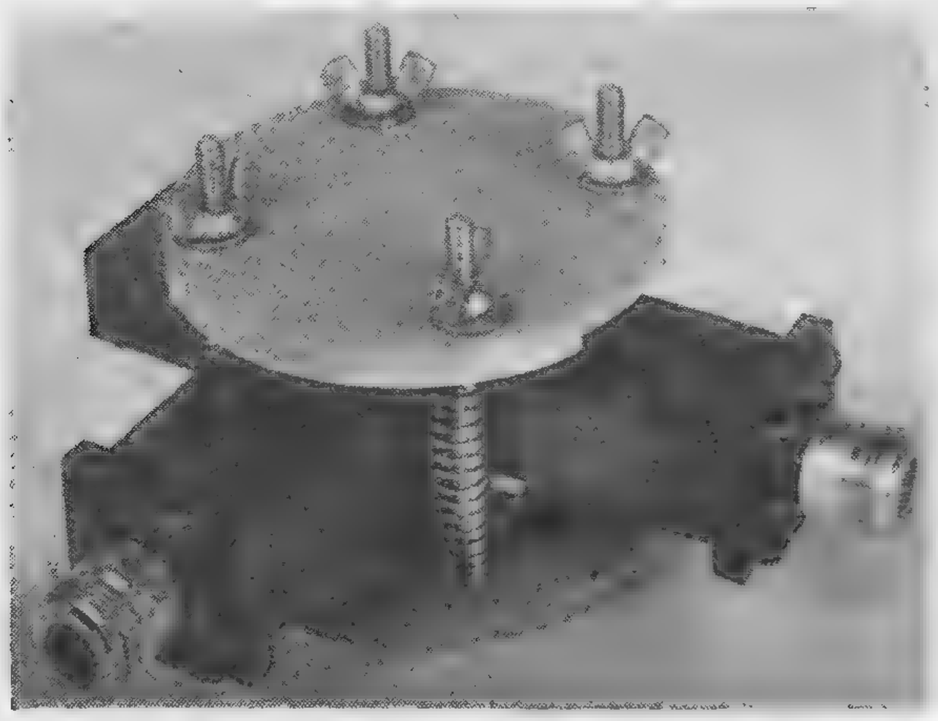

Figure 1—*L*-band limiter, shown with adjustable permanent magnet.

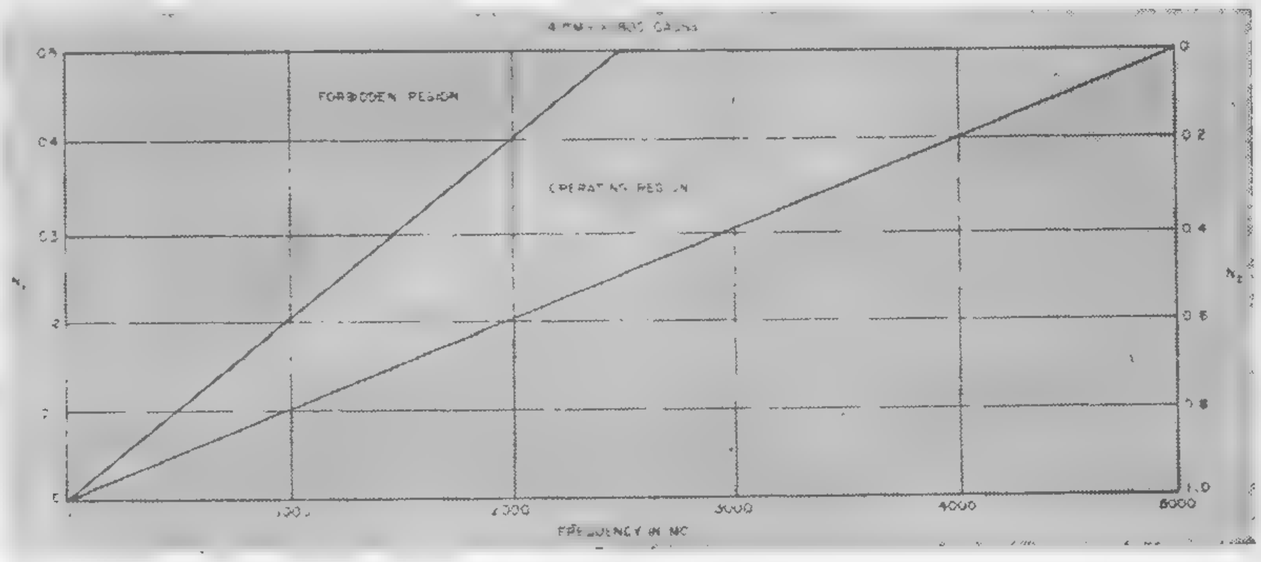


Figure 2—Frequency region for low-level limiting as a function of ferrite geometry for *YIG*.

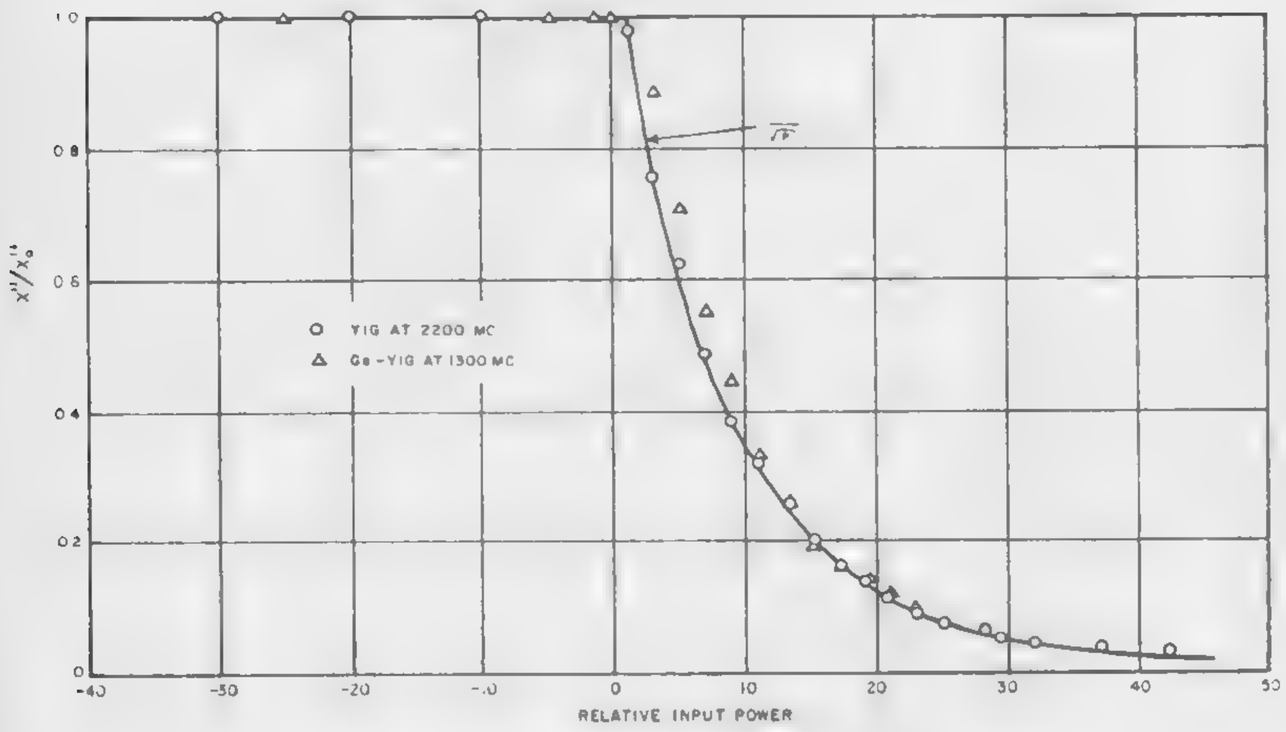


FIGURE 3. MAGNETIC SUSCEPTIBILITY OF YIG AND Ga-YIG SPHERES AS A FUNCTION OF INPUT-POWER LEVEL

Figure 3—Magnetic susceptibility of *YIG* and *Ga-YIG* spheres as a function of input-power level.

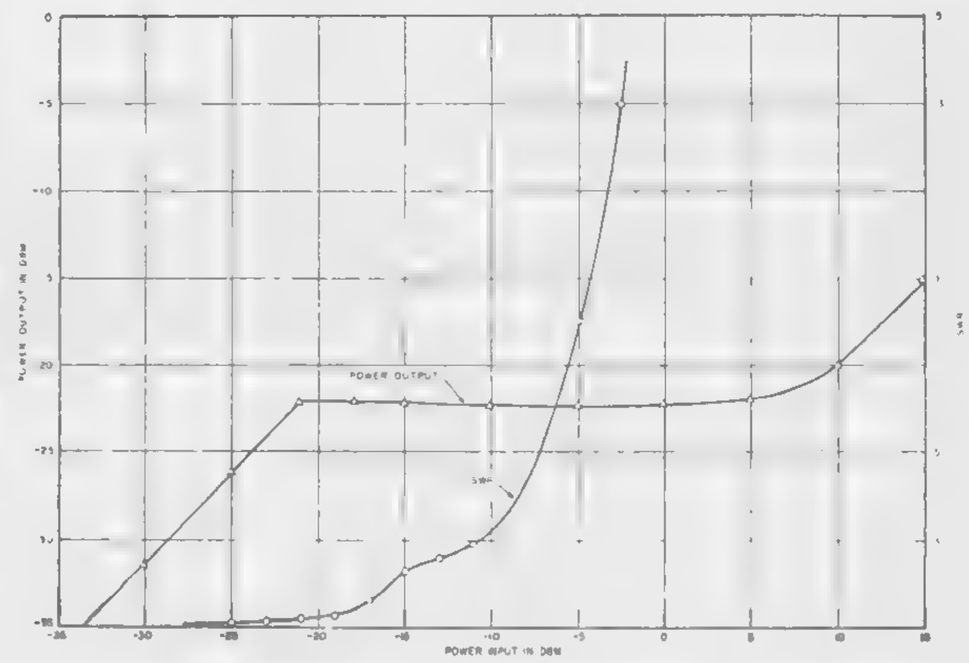


Figure 5—Transmission characteristics of *L*-band limiter.

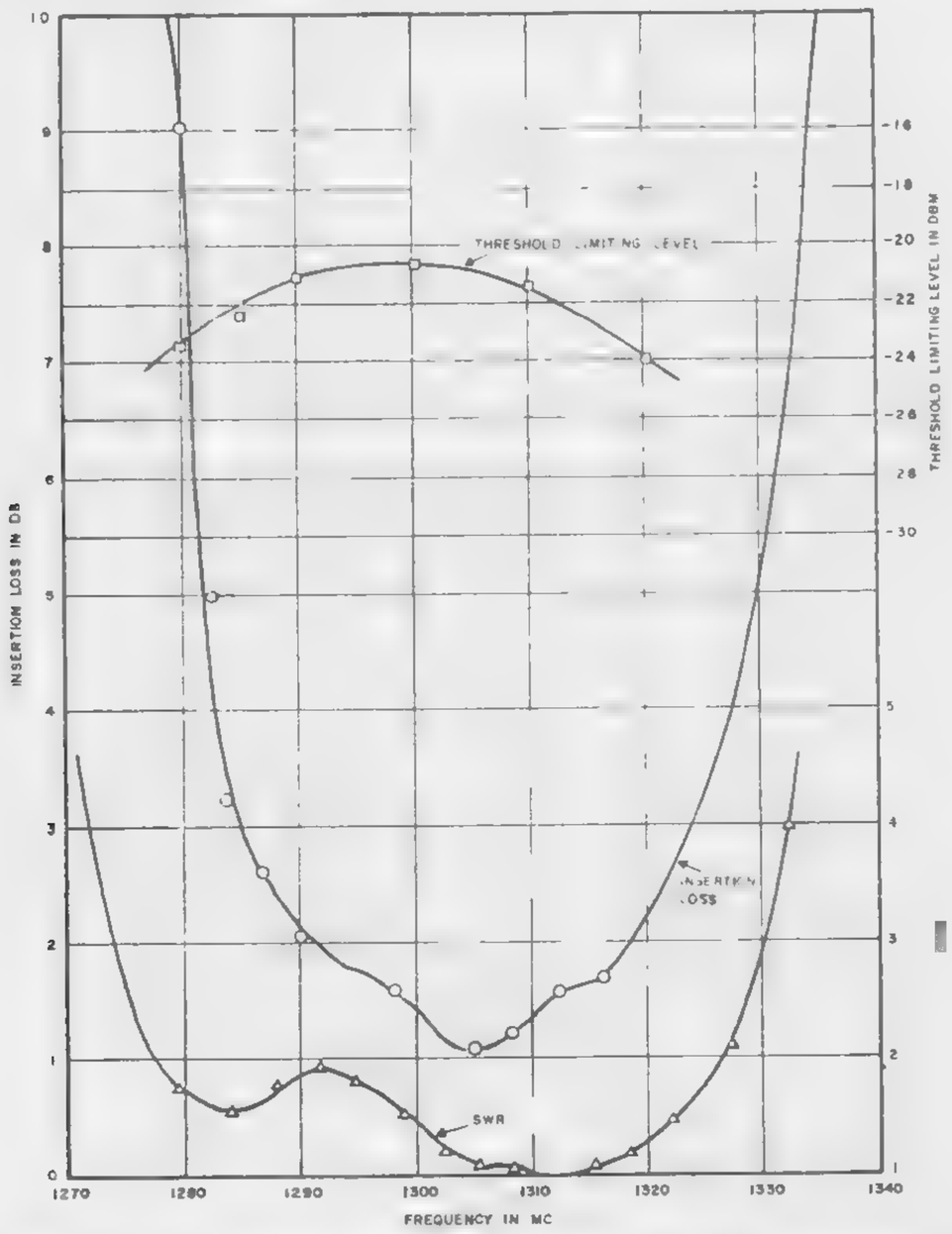


Figure 4—Operating characteristics of *L*-band limiter.

## SESSION VIII: Microwave Applications

### 8.3: Microwave Tunnel Diode Autodyne Receiver*

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Electron Tube Division, RCA

Princeton, N. J.

A MICROWAVE TUNNEL DIODE autodyne receiver using a single tunnel diode to obtain frequency conversion with gain, has been developed. It converts a microwave input signal to an *if* output without a separate local oscillator. Other features of this receiver are:

(*1*) It lends itself readily to miniaturization; the only active circuit element required is a tunnel diode and the passive circuitry required is simple.

(*2*) Power supply requirements are modest; a *dc* voltage of about 0.1-0.3 volt providing a few milliwatts of power is sufficient.

(*3*) The autodyne can operate with unstable tunnel diodes, i.e. diodes where $L_D/R^2_D C_D > 3$, ($L_D$ = series inductance of diode, $-R_D$ = negative resistance of diode, $C_D$ = diode junction capacitance), whereas conventional tunnel diode amplifiers[1] and non-oscillating down converters cannot. This fact is important because diodes operable at high microwave frequencies are, in general, unstable.

Figure 1 shows the circuit of the autodyne receiver. The *rf* input signal is fed through a high-pass filter (which prevents passage of the *if* output signal to the input circuit) and through an impedance transformer into an oscillating circuit. This oscillator consists of a tunnel diode coupled to a transmission line resonator. The diode is biased by battery $V_B$. The value of stabilizing resistor $R_S$ is chosen to provide a *dc* load line intersecting the diode current-voltage characteristic at a single point lying in the negative resistance region, i.e., $(R_S||R_B) < R_D \cdot L_B$ is a choke to decouple the battery from the *rf* and *if* circuits.

The frequency of oscillation[2] is determined by the values of the tunnel-diode parameters and the impedances to which the diode is coupled. To inhibit low-frequency oscillation in the *dc* circuit, the inductance of the stabilizing resistor must be chosen so that $L_S << L_B$. At the signal and oscillation frequencies, also, $L_S$ reduces the loading due to $R_S$.

The nonlinearity of $R_D$ produces mixing of signal and self-oscillation frequencies. The resultant difference frequency *if* passes through a low-pass filter and an impedance transformer to the output circuit. All other frequencies are rejected by the filter.

The output circuit consists of the load $R_L$, which in practice might be the input impedance of an *if* amplifier, and reactive elements $C_L$ and $L_L$, which tune the circuit to the desired intermediate frequency.

Several realizations of the autodyne circuit have been built and tested, using low inductance *pill-type* tunnel diodes**. Strip transmission line circuits have been operated with oscillation frequencies between 800 and 1800 *Mc*, and a coaxial circuit has been operated in the range between 200 and 2500 *Mc*.

A typical strip transmission line autodyne was operated with a signal frequency of 1665 *Mc* and a small signal intermediate-frequency of 30 *Mc*. Figure 2 shows conversion power gain as a function of input power. (The signal power level above which the conversion gain decreases is proportional to the peak current of the diode.) At higher signal power levels, the self-oscillation frequency is pulled by the input signal, and the intermediate frequency is reduced. This effect is illustrated in Figure 3.

In some autodyne circuits, responses were obtained by mixing with harmonics of the oscillation frequency with sensitivity comparable to that at the fundamental. Measurable responses at frequencies as high as the ninth harmonic have been observed.

Noise figure measurements were made on a 1550 *Mc* autodyne using a 30-*Mc* *if* amplifier having a 3-db noise figure. With a wideband noise source, overall noise figures of 6.5 db were measured for the autodyne-*if* amplifier combination.

* Part of the work reported in this paper was supported by the Wright Air Development Division under contract No. AF33(616)-7314.

** RCA.

[1] Smilen, L. I. and Youla, D. C., "Exact Theory and Synthesis of a Class of Tunnel Diode Amplifiers," *National Electronics Conference Record;* 16, 1960.

[2] Nelson, D. E. and Sterzer, F., "Tunnel-Diode Microwave Oscillators with Milliwatt Power Output," *IRE WESCON Convention Record;* 1960.

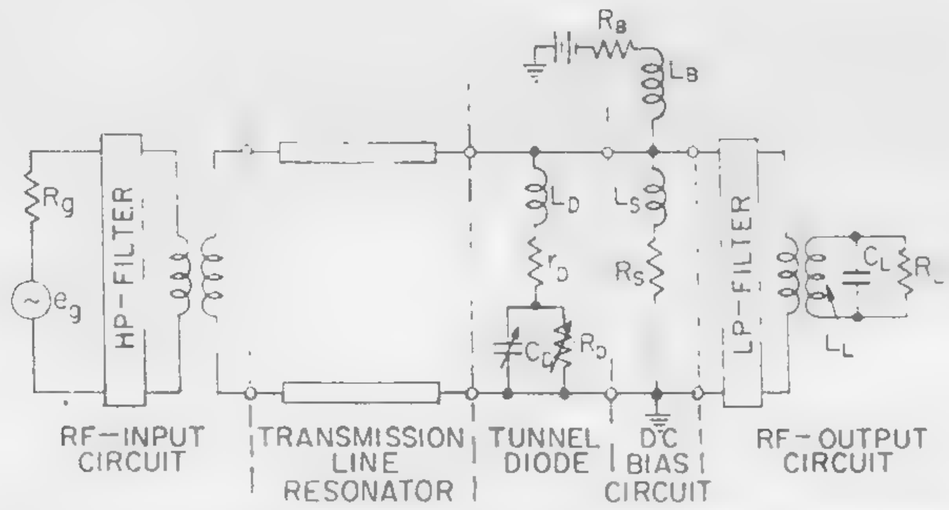


**Figure 1—Equivalent circuit of tunnel-diode autodyne receiver.**

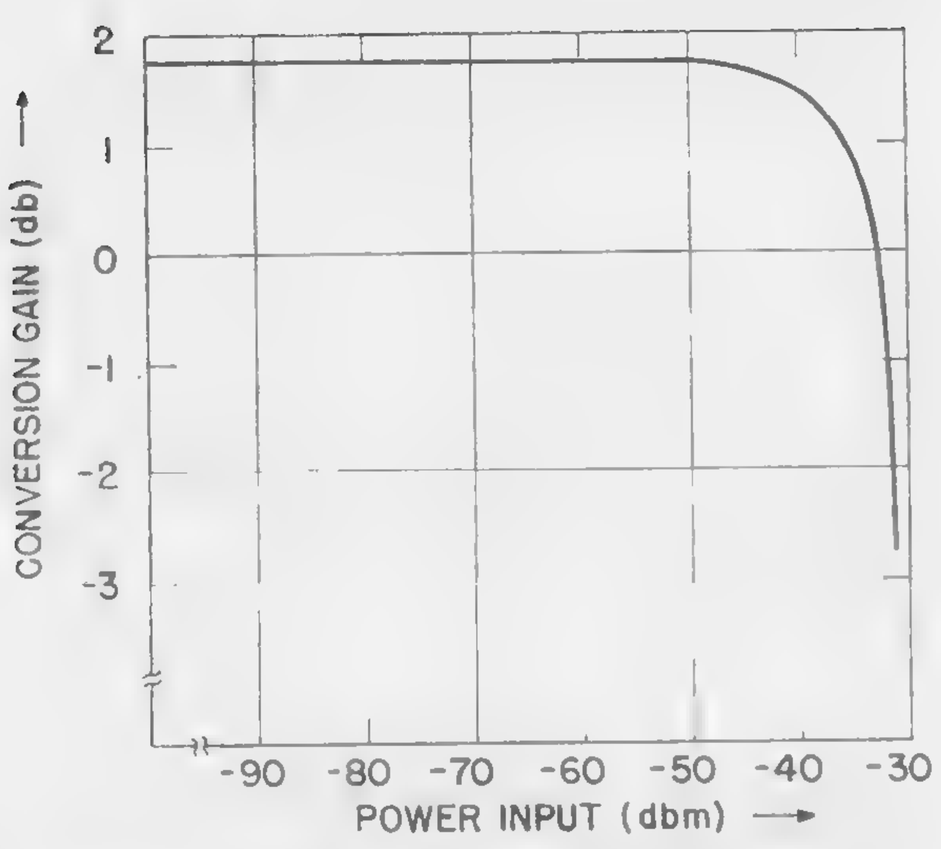


**Figure 2—Conversion gain versus signal input power (signal frequency = 1665 *Mc)* for a strip transmission-line autodyne receiver. A tunnel diode with 5-*ma* peak current was used.**

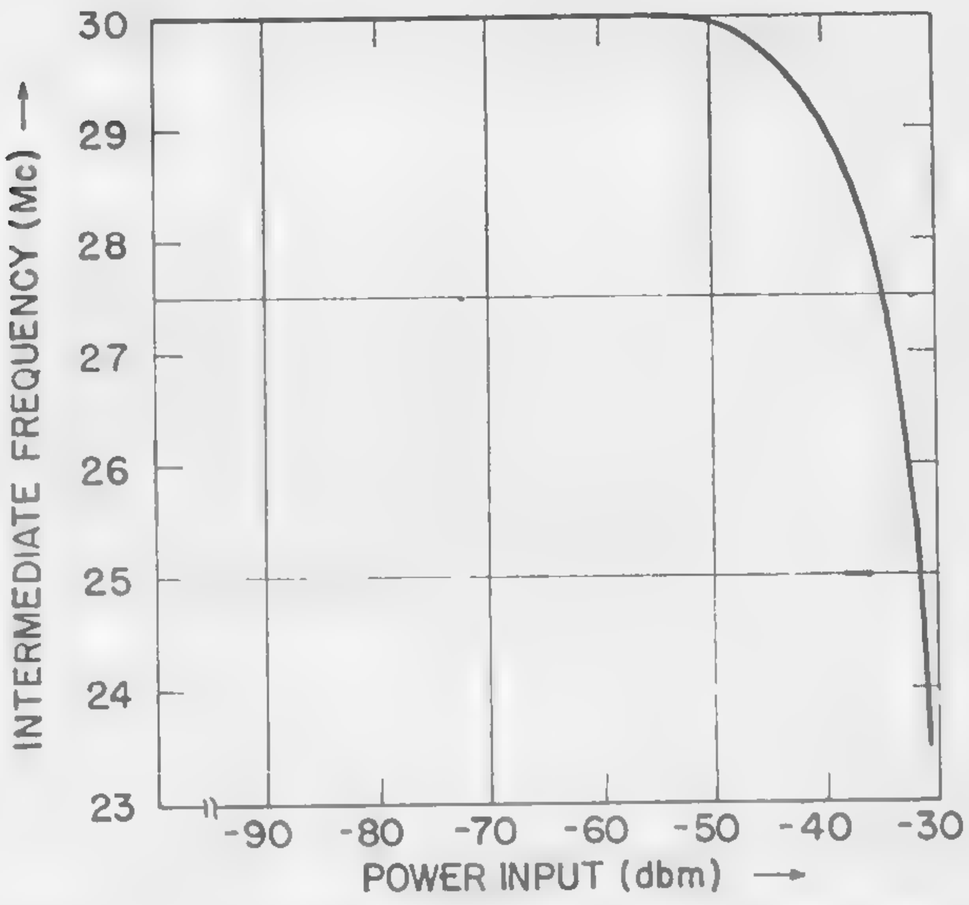


**Figure 3—Output frequency versus signal input power (signal frequency = 1665 *Mc)* for the autodyne receiver referred to in Figure 2.**

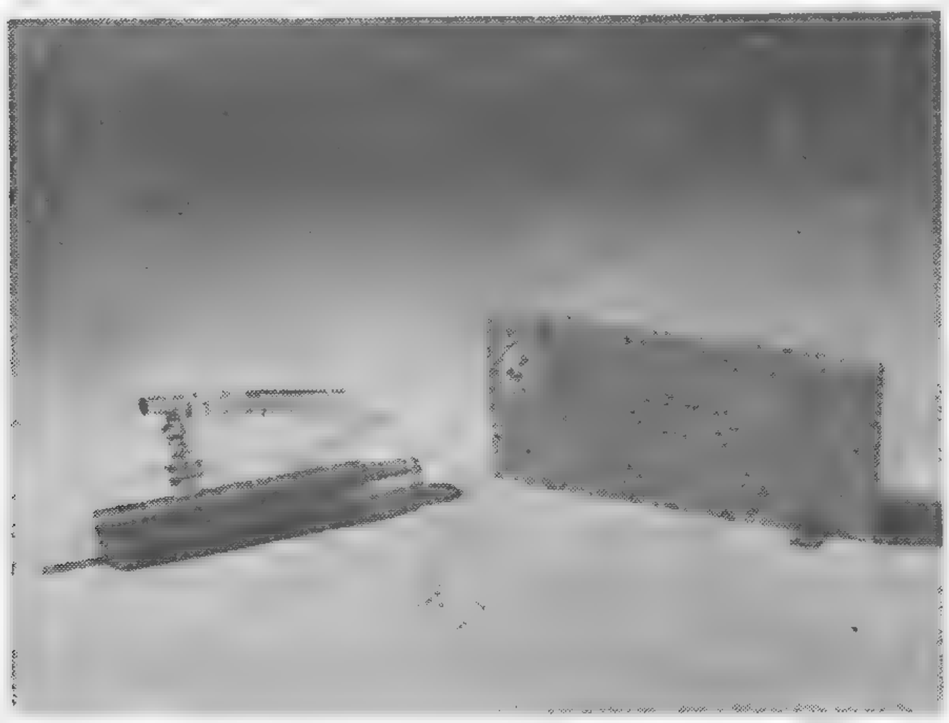

**Figure 4—Photograph of two microwave tunnel-diode autodyne receivers. Shown in the foreground is a tunnel diode of the type used in the two receivers.**

## SESSION VIII: Microwave Applications

### 8.4: A New Broadband Absorption Modulator for Rapid Switching of Microwave Power

**F. Reggia**

Diamond Ordnance Fuze Labs

Washington, D. C.

THIS PAPER WILL DESCRIBE a new technique for obtaining a broadband absorption modulator for high-speed switching or amplitude modulation of microwave power. This ferrite modulator, an outgrowth of the longitudinal-field rectangular waveguide phase shifter[1], has electrical characteristics particularly desirable in a microwave switch. These include a zero-field insertion loss of 0.5 *db*, an isolation of 60 *db* which is nearly independent of the magnetic control field, and an input *vswr* no greater than *1.2* for all values of applied field. These electrical characteristics are nearly constant over a frequency range of 3,000 *Mc* at the *X* band. Also, it is possible to obtain negligible phase shift at the operating frequency. This ferrite modulator is small, requires less than a 50-*oersted* control field, and has a capability of less than one microsecond switching time.

It has been shown[2] that the relationship between the induced *rf* flux density $\vec{b}$ and the internal *rf* magnetic field $\vec{h}$ in a magnetized but unsaturated ferrite medium at microwave frequencies is given by a permeability tensor of the form:

$$\begin{bmatrix} \mu & -jK & O \\ jK & \mu & O \\ O & O & \mu_z \end{bmatrix}$$

where $\mu$, $K$ and $\mu_z$ are the components in the three mutually perpendicular directions and the static magnetic field is taken along the $z$ direction. Thus,

$$b_x = \mu h_x - jK h_y$$
$$b_y = jK h_x + \mu h_y$$
$$b_z = \mu_z h_z.$$

As seen from the first two expressions, an *rf* magnetic field $h_y$ in the $y$ direction induces a component of the *rf* flux density $b_y$ which is proportional to $\mu$ and, due to the electron spins precessing about the direction of the *dc* magnetization, also induces a component $b_x$ in the $x$ direction proportional to $K$. It is this latter component of the permeability tensor which accounts for the transfer of the incident microwave energy to a tightly coupled perpendicular wave in a magnetized ferrite medium.

If a very thin film of absorptive material is used to attenuate this perpendicular field, without appreciable loss to the vertically polarized microwave field which exists when the medium is unmagnetized, it is possible to obtain a broadband absorption modulator with electrical characteristics especially desirable in a high-speed microwave switch.

A simplified drawing of a broadband absorption modulator which makes use of the gyromagnetic phenomena described above is shown in Figure 1. It consists of a low-loss $M_qM_n$ ferrite rod (split along its length) centrally located inside a standard rectangular waveguide system excited in its fundamental $TE_{01}$ mode. The thin resistive film, placed between the sections of the split rod and perpendicular to the input *rf* electric field, is used to attenuate the perpendicular field generated in the magnetized ferrite rod. A low-current solenoid is used to supply the longitudinal magnetic control field.

The electrical characteristics of the modulator switch at 9250 *Mc* are shown in Figure 2, along with the dimensions of the ferrite rod. The attenuator element is a thin film of aquadag on a 0.0003-inch thick mylar sheet. An isolation of greater than 40 *db* is obtained and this isolation is nearly constant for control fields greater than 30 *oersteds*. Less than 2 watts of *dc* power is required.

Further improvements in the isolation-bandwidth characteristics of the absorption modulator were made by adjusting the geometry of the ferrite rod and selecting an attenuator element whose resistivity is accurately known and controlled. These results are shown in Figures 3 and 4 for a number of $M_qM_n$ ferrite rods (4-inches long) and a metallized mica attenuator element.

The measured data shown in Figure 4 were obtained for three ferrite rods which were 4-inches long, including the impedance matching tapers at both ends. An isolation in the *OFF*-state of greater than 60 *db* was found possible over a bandwidth in excess of 2500 *Mc* and as much as 55-*db* isolation was obtained over a 3500 *Mc* bandwidth.

The electrical characteristics of the rectangular waveguide absorption modulator from 8500 to 9500 *Mc* are shown in Figure 5. These results were obtained with a 4-inch long ferrite rod, including ⅞-inch tapers at both ends, having a height and width of 0.300-inch and 0.320-inch, respectively. A metallized mica attenuating element was used.

Adjustment of the resistivity of the attenuator element can be made to produce nearly zero phase shift at the desired operating frequency. This is shown in Figure 6 for four different frequencies, along with specific results obtained at 9,200 *Mc* for attenuator element resistivities varying from 10 to 80 ohms per square. Thus, amplitude modulation without phase modulation is possible.

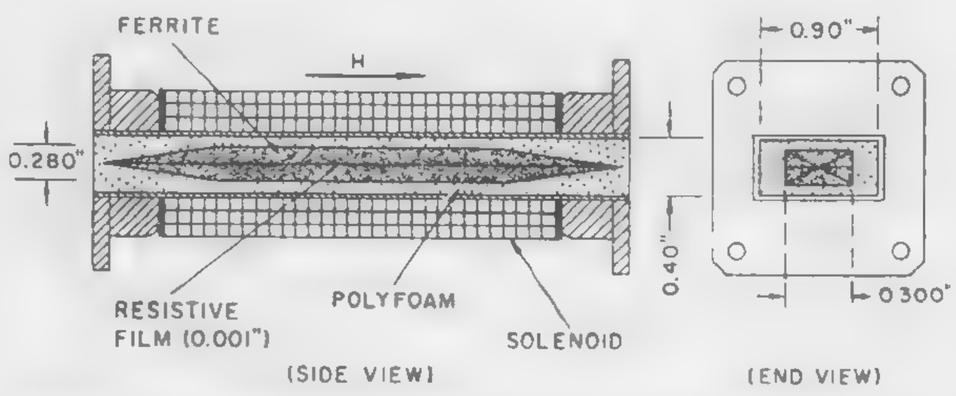


**Figure 1—Cross-sectional views of the ferrite absorption modulator. The rectangular ferrite rod is centrally located inside an *X*-band waveguide.**

---

[1] Reggia, F. and Spencer, E. G., "A New Technique in Ferrite Phase-Shifting for Beam Scanning of Microwave Antennas," *Proc. IRE*, p. 1510-1517; November, 1957.

[2] Rado, G. T., "Electromagnetic Characterization of Ferromagnetic Media," *Trans. of IRE (PGAP)*, p. 512-525; July, 1956.

[3] Tompkins, J. E., Reggia, F., and Joseph, L., "Multimode Propagation in Gyromagnetic Rods and its Application to Traveling Wave Devices," *Jour. Appl. Physics*, p. 176S; May, 1960.

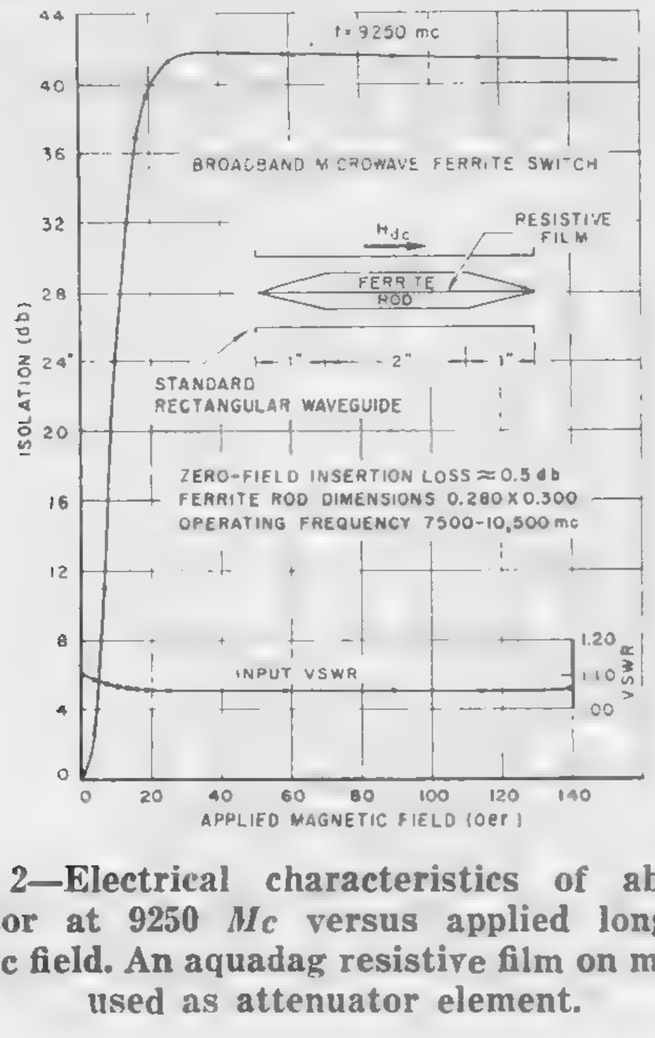


**Figure 2—Electrical characteristics of absorption modulator at 9250 *Mc* versus applied longitudinal magnetic field. An aquadag resistive film on mylar was used as attenuator element.**

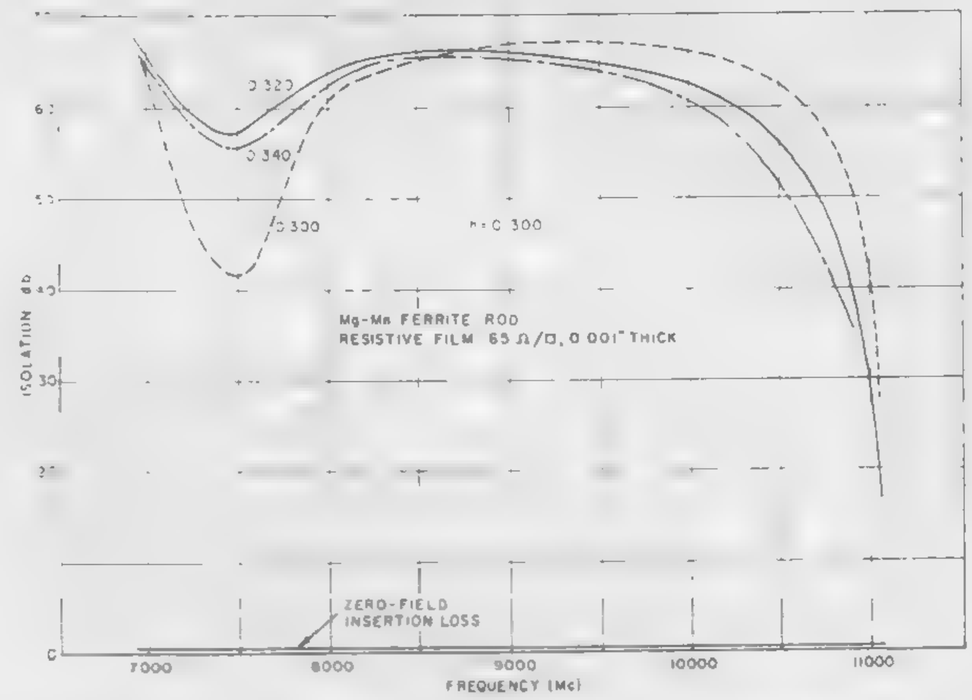


**Figure 3 — Isolation bandwidth characteristics of modulator using ferrite rods 4-inches long and 0.320-inch wide. Applied magnetic field was 100 *oersteds* and parameter was the rod height. Zero-field insertion loss of rods was 0.5 *db*.**

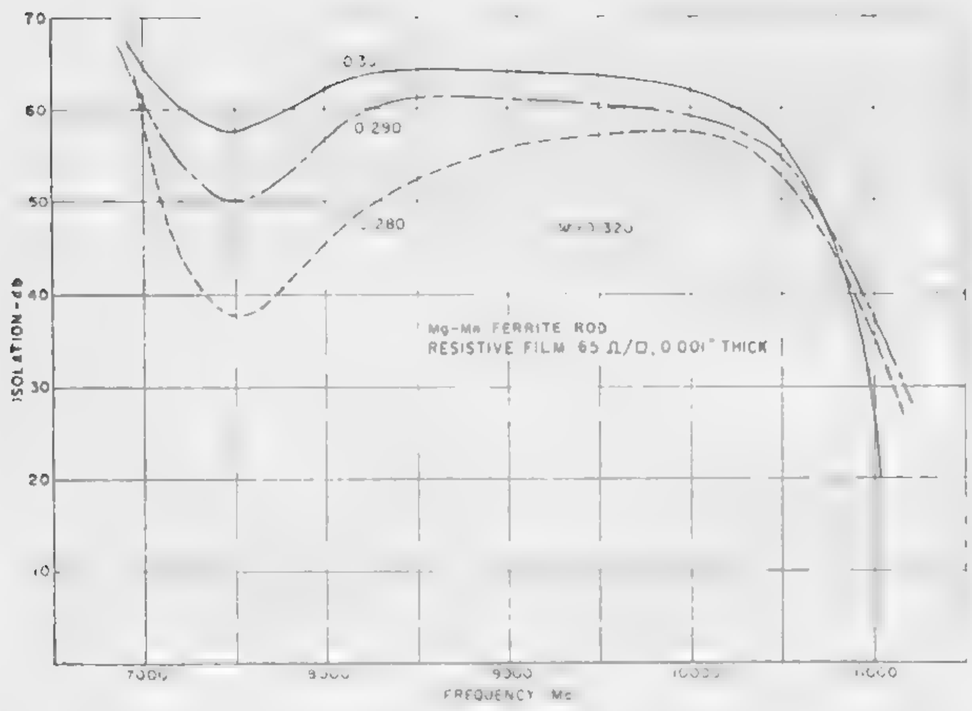


**Figure 4—Isolation bandwidth of absorption modulator. Ferrite rods were 4-inches long and 0.300-inch high. The applied magnetic field was 100 *oersteds* and the rod widths varied from 0.300 to 0.340-inch.**

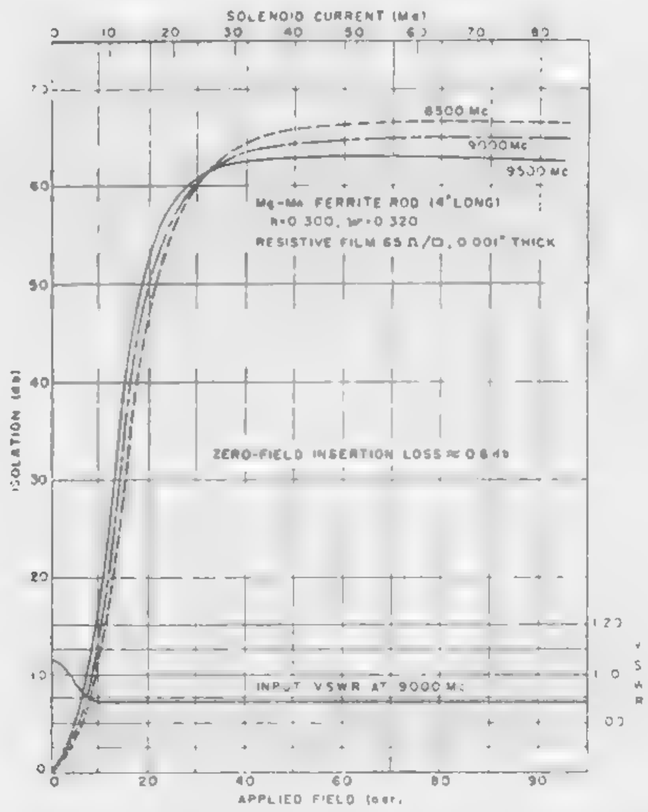


**Figure 5—Electrical characteristics of broadband absorption modulator versus applied magnetic field. A *dc* power of 2 watts was required to obtain a field strength of 40 *oersteds*.**

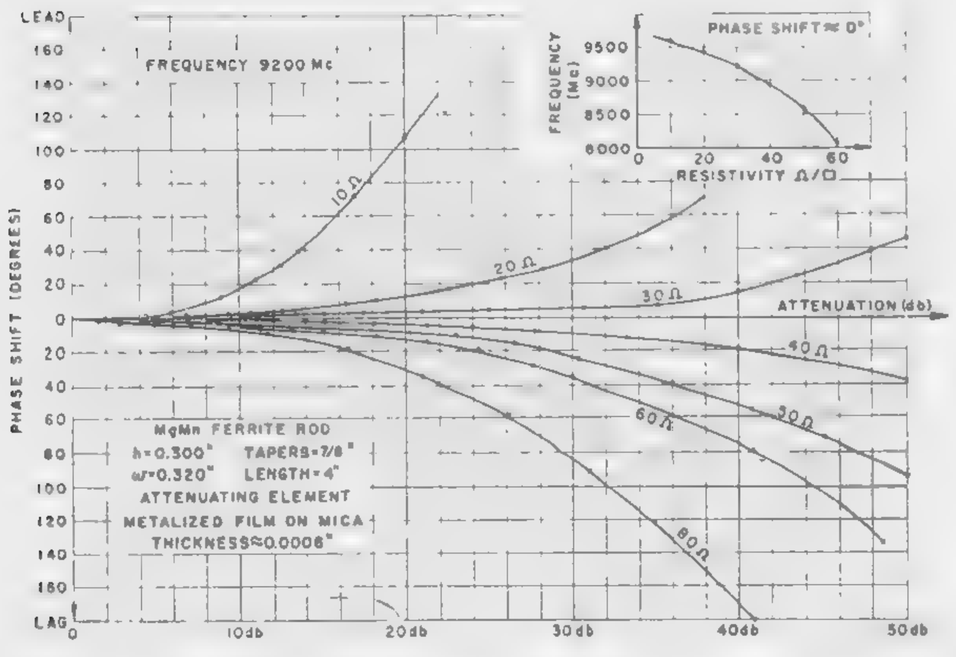


**Figure 6—Phase shift characteristics of modulator at 9,200 *Mc* using a ferrite rod (4-inches long) with height and width of 0.300 and 0.320-inch, respectively.**

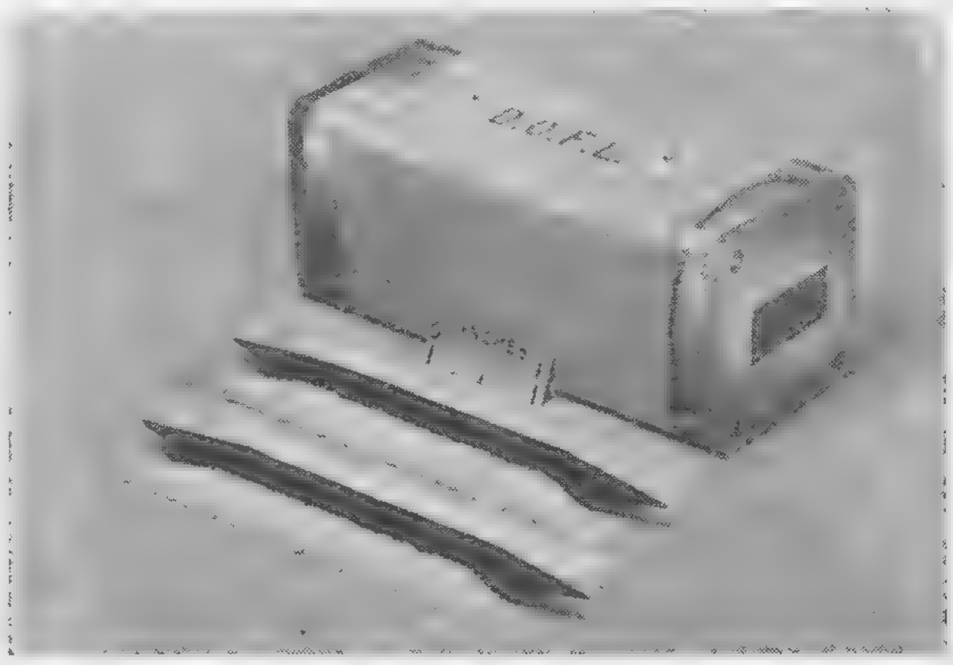

**Figure 7—Photograph of *X*-band absorption modulator. Split sections of ferrite rod and polyfoam support are shown in foreground. Total length of modulator is 4 inches.**

## SESSION VIII: Microwave Applications

### 8.5: Fast One-Kilomegacycle Ferrite Switch

E. Stern and R. E. Cole

Electronics Lab., General Electric Company

Syracuse, N. Y.

THE VARIATION OF FERRITE PERMEABILITY with magnetizing field has been used successfully in one fashion or another for switching microwave power. This paper will describe a means for increasing the speed of a 1-*kMc* moderate power switch to one microsecond or less.

The real ($\mu'$) and imaginary ($\mu''$) parts of ferrite permeability are shown in Figure 1 as a function of magnetizing field. Low loss switching is achieved by varying the permeability with a magnetizing field either well below or above resonance. At low frequencies in the microwave range, an additional loss occurs about zero field. Therefore, a 1 *kMc* switch should operate above resonance. Since the permeability varies slowly with the magnetizing field above resonance, a large change of field in a large volume of ferrite is normally required to provide the necessary phase shift to switch the microwave energy. These combined requirements predicate the use of a large magnetizing coil with many turns having an $^{L}/_{R}$ ratio of 1 to 10 milliseconds.

The circuit in Figure 2 permits a drastic reduction of the ferrite volume and switching field by the use of the variable-reactance principle. The variable reactance at the ferrite-coax interface controls the phase of the reflected wave. A thin ferrite tube, silvered on the inner and outer surfaces, provides the shorted section of ferrite-filled coaxial line whose input reactance is sensitive to the permeability. The silver deposit on the outer surface can be made sufficiently thin to avoid the *shorted turn* effect, and the coil can be wound directly on the ferrite tube to minimize its inductance. When necessary, the ferrite can be cooled at the outer surfaces.

A phase shift of ±45° is required at each element to switch the power from port *A* to *B*. The necessary change of permeability ($\Delta\mu$) to produce this phase shift is shown in Figure 3 as a function of the coax-ferrite line impedance ratio

$$Z_1 = \sqrt{\frac{\mu_1}{\epsilon_1}} \frac{ln\ (^{b}/_{a2})}{ln\ (^{b}/_{a1})}$$

The parameter (2*N*-1) represents the number of odd quarter wavelengths of ferrite.

The upper limit of loss tangent (tan $\delta$) consistent with a maximum absorption loss of 1 *db* is shown in Figure 4 as a function of $z_1$ *and* N.

The bandwidth of the switch is limited by the differential permeability and electrical length. The bandwidth of the phase error resulting from the frequency sensitivity of switch is shown on Figure 5 as a function of $z_1$ and *N*. The bandwidth is defined as the frequency range wherein the switch directivity error is less than 0.5 *db*. It will be noted that this definition of bandwidth is somewhat arbitrary. The actual frequency range of a switch depends upon its application.

### *Heat Transfer Capability*

The maximum average power capacity depends upon the heat transfer capability from the ferrite to a heat sink within the allowed temperature rise $\Delta T$. It is roughly equal to (*cgs* units)

$$P_{av} \leq \frac{4.2\,\pi K l \Delta T}{s\ ln\ (^{b}/_{a_2})} \quad watts$$

where $s$ equals $P_{out}{}^{\circ}P_{in}$, $K$ is the thermal conductivity of the ferrite, and $l$ is the ferrite length.

The peak power capacity is limited by the spin instability threshold[1] field $h_{crit}$, and is equal to (*MKS* units) $60\pi^2 ln\,(^{b}/_{a1})\ a_2{}^2\ (h_{crit})^2$ watts.

The inductance of the switching coil L is roughly equal to $\frac{\mu_0 \pi n^2 b^2}{4l}$ henries, and the number of ampere turns ($nI$) necessary for switching equals $h_s l$ ampere turns. The normalized value of switching field is shown in Figure 6 for a particular ferrite as a function of $Z_1$ and *N*. The parameter $\Omega_m$ is defined as $\frac{4\pi\gamma M}{\omega}$ ; where $4\pi M$ is the saturation magnetization, $\gamma$ the gyromagnetic ratio, and $\omega$ the angular frequency. The switching field $h_B$ equals $\omega/\gamma$ $\left(\frac{\gamma h_\sigma}{\omega}\right)$ *amperes/meter.*

### *Switch Element Design*

A switch element was built according to the preceding design techniques. The pertinent parameters are $N = 2$, $z_1 = .55$, $\Omega_m = 2$; $I$, the switching current = 10 amperes. The preliminary measurements indicate an insertion loss of 1 *db* or less, and a coil inductance of 0.4 microhenries.

[1] Suhl, H., Proc. IRE, p. 1270; October, 1956.

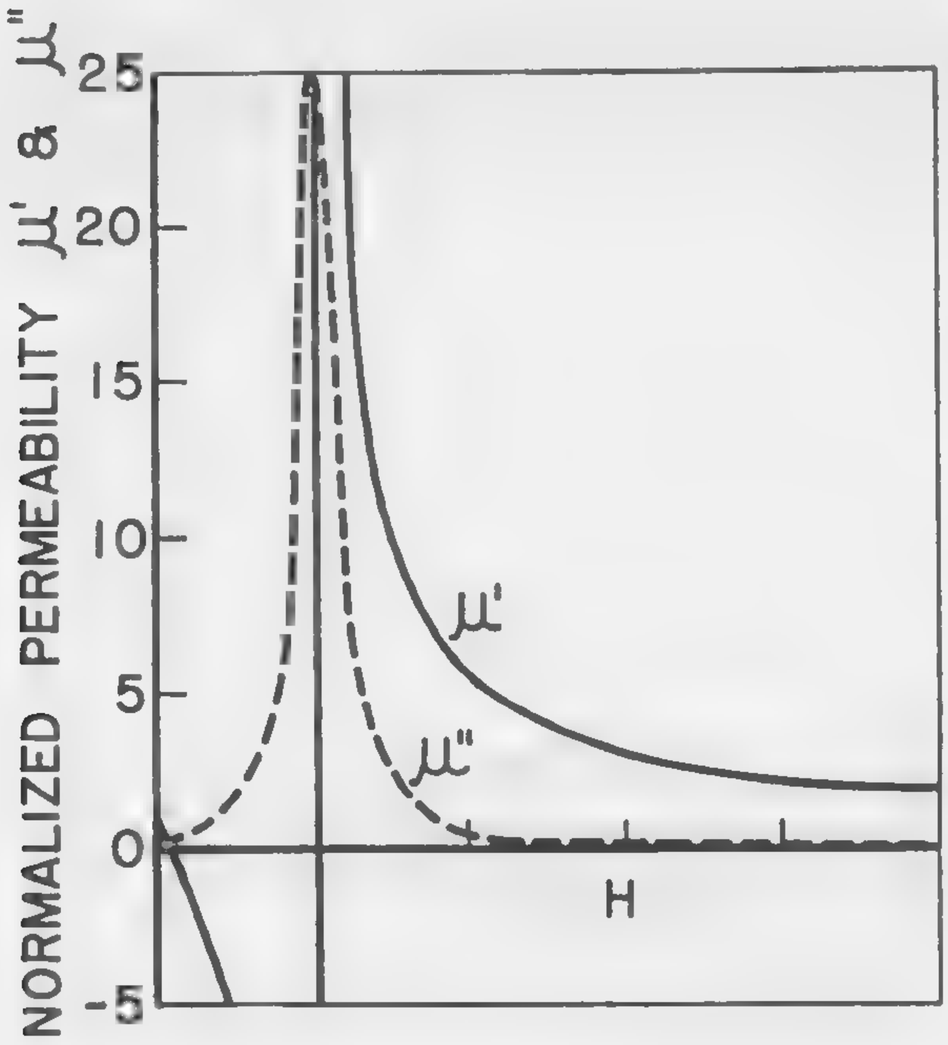


Figure 1 (*left*)—The behavior of ferrite permeability ($\mu = \mu' + j\mu'$) as a function of magnetizing field $H$ at low microwave frequencies. The zero field loss has been omitted in this figure.

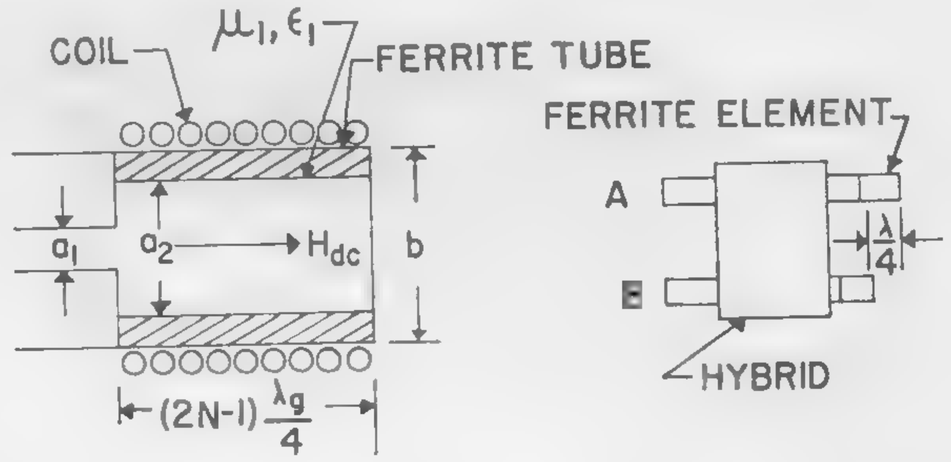


Figure 2 (*above*)—The switch element, a coaxial line coupled to a shorted section of a ferrite-filled coaxial line. The switch input $A$ should normally be preceded by a circulator.

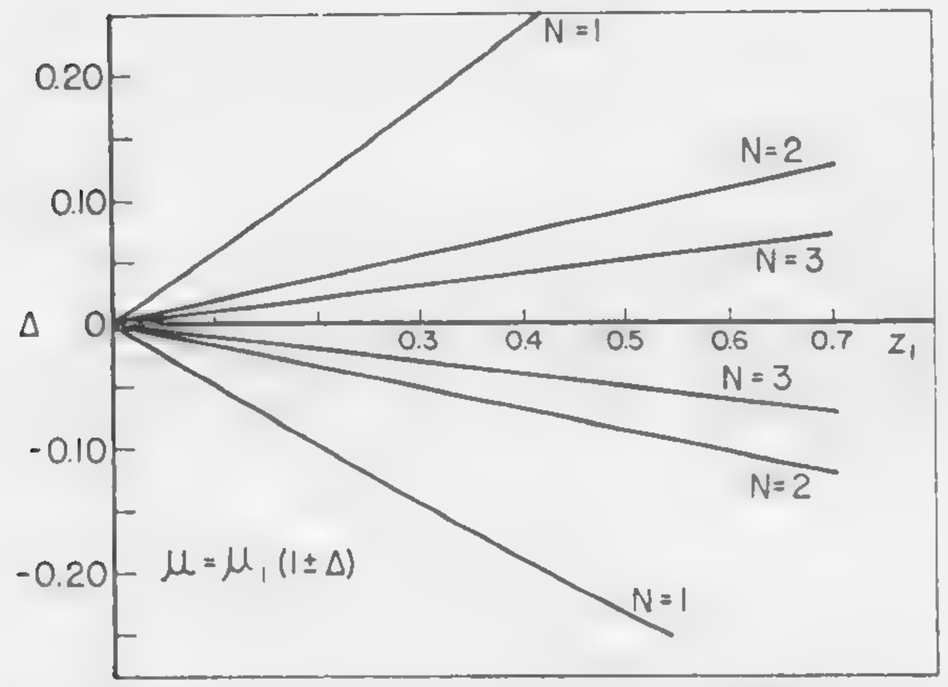


Figure 3—The required change of permeability $\Delta\mu$, as a function of the impedance ratio $Z_1$ with $N$ as a parameter; note that the ferrite length equals

$$(2N - 1)\frac{\lambda g}{4}$$

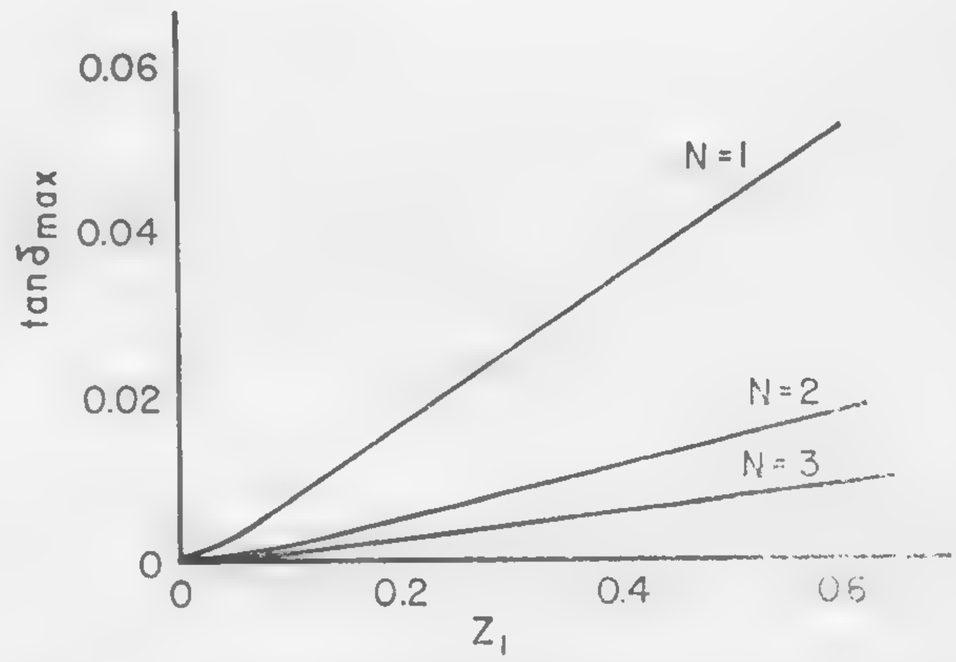


Figure 4—The maximum allowable loss tangent of the ferrite consistent with a 1-*db* insertion loss as a function of $Z_1$ and $N$.

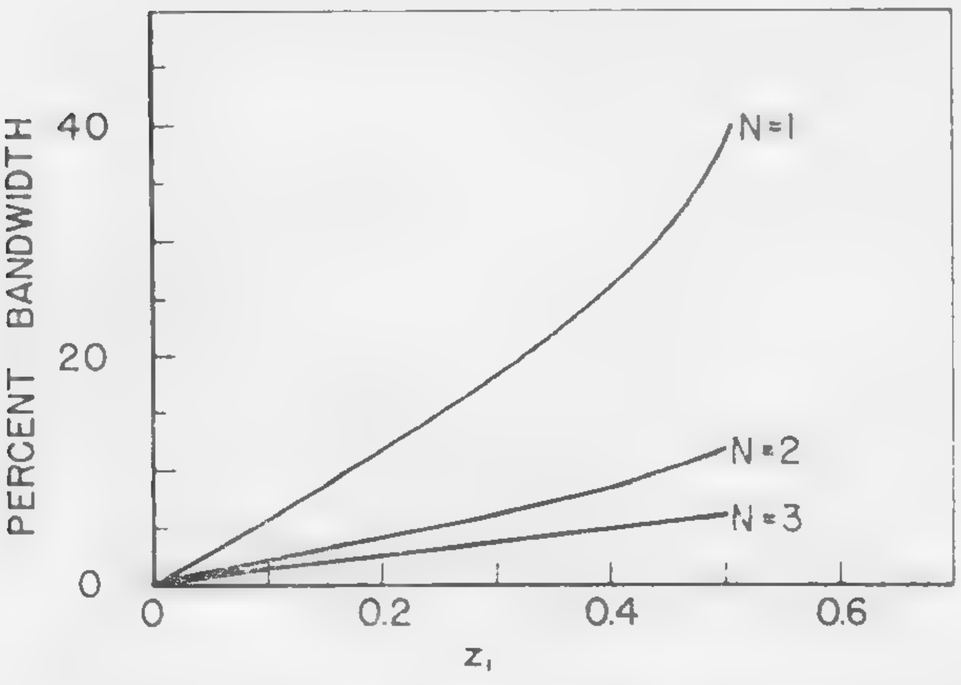


Figure 5—The nominal bandwidth of the switch as a function of $Z_1$ with $N$ as a parameter. The bandwidth is defined as the frequency range wherein the switch directivity loss is less than 0.5 *db*.

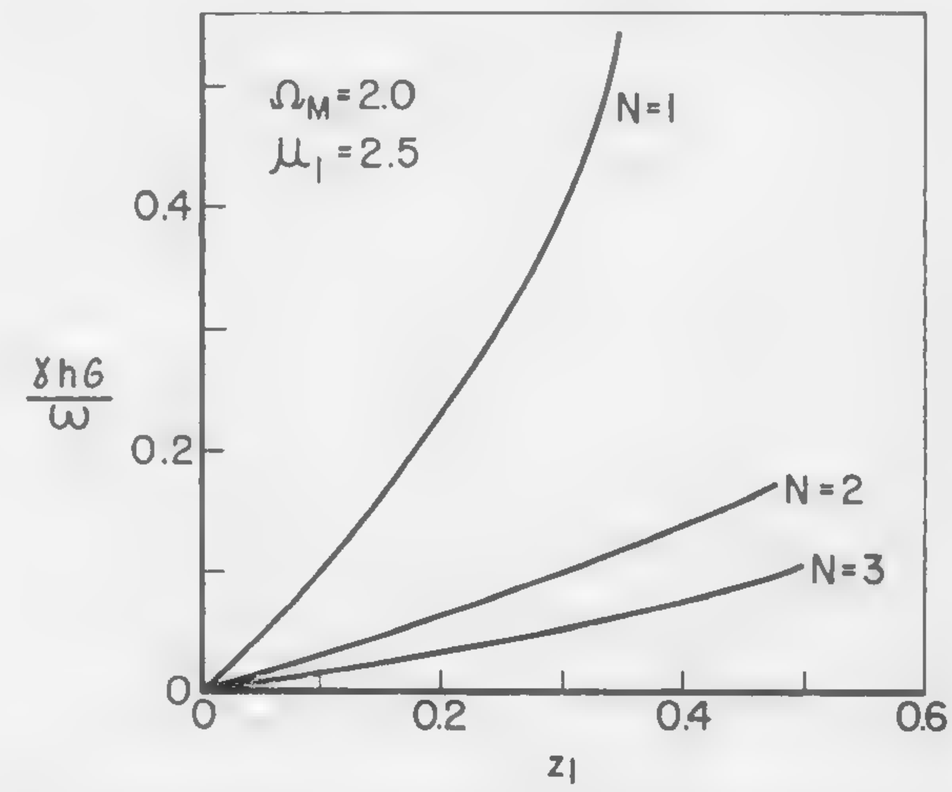


Figure 6—The normalized switching field as a function of $Z_1$ for a particular material and operating point. The switching field is equal to

$$\frac{\omega}{\gamma}\left(\frac{\gamma h\sigma}{\omega}\right) \textit{ amperes/meter;} \text{ and } \Omega_m \equiv \frac{4\pi M}{\omega}$$

## Informal Discussion Sessions

### E.7: Low-Frequency, Low-Level Signal Amplification

*[Delaware Valley]*

**Moderator: W. Moore, Jr.**, Brown Instrument Div., Minneapolis-Honeywell Regulator Co., Philadelphia, Pa.

**Panel Members:** J. S. MacDougall, Raytheon Co., Needham, Mass.
D. B. Hall, Texas Instruments, Inc., Dallas, Tex.
M. W. P. Strandberg, Cambridge Electronics Corp., Newton Lower Falls, Mass.
E. G. Nielsen, Electronics Lab., General Electric Co., Syracuse, N. Y.
D. A. Robinson, Airpax Electronics, Inc., Ft. Lauderdale, Fla.
D. Hilbiber, Fairchild Semiconductor Corp., Palo Alto, Calif.

### E.8: A Second Look at Microelectronics

*[Ballroom East]*

**Moderator:** E. Fletcher, MIT, Cambridge, Mass.

**Panel Members:** J. Nall, Fairchild Semiconductor Corp., Palo Alto, Calif.
R. G. Counihan, IBM Corp., Kingston, N. Y.
R. Alberts, WADD, Dayton, O.
W. Gaertner, CBS Laboratories, Inc., Stamford, Conn.
T. Stanley, RCA Laboratories, Princeton, N. J.
R. E. Lee, Texas Instruments, Inc., Dallas, Tex.
V. J. Kublin, Engineering Lab., U.S. Army Signal Corps, Ft. Monmouth, N. J.
A. P. Stern, Electronics Lab., General Electric Co., Syracuse, N. Y.
G. Mollenstedt, University of Tübingen, Tübingen, West Germany
S. J. Angello, Westinghouse Electric Corp., Pittsburgh, Pa.
E. Keoniian, American Bosh Arma Corp., Garden City, N. Y.
R. Rice, IBM Corp., Poughkeepsie, N. Y.

### E.9: Tunnel Diodes

*[Ballroom West]*

**Moderator:** E. O. Johnson, RCA, Somerville, N. J.

**Panel Members:** L. Cuccia, RCA, Harrison, N. J.
J. A. Walsh, IBM Corp., Poughkeepsie, N. Y.
G. Sharpe, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
J. Tiemann, Research Lab., General Electric Co., Schenectady, N. Y.
J. R. Biard, Texas Instruments, Inc., Dallas, Tex.

## E.10: Access and Storage Techniques

*[Pennsylvania East-West]*

**Moderator: A. Lo,** IBM Corp., Poughkeepsie, N. Y.

**Panel Members:** J. Rajchmann, RCA Laboratories, Princeton, N. J.
S. M. Rubens, Sperry-Rand Univac, St. Paul, Minn.
Q. W. Simkins, IBM Corp., Poughkeepsie, N. Y.
M. Rosenberg, Telemeter Magnetics, Los Angeles, Calif.
E. A. Fisch, Electronics Lab., General Electric Co., Syracuse, N. Y.
J. E. Mack, Bell Telephone Laboratories, Inc., Whippany, N. J.
R. McMahon, MIT Lincoln Laboratory, Lexington, Mass.

## E.11: Optical Masers

*[Constitution and Independence]*

**Chairman: A. L. Schawlow,** Bell Telephone Laboratories, Inc., Murray Hill, N. J.

**Panel Members:** M. Stevenson, IBM Corp., Yorktown, N. Y.
J. P. Wittke, RCA Princeton, N. J.
R. T. Daly, Technical Research Group, Inc., Syosset, L. I., N. Y.
G. C. Dacey, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
W. S. Boyle, Bell Telephone Laboratories, Inc., Murray Hill, N. J.
G. Wessel, Electronics Lab., General Electric Co., Syracuse, N. Y.
G. Birnbaum, Hughes Research Laboratory, Malibu, Calif.

## E.12: Varactor Applications

*[Hall of Flags, East]*

**Moderator: R. P. Rafuse,** MIT, Cambridge, Mass.

**Panel Members:** K. Johnson, Texas Instruments, Inc., Dallas, Tex.
P. Penfield Jr., MIT Cambridge, Mass.
N. Houlding, National Co., Malden, Mass.
A. Uhlir, Jr., Microwave Associates, Burlington, Mass.
G. Luettgenau, Pacific Semiconductors, Inc., Culver City, Calif.
B. Salzberg, Airborne Instrument Labs., Mineola, L. I., N. Y.
B. Diamond, MIT Lincoln Laboratory, Lexington, Mass.

## SESSION IX: Communication Circuits and Techniques

Chairman: R. L. Pritchard

Texas Instruments, Inc., Dallas, Tex.

### 9.1: Optical Masers

**G. C. Dacey**

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

THE POSSIBILITY THAT THE MASER principle could be extended to optical frequencies was published in the Physical Review in 1958 by *Schawlow* and *Townes*[1]. Since then a good deal of work has been done at many laboratories and several different optical maser oscillators have been demonstrated recently[2,3]. All of these devices depend for their operation on essentially the same principle: An assemblage of atoms appropriately excited to an excited energy state is placed in an appropriate optical cavity. If the atoms are able to radiate light quanta by stimulated emission and if the density of the excited atoms exceeds that critical value with which the stimulated emission of light exceeds the radiation and other losses of the optical cavity, then a coherent standing wave of light will build up in the cavity.

To illustrate more fully the principle of operation of an optical maser oscillator, let us consider the case of the $R_1$ line ruby optical maser [2,3]. Ruby consists of a crystal of aluminum oxide with a small concentration of chromium atoms substituted for aluminum atoms. These chromium atoms have a broad absorption band in the green and another in the blue. The absorption of light in either of these bands leads to the emission of several sharp lines in the red part of the spectrum. These lines correspond to emission from metastable levels to the ground state. The quantum efficiency of the fluorescence is nearly unity, and the spectral lines are very sharp. A simplified energy diagram representing this situation is shown in Figure 1.

The emission of light from an excited state, such as the $R_1$ emission from ruby, can take place in two different ways. If the excited atom is not disturbed, emission can occur sponstaneously. If, however, the excited atom is immersed in a photon field at the emission frequency, then the emission is accelerated by a process called *stimulated emission.* The stimulated emission light has the same frequency and phase as the radiation field. As the radiation field increases in intensity, stimulated emission will predominate over spontaneous emission. If there are present in the radiation field unexcited chromium atoms, these can absorp photons from the field. For maser action to take place the density of atoms in the excited state must be greater than that in the lower or ground state; if this is not the case then absorption will predominate over stimulated emission. This situation is illustrated in Figure 2.

To satisfy the excess population condition for the $R_1$ line of ruby, it is necessary to transfer more than half of the chromium atoms from the ground state to the metastable state. This, in general, is accomplished by pumping the ruby with a bright flash of green light; for example by a Xenon flash lamp, as illustrated in Figure 3.

When the excess population in the metastable level has been effected, the ruby constitutes a medium capable of amplifying light waves passing through it. To produce oscillations it is necessary to provide an optical feedback path. This can be conveniently done by using a pair of plane-parallel partially-reflecting mirrors at either end of a rod of ruby. This situation is illustrated in Figure 4. Waves oscillating back and forth along the axis of the two mirrors are amplified, leading to coherent oscillations, whereas waves traveling in any other direction soon miss the end mirrors and are lost from the system. The resulting light which emerges from the partially transmitting mirrors is intense, coherent, highly monochromatic, and very directional.

#### *Implications for Communications*

With the advent of optical masers, it is possible for the first time to generate coherent light waves in a manner analogous to that in which it has previously been possible to generate radio waves. However, the carrier frequencies are on the order of $5 \times 10^{14}$ *cps*—a factor of $10^4$ greater than the highest microwave frequencies in use. The band of frequencies which in principle becomes available is wider than $10^{14}$ *cps*—more than adequate to carry 10-million simultaneous television programs. Equivalent directivity can be obtained with antennas ten-thousand times smaller than conventional microwave antennae. For example, the ruby maser beam, emanating from a ¼-inch diameter rod is only 1/20-inch of a degree in angular divergence. It would take a microwave antenna 1,200-feet in diameter to obtain equivalent directivity. Of course, many problems remain, e.g., modulation, detection, and continuous operation. Nevertheless, it is fair to say that a new era of communication possibilities has begun.

With optical masers it is possible to produce light beams of greater intensity, especially in the infrared part of the spectrum, than have previously been available. Electric field strengths at optical frequencies of greater than $10^5$ volts/cm may be possible. Thus, we may find entirely new interactions between light and matter. Perhaps it will become possible to accelerate greatly the rate of photochemical reactions thus producing new substances, or, since the beam can be so highly monochromatic, to favor the reaction of one isotope rather than another. Standard radio technique, for example the heterodyne principle, will have interesting implications for spectroscopy, if it becomes possible to beat light against light. Then, too, such intense light sources may have important technological applications—for example, in high speed microphotography.

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[1] Schawlow, A. L., and Townes, C. H., *Phys. Rev.*, p. 1940; 112, 1958.

[2] Maiman, T. H., *Nature*, 493; 187; 1960.

[3] Collins, J. R., Nelson, D. F., Schawlow, A. L., Bond, W. L., Garrett, C. G. B., and Kaiser, W. K., *Phys. Rev. Letters*, p. 303; 5; 1960.

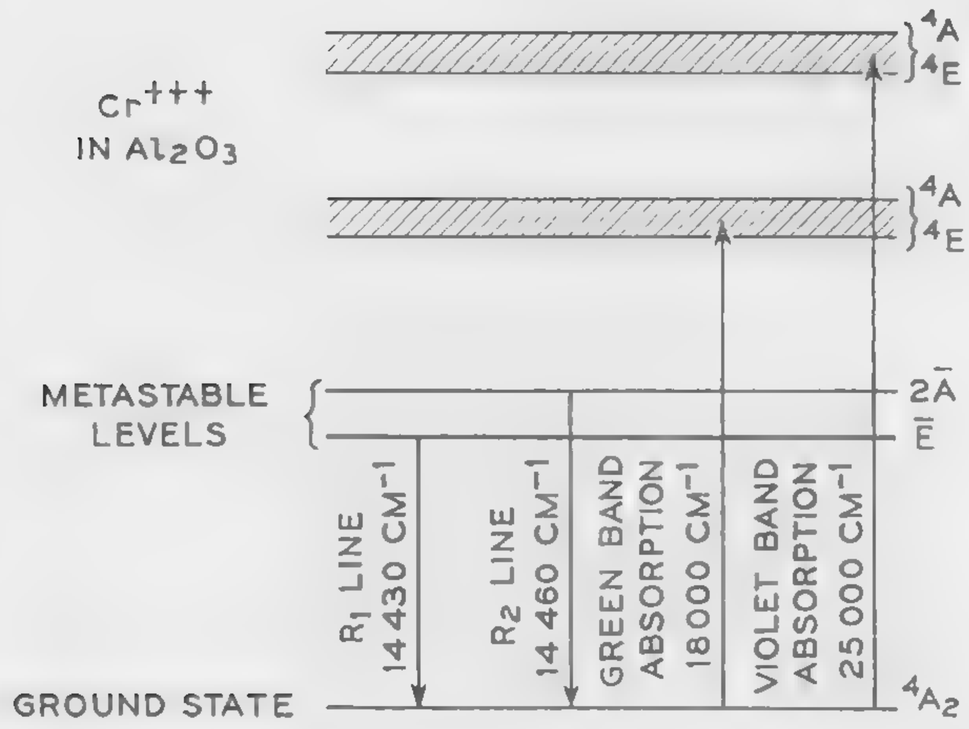


**Figure 1—Simplified energy level diagram for the fluorescence of ruby.**

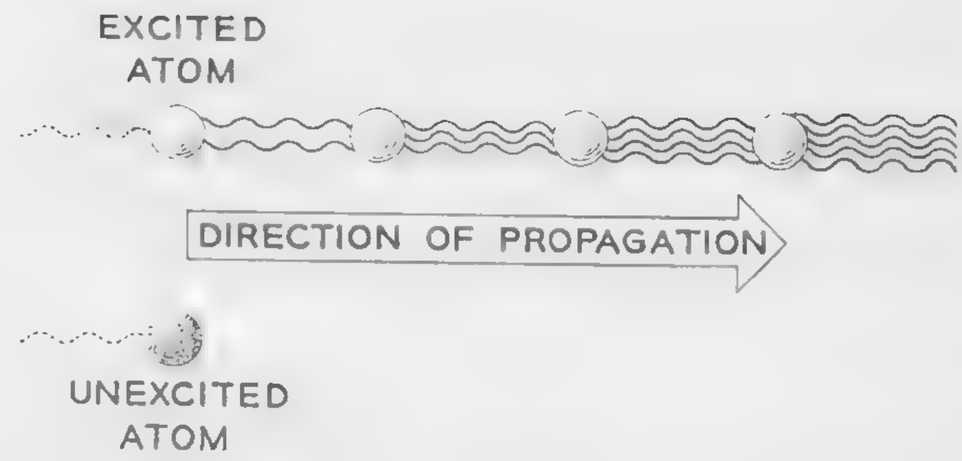


**Figure 2—Growth of a light wave by stimulated emission. Wave striking excited atom at same frequency forces it to *join* the original emission. Unexcited atom absorbs wave and ends emission.**

**Figure 3—The schematic representation of pumping arrangement for pulsed ruby optical maser. The helix represents a Xenon flash lamp.**


**Figure 4—One arrangement of optical maser in which wave *grows* as it bounces back and forth between reflecting walls. (Vertical dimension of the diagram has been greatly exaggerated for clarity.)**

## SESSION IX: Communication Circuits and Techniques

### 9.2: Low-Gain Wide-Band Esaki-Diode Amplifiers

**B. G. King and G. E. Sharpe**

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

VOLTAGE GAIN can be obtained with a negative resistance $-R_D$ and a load resistance $R_O$ as shown in Figure 1. To modify the input resistance of such an amplifier, its input can be shunted with a resistance $R_I$, as shown in Figure 2.

An *Esaki* diode, whose current-voltage and dynamic resistance characteristics are shown in Figure 3 can, if properly biased, be used to provide the required negative resistance. The equivalent circuit of such a diode, loaded at its input with the parallel combination of $R_O$ and $R_I$, and at its output with $R_O$ is shown in Figure 4. Clearly, the diode capacitance $C_D$ and the diode inductance $L_D$ affect the circuit behavior at higher frequencies. It can be shown that the insertion current gain is inversely proportional to $|Z|$, where $Z$ is the impedance seen at the break $xx$ in the circuit shown in Figure 4. A calculated plot of $Z$ for typical diode parameters used in these experiments is shown in Figure 5. It is seen that the shape of this curve and consequently the amplifier frequency response can be modified for a given diode having parameters $-R_D$, $L_D$ and $C_D$, by adding inductance or by changing the total resistance $R_T$ in the circuit. The spreading resistance of the diode, $R_S$, has been ignored in the calculations.

By making $|Z|$ at some frequency equal to its value at *dc*, a low-pass amplifier can be constructed. For such an amplifier it can be shown that the average computed gain and bandwidth vary as follows:

| *Average Gain—Db* | *Bandwidth* |
|---|---|
| 6 | $\sqrt{2} f_M$ |
| 9.5 | $f_M$ |
| 12 | $\frac{\sqrt{3}}{2} f_M$ |

For a typical germanium diode $-R_D = -75$ ohms, $C_D$ is $5 \times 10^{-12}$ farads, and $f_M$ is $1/2\pi \times 1/C_D R_D = 425$ *Mc*.

The dynamic stability of such a negative resistance amplifier is assured provided:

*Total Circuit Inductance* $< |-R_D| |-R_D| C_D$

An amplifier using a film disc resistor $R_I$, designed for 6-*db* of gain and obeying these stability criteria was built in a coaxial structure. This, together with its voltage insertion gain versus frequency characteristic, is illustrated in Figure 6. The input impedance of the amplifier remained slightly capacitive below 400 *Mc* and its real component gradually decreased from 50 ohms at 1 *Mc* to about 10 ohms at 400 *MC*. The insertion gain measurements were made as shown in Figure 7, with the negative resistance amplifier placed between two 10-*db*, 50-ohm pads. The input voltage was measured with a high-impedance probe* and the output with a 50-ohm probe terminating the output pad. Two measurements were made, the first with the amplifier inserted as shown, and the second with the amplifier replaced with a through connection. The gain shown in Figure 6 is the difference between the two measured losses. The output voltage was held to 10-*mv rms* to avoid compression effects.

It can be seen from Figure 3, that if the voltage excursion across the diode is too high, voltage compression takes place. In all these experiments, the maximum allowable voltage across the diode was 20-*mv rms*.

Another amplifier, designed for 6-*db* of gain at low frequency, having a complex impedance $Z_I$ replacing the disc resistor $R_I$, was built. As seen in Figure 8, the reactive element of this impedance is a short-circuited transmission line whose input is shunted with a disc resistor. By adding this inductance to the input circuit, the gain was peaked at the high frequency end, as shown in Figure 8. The variation of amplifier input impedance with frequency was not so marked as in the previous amplifier, though its shape was similar, decreasing to 20 ohms at 400 *Mc*.

* Boonton model 91 CA.

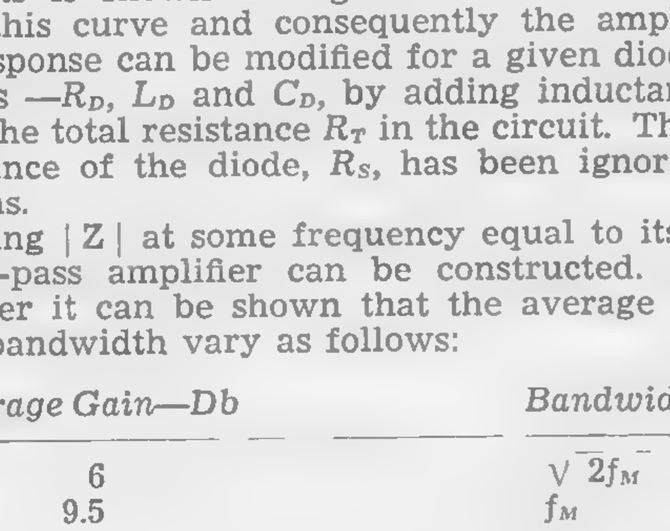


**Figure 1—Negative resistance amplifier. The term $R_I$ in the denominator should be $R_D$.**

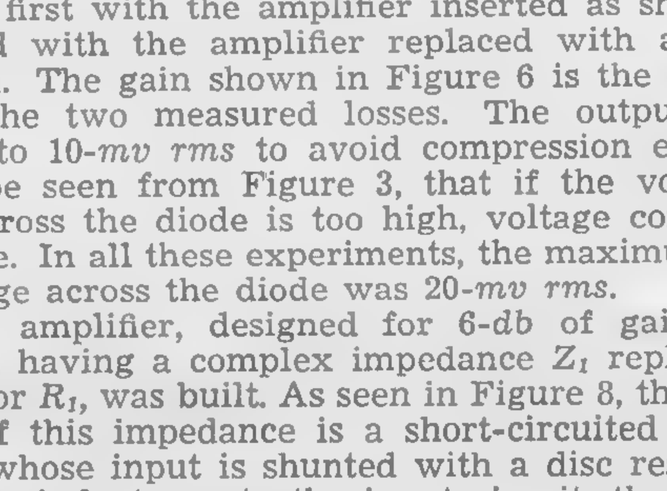


**Figure 2—Matched negative resistance amplifier.**

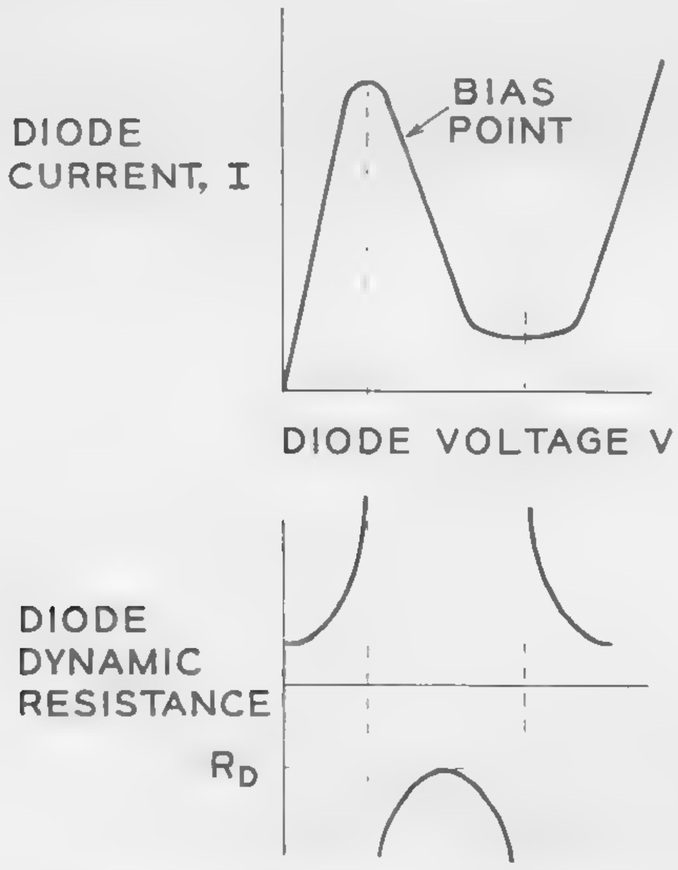


Figure 3—*Esaki*-diode characteristics.

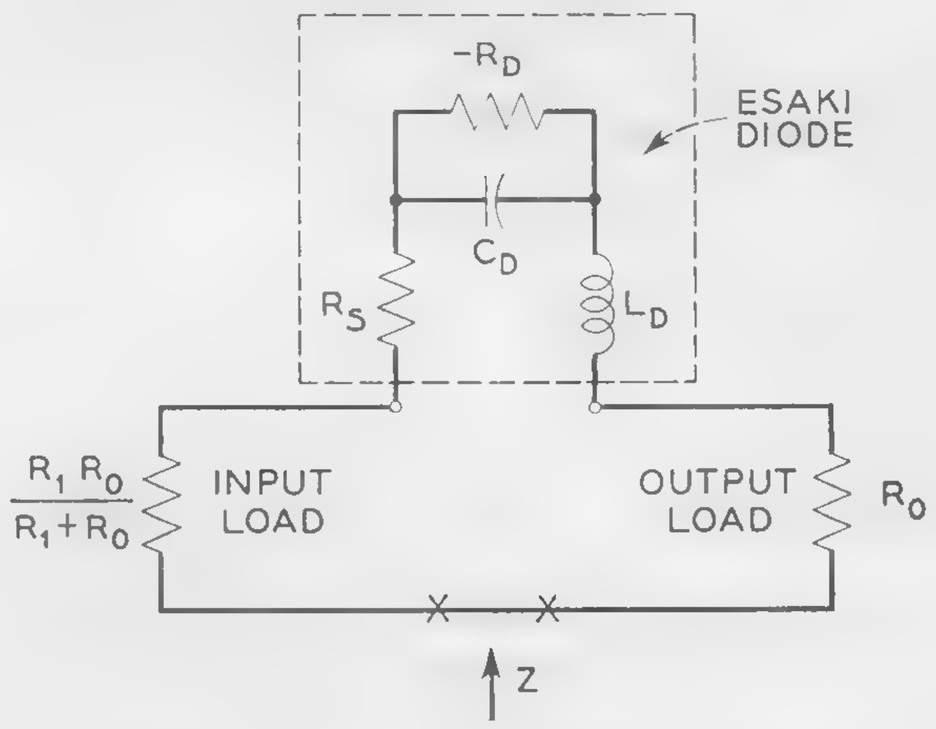


Figure 4—Equivalent circuit of *Esaki* diode with resistive loads.

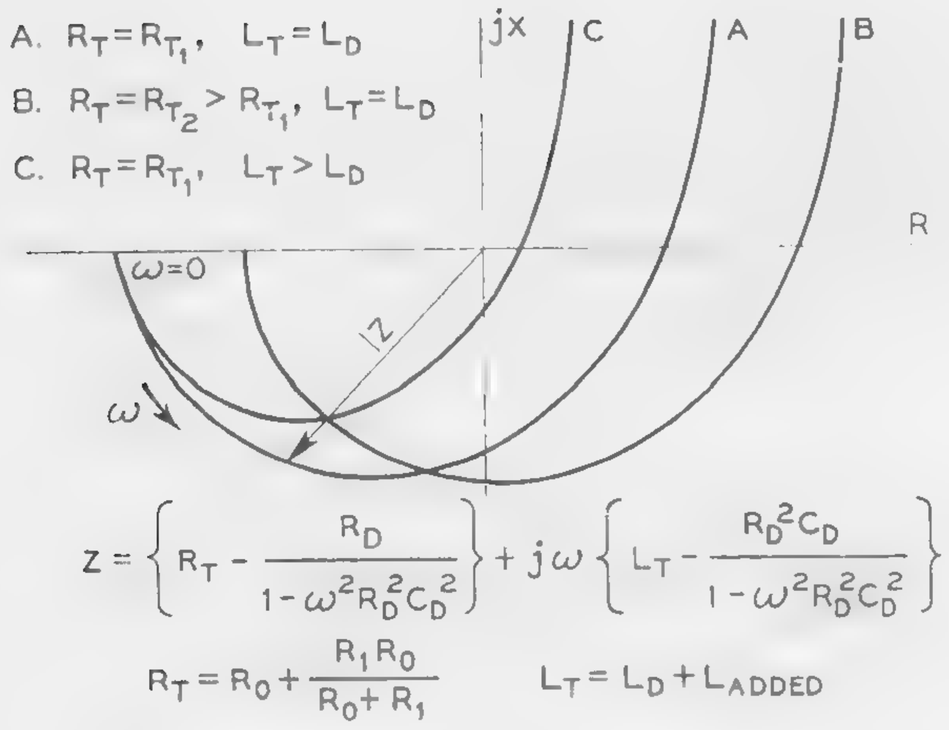


Figure 5—Calculated impedance *Z* of *Esaki* diode and load showing variations with external parameters *R* and *L*.

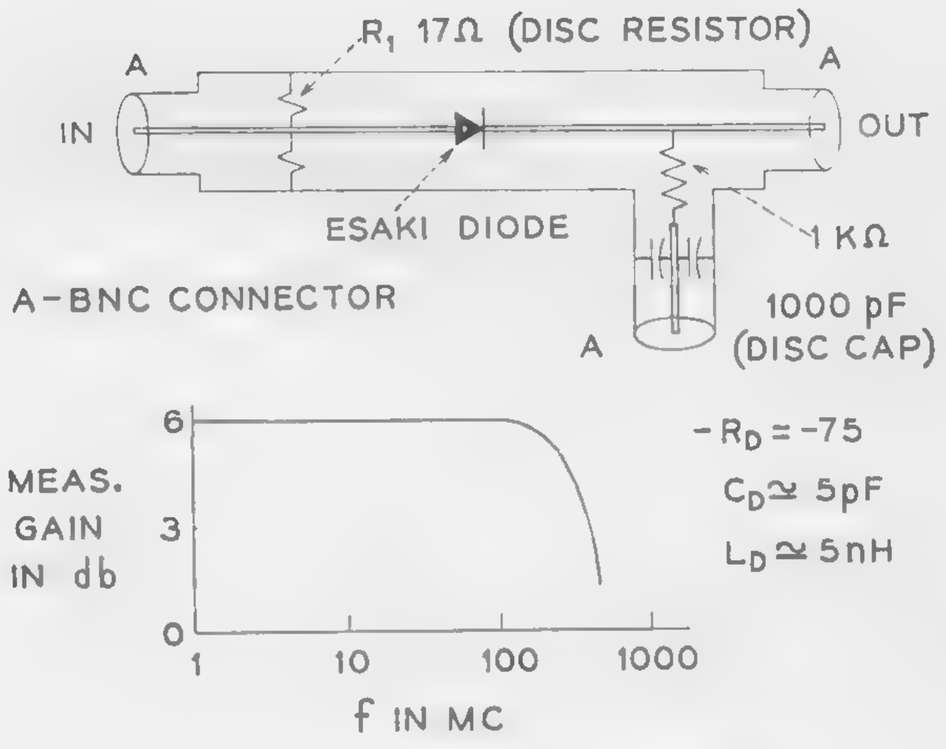


Figure 6—*Esaki* diode coaxial amplifier.

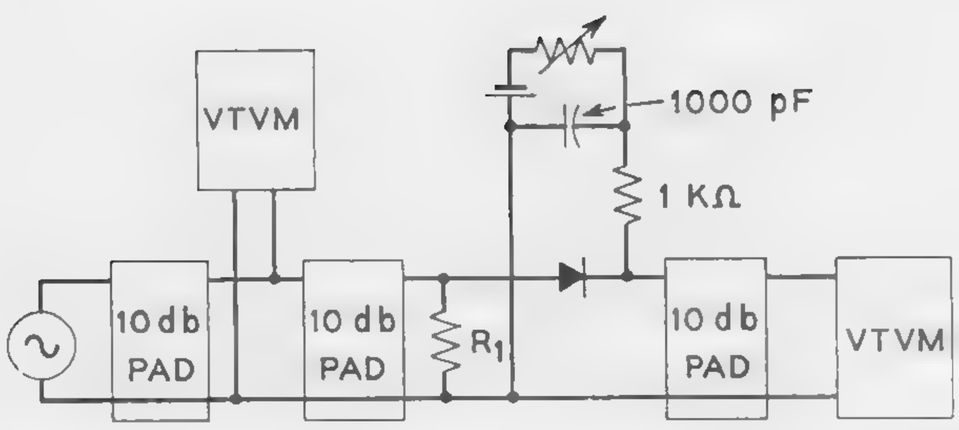


Figure 7—Experimental arrangement for determining gain of *Esaki*-diode amplifier.

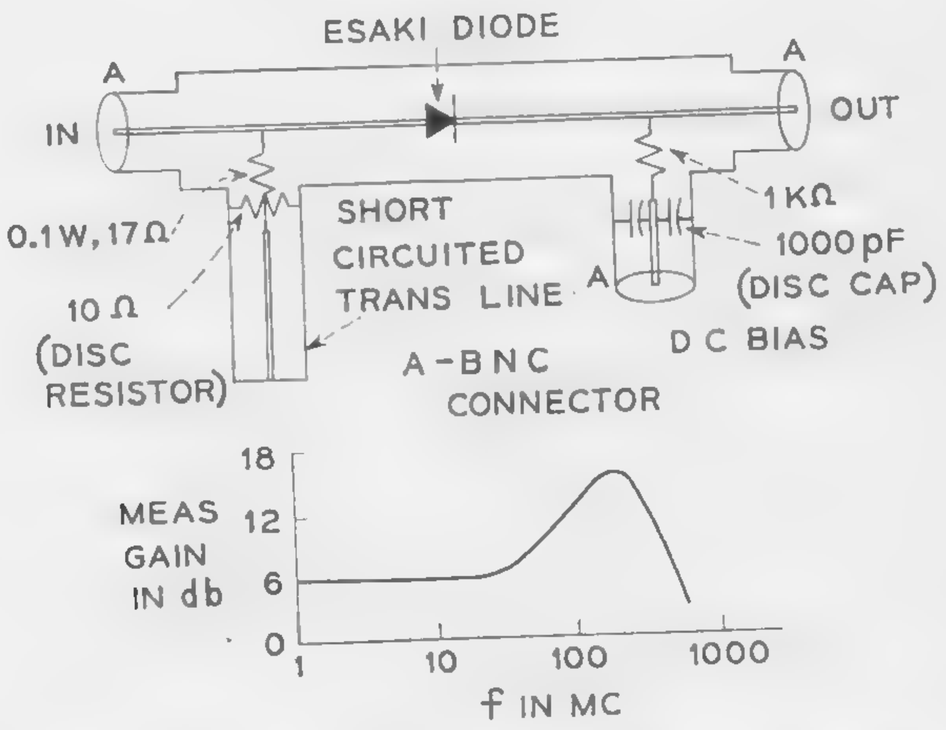


Figure 8—*Esaki*-diode coaxial amplifier with shunt peaking.

## SESSION IX: Communication Circuits and Techniques

### 9.3: High-Speed Analog-to-Digital Converters Utilizing Tunnel Diodes

R. A. Kaenel

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Murray Hill, N. J.

TWO ANALOG-TO-DIGITAL CONVERTERS, which combine the functions of an amplitude discriminator and memory in a tunnel diode pair per bit, have been devised. In addition, one of the two schemes utilizes each tunnel diode pair as a delay element. The conversion speed of the six bit converters which employ germanium *2N559* transistors and gallium arsenide *1N651* tunnel diodes has been set to 5 *Mc.* Higher conversion rates are possible, but not required in the present application. The use of tunnel diodes presents a significant improvement in the art of converter design by virtue of circuit simplicity and performance.

Over the years high speed analog-to-digital converters have enjoyed a rapidly increasing demand. Digit-at-a-time converters, of the kind which will be described in this paper, have many advantages over other schemes. For one, the speed requirement on the various components is not as high as in other principles of conversion. Another important factor is that conventional multipurpose elements such as diodes and resistors can be used to implement the principle.

Without going into the various details of the basic building block,* the fundamental converter functions are introduced with Figure 2. Briefly, the circuit operation is as follows. Assume that all bottom tunnel diodes reside in their high voltage state designated *O* and the top diodes accordingly in their low voltage state. Let the signal input cause a control current at the tunnel diode-pair tie point to flow in the outward direction. To initiate a conversion cycle, a conversion trigger drops the bottom diode of the highest order digit, which is connected to the weighting resistor, *R* to its low voltage state designated *1*. This causes the control current to decrease by a well-defined amount through the inverter, which has been added for the sake of the subsequent discussion only. With the power-supply voltage of a magnitude which in the quiescent condition permits only one diode to reside in its low voltage state, the current through the inductor of the first stage will gradually increase. Both diode currents will converge towards the diode characteristic peak current, timed by the inductor value. Depending on the control current one of the two diodes will reach its peak current first and immediately switch to its high voltage state. Although the decision is sensitive to minute control currents, the decision reached is unaffected by large control current fluctuations, especially those due to testing of lesser significant digit stages.

The discrimination process across the inductor causes a fast jump of voltage due to one diode switching. This voltage transition, differentiated and inverted, can be used to initiate the testing of the second most significant digit stage connected to the weighting resistor *2R*. Accordingly, the other digits are tested to complete one conversion cycle. Conversion of a highly positive signal performs the reset operation simply and reliably.

Removing the timing function from the intrinsic converter and associating transistor switches for current amplification to each stage results in the Figure 3 schematic. The regular diodes modify the high diode-pair load resistor to insure that each high and low voltage state is occupied by only one tunnel diode in the quiescent condition.

In conclusion, it was found that the second of the two circuits was remarkably simple to assemble; 10% tolerances could be accepted on all components with exception of the weighting resistors. The combination of gallium arsenide diodes with germanium transistors affords adequate margins to allow losses both in voltage swing for speed-up and for strong transistor cut-off, by means of germanium diodes connected to the transistor emitters. It is hoped that the future will soon bring tunnel-diode pair units, eventually including a transistor switch. This would further reduce the size of the already small converter board.

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* Kaenel, R. A., "High Speed Analog-to-Digital Converter Utilizes Tunnel Diodes," *IRE PGEC Transactions;* 1961.

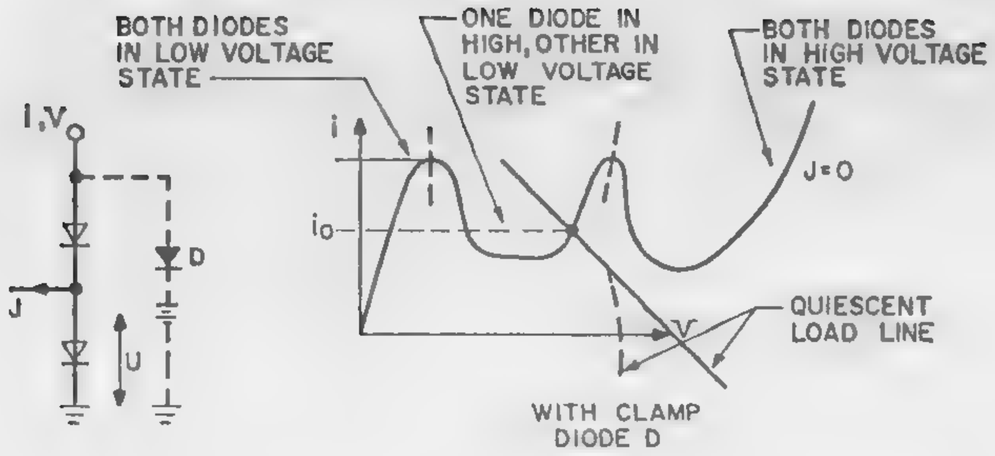


**Figure 1*a*—Composite characteristic of two series-aiding tunnel diodes. The load line of an imaginary resistor has been added to illustrate the effect of a clamping diode *D*.**

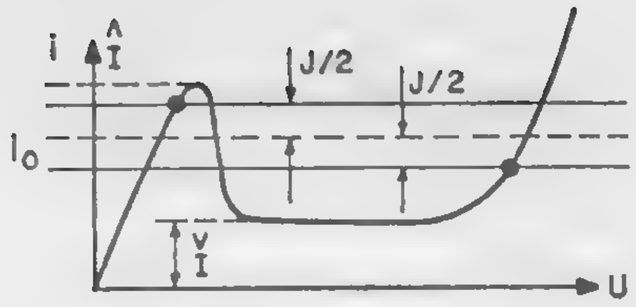


**Figure 1*b*—Quiescent conditions of two diodes in a pair. Uncritically small currents *J* cannot affect the state of the two diodes.**

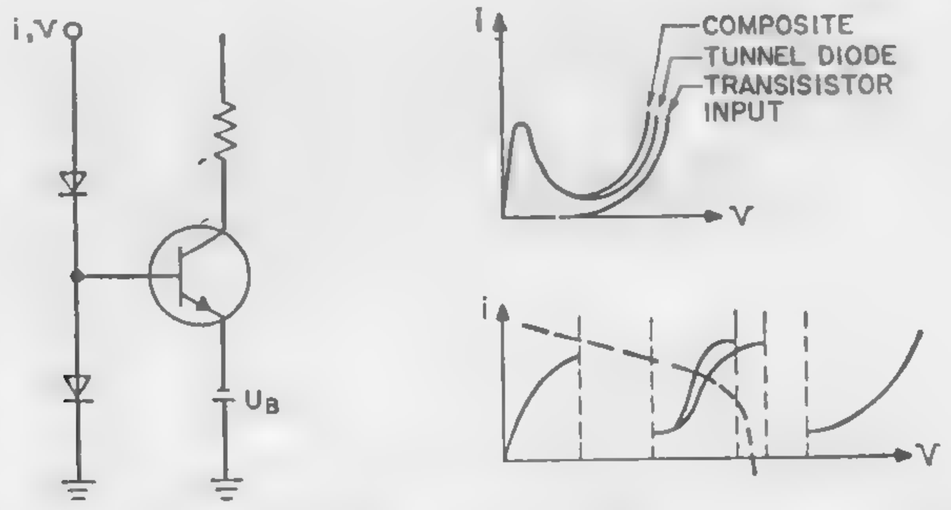


**Figure 1*c*—Composite characteristic of two series-aiding tunnel diodes and one transistor. Because of transistor loading, the center stable characteristic portion splits into two branches.**

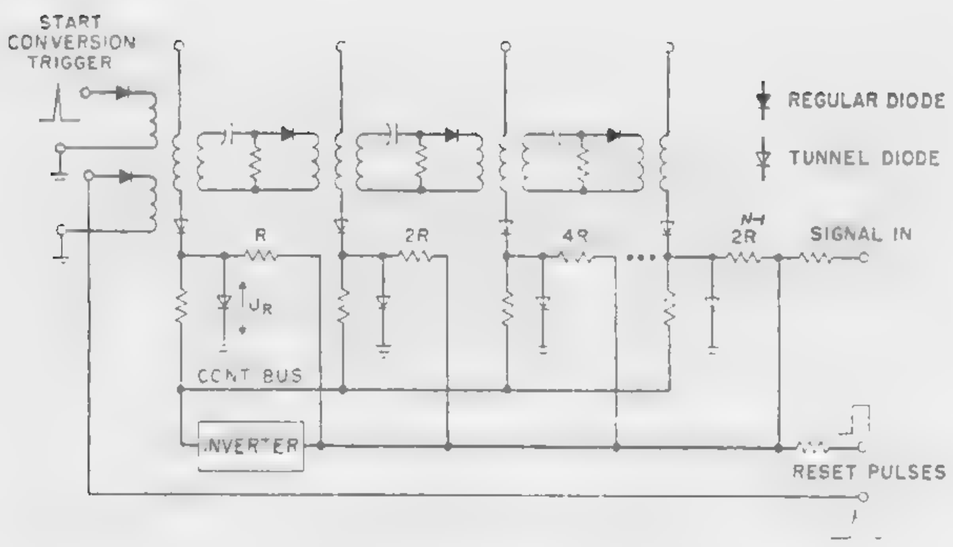


**Figure 2—Basic sequential analog-to-digital converter utilizing inductive tunnel-diode pair load to achieve monpulser timing action. The trailing pulse edge of one stage is coupled to the subsequent stage to initiate digit testing.**

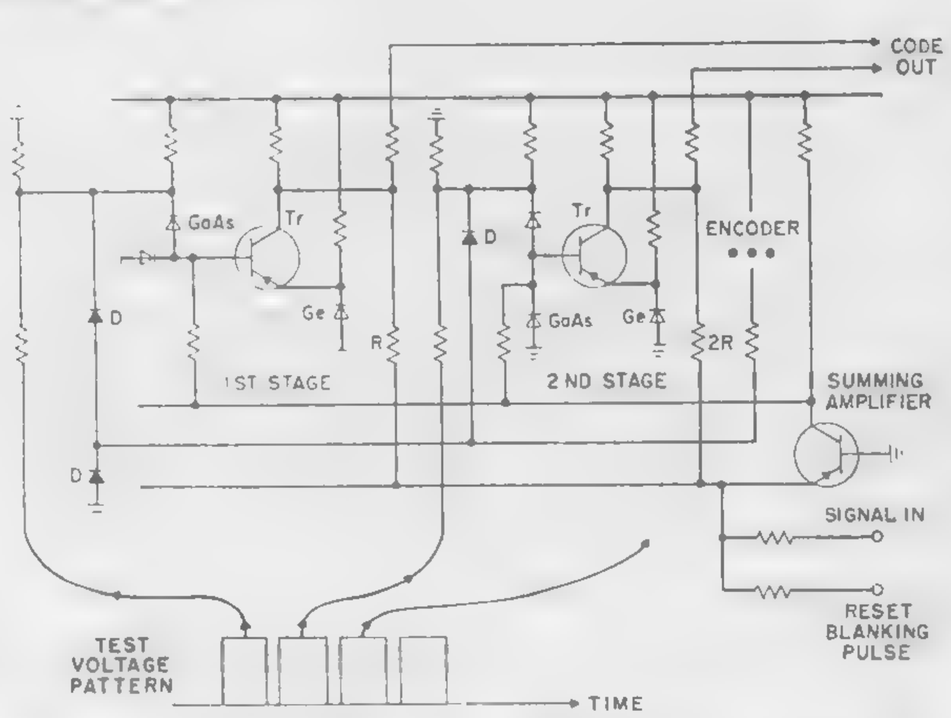


**Figure 3—Basic sequential analag-to-digital converter with externally generated test voltage pattern for each tunnel diode pair. Germanium tunnel diodes are used in the transistor emitters for biasing.**

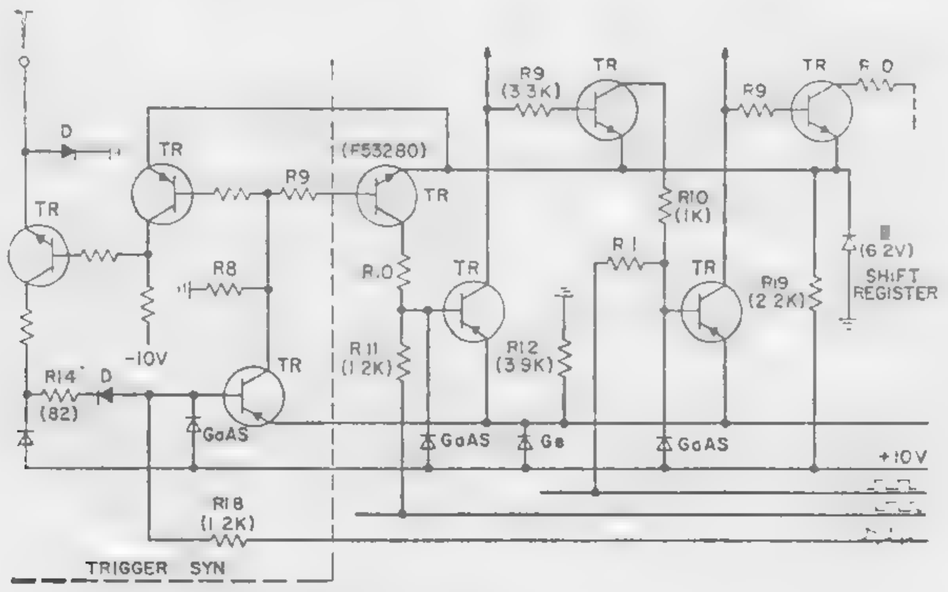


**Figure 4—Shift-register arrangements to generate test voltage pattern for the basic converter.**

## SESSION IX: Communication Circuits and Techniques

### 9.4: Superregenerative Circuits Using Tunnel Diodes

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Research Div., Philco Corporation

Philadelphia, Pa.

CONSIDERABLE DIFFICULTY has been experienced by tunnel-diode circuit designers in attempting to bias the tunnel diode in the negative-resistance region and still maintaining a reasonable degree of stability. In the superregenerative circuit we may bias the tunnel diode outside of the negative resistance region, as shown in Figure 1, and periodically permit the operating point to be driven into the negative resistance region. The initial operating point may be in the forward or reverse voltage region depending upon the quench magnitude. During the excursion into the negative resistance region, provided that the net circuit resistance during this time is negative, the circuit will become oscillatory and will build up at a rate which is a function of the circuit parameters. If a small signal is injected into the resonant circuit, the rate of oscillation buildup will be a function of the input signal magnitude. Therefore, it is desired that the natural rate of oscillator voltage buildup be relatively slow. The requirements for various modes of oscillation (i.e., sinusoidal, relaxation) for a device having a negative resistance characteristic have been previously derived[1]. This analysis has been extended to include the tunnel diode by assuming a cubic relationship between diode current and voltage. It is shown that the voltage-time relationship for a negative resistance device, as shown in Figure 2, is given by the differential equation shown therein. $R_N$ is the value of the negative resistance at the *dc* operating point and $R$ includes the tank loss and load resistance. The character of the buildup of the oscillator voltage is highly dependent upon the magnitude of $\epsilon$ and it may be shown[1] that for $\epsilon \geq 1$, the buildup is of a relaxation type while for $\epsilon \leq 0.1$ the voltage is sinusoidal with a slow buildup.

The tunnel diodes available at the time of this investigation had negative resistances on the order 200 ohms. Operation at 4 *Mc*, with a reasonable minimum value of oscillator tank inductance taken as 1.5 $\mu h$, required a tuning capacitance of 1000 $\mu\mu f$ to obtain satisfactory operation. The diagram of an externally quenched superregenerative circuit, using a separate diode detector, is shown in Figure 3. The bias and quench drive are adjusted as shown in Figure 1. Voltage gain was taken as the ratio of the audio output amplitude to the amplitude of the input modulation envelope. For the circuit shown, voltage gains of approximately *300* were obtained.

Self-quenching can be obtained by replacing the audio quench oscillator and 1-*mh* choke with a low-frequency resonant circuit and series resistance (shown dotted in Figure 3). The bias now is placed in the negative resistance region and the resulting low-frequency oscillation effectively serves as the quench signal. Voltage gains using self-quenching were approximately *250*.

Calculation of voltage gains may be performed using expressions derived by *Whitehead*[2] for the linear mode of operation with a conductance versus time variation which passes through zero with a finite slope as shown in Figure 4. Here gain is defined as the ratio of oscillator amplitude buildup to amplitude of injected signal across the passive tank circuit. Assuming a sinusoidal conductance variation, values of theoretical voltage gains may be calculated as a function of the minimum value of negative resistance obtained during the quench cycle. A plot of this characteristic is given in Figure 5, where a rapid increase in gain is observed for decreasing values of diode negative resistance. In actual practice, however, to maintain a reasonable value of $\epsilon$ (Equation 2) it is necessary to increase $C$ and therefore the expected increase in gain will not be achieved.

In the circuits tested the lower measured voltage gain (*300*) may be attributed to poor rectification efficiency of the detector at the low levels of operation (approximately 20 *mv*) and departure from sinusoidal conductance-time variation due to the nonlinear conductance versus voltage characteristics.

Sensitivity limitation due to noise factors was not considered. Improved fabrication techniques resulting in lower values of $R_S$ and $L_S$ should extend the frequency range of operation using the same type of analysis. Lower values of $R_N$, however, may require impractical $L/C$ ratios for proper oscillatory build-up. Low-operating level also seems to be a practical limitation in the superregenerative application of tunnel diodes.

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[1] Van der Pol, B., "The Nonlinear Theory of Electric Oscillations," *Proc. of the IRE*, p. 1051-1086; 22, 1934.

[2] Whitehead, J. R., "Superregenerative Receivers," *University Press*, (Cambridge), p. 52; 1950.

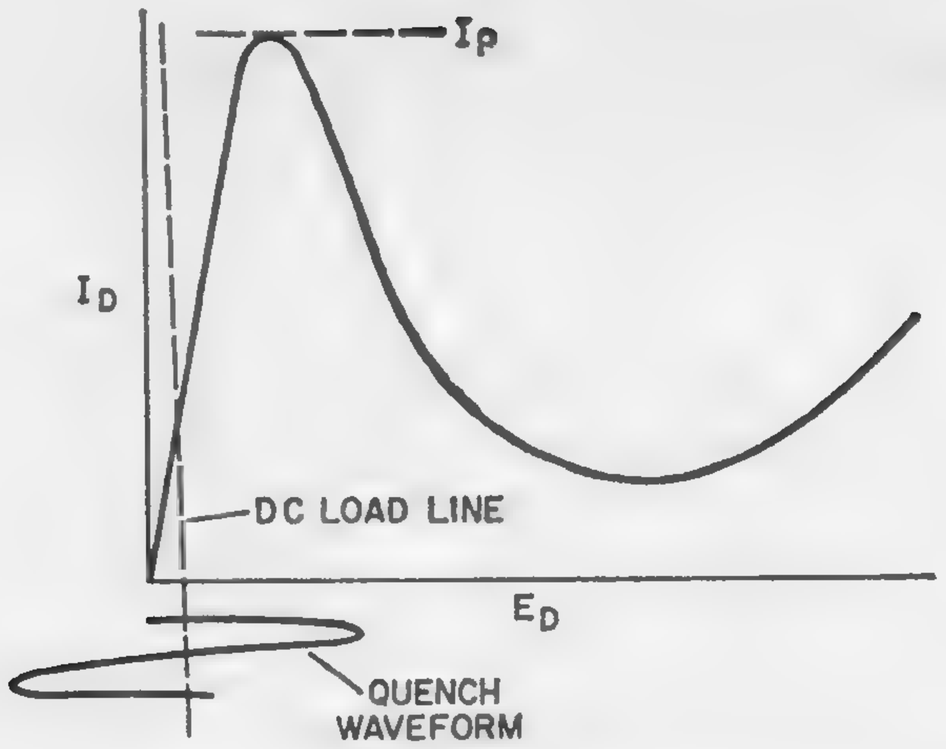
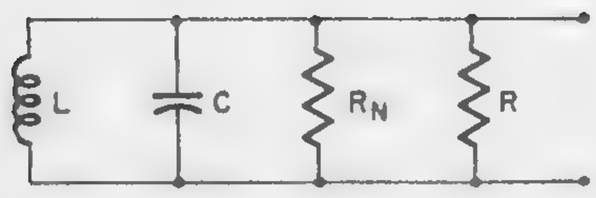



**Figure 1—Tunnel-diode voltage-current characteristics and quench waveform. The bias is placed in the positive resistance region and periodically driven into the negative resistance region by a quench waveform to produce oscillation.**




$$(1)\quad \frac{d^2V}{d\tau^2} - \epsilon(1-V^2)\frac{dV}{d\tau} + V = 0 \qquad (2)\quad \epsilon = \sqrt{\frac{L}{C}}\left[\frac{1}{R_N} - \frac{1}{R}\right]$$

WHERE $\tau = \omega_0 t$

$$\omega_0 = \sqrt{\frac{1}{LC}}$$

$$\epsilon \approx \sqrt{\frac{L}{C}}\left[\frac{1}{R_N}\right] \leqq 0.1$$

**Figure 2—Equivalent circuit and conditions for sinusoidal oscillatory voltage buildup. For slow, sinusoidal voltage buildup rather than relaxation type oscillation $\epsilon$ should be less than unity.**

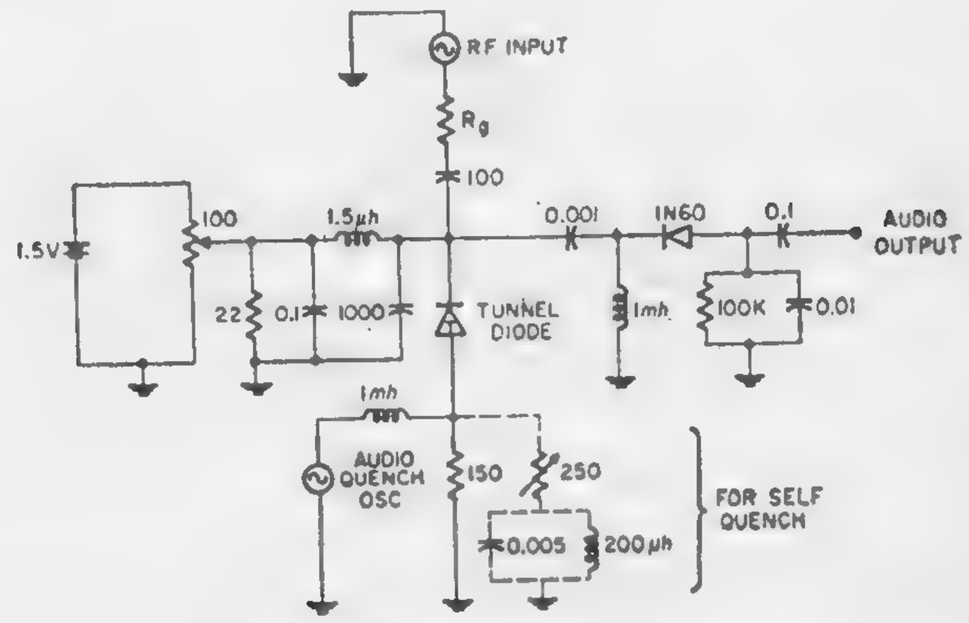
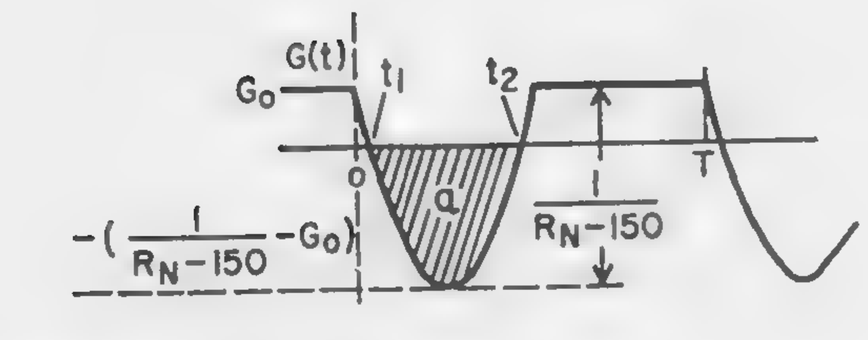



**Figure 3 — Externally-quenched superregenerative amplifier and diode detector.**




$$\text{GAIN} = G_o\sqrt{\frac{\pi}{C[G'(t_1)]}}\,e^{\frac{a}{2C}}$$

$G_o$ = QUIESCENT TANK CONDUCTANCE = 500 $\mu$ MHOS
C = TANK CAPACITANCE = 1000 pf.
$G'(t_1)$ = SLOPE OF CURVE AT $t_1$
a = AREA UNDER NEGATIVE PORTION OF CURVE
−150 = MINIMUM RESISTANCE DURING QUENCH CYCLE

**Figure 4—Conductance variation and voltage-gain expression. The conductance-time variation is assumed to be sinusoidal in the negative resistance region, crossing the zero axis with a finite slope.**

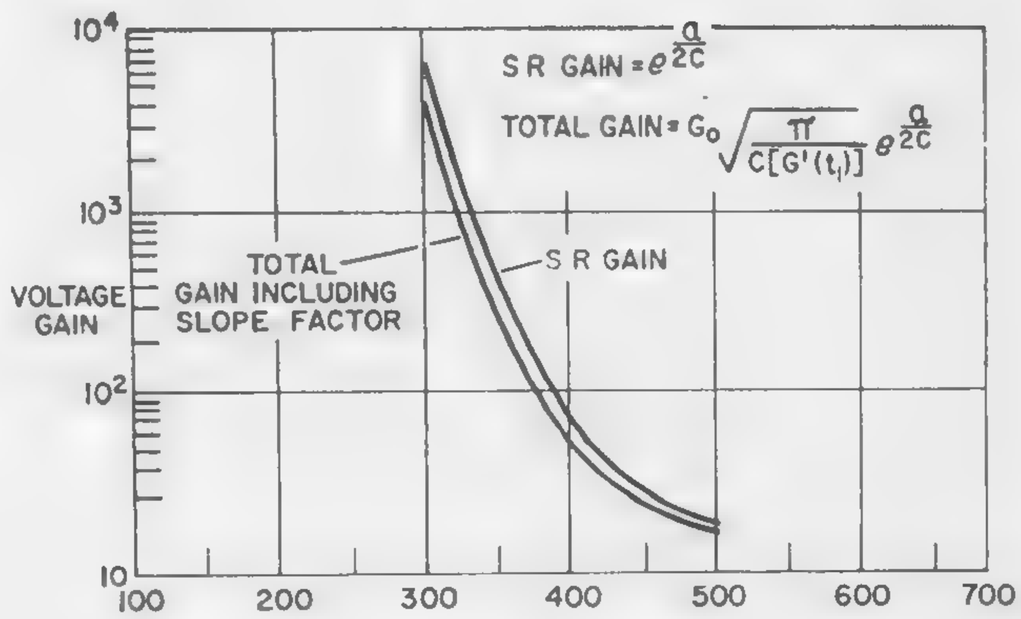



**Figure 5—Plot of superregenerative voltage gain versus negative resistance. These curves assume a constant value of capacitance, *C*, a condition difficult to fulfill and yet maintain a reasonable value of $\epsilon$.**

## SESSION X: Storage

Chairman: R. A. Henle
IBM Corporation, Poughkeepsie, N. Y.

### 10.1: A New Load-Sharing Matrix Switch

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IBM Corporation,
Poughkeepsie, N. Y.

A NEW WINDING PATTERN for load-sharing matrix switches which requires fewer independent windings on each transformer has been developed. This reduction in the number of windings on each transformer permits higher speeds, larger size switches, smaller size switch cores, simplified winding techniques, and more freedom in the selection of turns ratios.

A 32-input, 16-output switch has been built using the new winding pattern. This switch is to be used to supply read-write pulses of less than 100 *nsec* width to a high-speed core memory.

Load-sharing matrix switches are used in electronic systems where the power of the entire system must be available at any one of several outputs but, statistically, the average power over a long time at any one of these outputs is much less. In a conventional system, this requires many high-power generators or switches whose capabilities are never fully utilized. A method of selectively combining at any one of several outputs the power of several generators will substantially reduce the peak loading on each of the generators. Also, the average power requirements of any generator will be independent of where the power is utilized.

*G. Constantine* has developed such a device[1]. His switch consists of a group of transformers, each having several primaries and one secondary. Each input winding consists of one primary from each transformer connected in series. Figure 1*a* is a schematic of a small load-sharing matrix switch; it will be noted that the windings are grouped into complementary pairs.

In this switch, if we apply positive input current pulses to inputs *0* and *1*, the magnetomotive forces will add in core *0* and induce a positive output current in the load *0*. On core *1*, the magnetomotive forces will cancel and no current will flow in load *1*. At a later time, positive input current pulses will be applied to inputs *0* and *1*, causing core *0* to reset and inducing a negative output current to load *0*. Again, the magnetomotive forces will cancel in core *1*.

To select output *1*, we would initially apply drives to inputs *0* and $\bar{1}$ and then to inputs $\bar{0}$ and *1*.

A tabulation of the winding pattern of Figure 1 appears in *b* of this illustration. Here a *1* signifies positive mutual coupling between an input and an output, and a *0* signifies negative mutual coupling.

In Figure 2 is a tabulation of the winding pattern for a larger switch with four input pairs, each linking all four cores. Each core has one secondary. The table is divided into quadrants. Quadrants *1*, *2*, and *3* are identical to the entire table of the next smaller size switch, and quadrant *4* is the complement of the smaller table. This procedure can be continued to design switches with $2^n$ outputs and $2^n+1$ inputs.

*M. P. Marcus*[2] and *R. T. Chien*[3,4] have developed similar devices with fewer inputs for a given number of outputs by removing the requirement of using input windings in pairs. These switches require at least one independent winding on each core per output.

*L. Russell* has developed a switch utilizing summation of secondary voltages rather than summation of magneto motive forces. These switches require two primary windings and several secondary windings on each core. The total number of windings is approximately the same as those used in the *Marcus* and *Chien* design.

Figure 3 shows a 4-pair input, 4-output switch with the new winding pattern. This switch utilizes both summation of primary magnetomotive forces and summation of secondary voltages. In this example, each primary winding links half the cores, and each secondary winding links two cores. The minimum number of independent windings on a core is approximately *3 x;* square root of number of outputs. This type of switch requires that some of the cores be capable of producing either positive or negative pulses. The primary windings may be connected in any of the patterns developed by *Constantine, Marcus,* or *Chien.* The input-output table can be made identical to those of *Constantine,* or can be a slight modification of *Marcus* or *Chien.*

Figure 4 illustrates the minimum number of independent windings on a core for the five types of switches discussed in this paper. Figures 5 and 6 show a load-sharing switch with primary winding based on the *Marcus* and *Chien* developments.

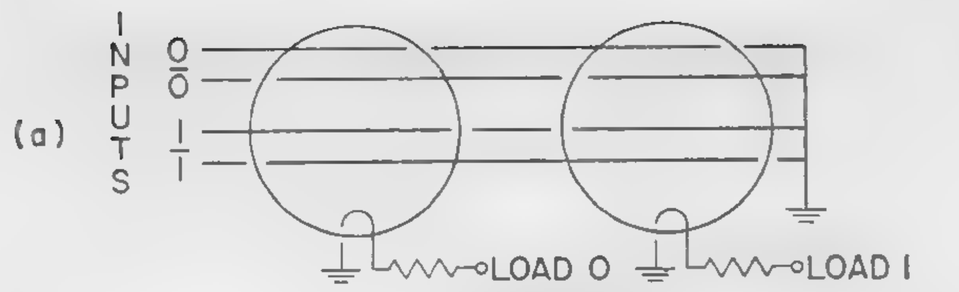
---

[1] Constantine, Jr., G., "A Load-Sharing Matrix Switch" *IBM J. Res. Dev.*, p. 204-211; July, 1958.

[2] Marcus, M. P., "Doubling the Efficiency of the Load-Sharing Matrix Switch," *IBM J. Res. Dev.*, p. 194-196; April, 1959.

[3] Chien, R. T., "A Class of Optimal Noiseless Load-Sharing Matrix Switches," *IBM J. Res. Dev.*, p. 414-417, Oct., 1960.

[4] Chien, R. T., "Orthogonal Matrices, Error-Correcting Codes and Load-Sharing Matrix Switches," *IRE Transactions on Electronic Computers*, p. 400; Sept., 1959.




(b)

| INPUTS | OUTPUTS 0 | 1 |
|---|---|---|
| 0 | 1 | 1 |
| 0̄ | 0 | 0 |
| 1 | 0 | 0 |
| 1̄ | 1 | 1 |

**Figure 1—*(a)* A small load-sharing matrix switch of the type designed by *G. Constantine*. *(b)* Tabulation of windings of this switch.**

| INPUTS | OUTPUTS 0 | 1 | 2 | 3 |
|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 |
| 0̄ | 0 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 |
| 1̄ | 0 | 1 | 0 | 1 |
| 2 | 1 | 1 | 0 | 0 |
| 2̄ | 0 | 0 | 1 | 1 |
| 3 | 1 | 0 | 0 | 1 |
| 3̄ | 0 | 1 | 1 | 0 |

**Figure 2—Tabulation of windings of a larger size matrix switch expanded by *Constantine's* method.**

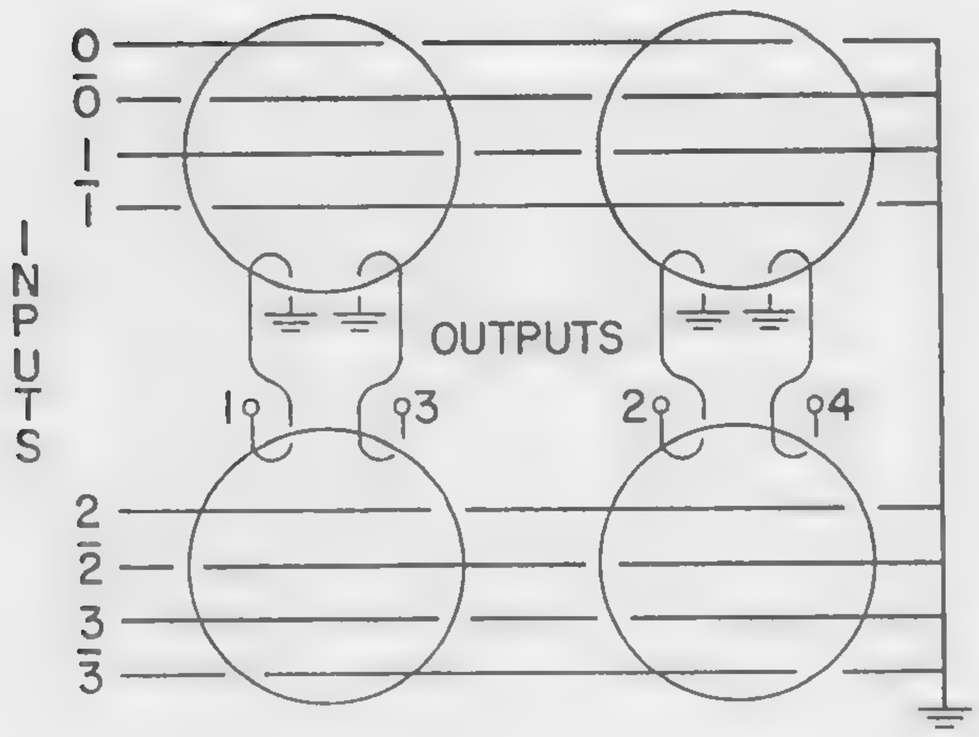



**Figure 3—A load-sharing matrix switch based on the tabulation of Figure 2, but wound according to the new winding pattern.**

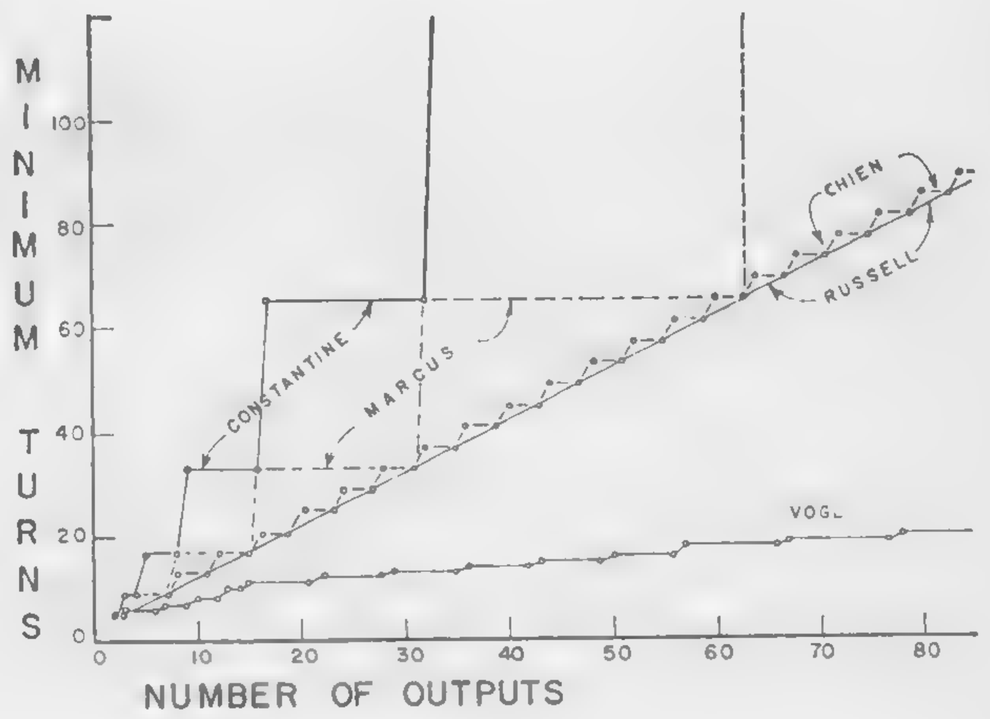



**Figure 4—Comparison of the minimum number of independent windings needed to build various sizes of switches according to five design procedures.**

| INPUTS | OUTPUTS 0 | 1 | 2 | 3 | 4 | 5 |
|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| 2 | 0 | 1 | 0 | 0 | 1 | 0 |
| 3 | 0 | 0 | 1 | 0 | 0 | 1 |
| 4 | 1 | 1 | 1 | 0 | 0 | 0 |
| 5 | 1 | 0 | 0 | 0 | 1 | 1 |
| 6 | 0 | 1 | 0 | 1 | 0 | 1 |
| 7 | 0 | 0 | 1 | 1 | 1 | 0 |

**Figure 5—Tabulation of an 8-input, 6-output load-sharing matrix switch to use new winding scheme. Primaries are wound according to the *Marcus* and *Chien pattern*.**

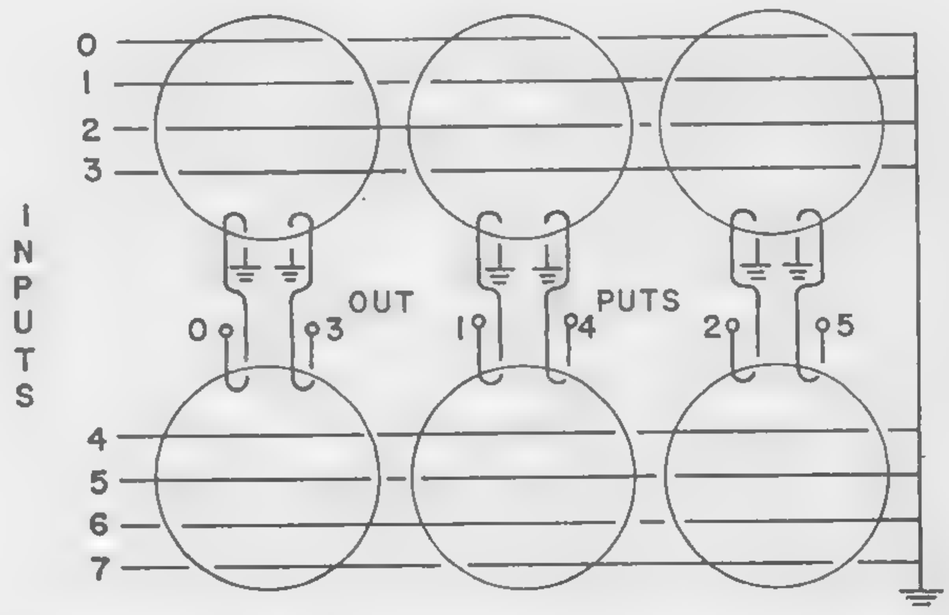



**Figure 6—The 8-input, 6-output load-sharing matrix switch.**

## SESSION X: Storage

### 10.2: A 12-Kilobit, 5-Microsecond Twistor Variable Store

W. B. Gaunt, Jr. and D. C. Weller

Bell Telephone Laboratories, Inc.

Murray Hill, N. J.

In 1957, A. H. Bobeck disclosed the invention of the twistor[1]. Two years ago, *Preston* and *Simkins* described a small buffer store[2]. To date some five different storage designs are complete and in manufacture. Twistor memory and store technologies have evolved along with this development program to a point where the performance limits of the twistor are becoming clear, and the potential of the device can be estimated.

In this paper, a 5-$\mu$sec, 512-word, 24-bit twistor store will be described, noting special design techniques applicable to twistor stores so that those who are experienced in store art will be able to judge the value of the twistor as a competitor with other contempory storage media. In the memory unit, (Figure 1), 30 twistor-copper pairs, 15-feet long are encapsulated in a mylar belt. Single-turn solenoids are wrapped around this belt and closed through ferrite cores. This assembly is then folded so that the cores form a 16 x 32 array. The access portion of the store (Figure 2) functions to select one of these cores and is conventional in form.

Since the twistor wire is used for both writing and sensing, suppression of the writing pulse is needed. This is accomplished by pairing a copper wire with the twistor wire, constituting a balanced system. Two currents are balanced: (*1*)-*A wire-bias* current which biases the twistor in the read direction and (2) a *bit-select* (reverse) current which writes on the twistor in coincidence with current flowing in the selected word solenoid. Both of these currents are independently controlled by reference voltages multipled to the *write drivers*.

Even with the use of a balancing scheme, the current pulses can never be totally suppressed. With a practical 26-*db* longitudinal balance, transverse write components ten times the 10 millivolt "*ONE*" can occur. By a combination of large dynamic range and broad bandwidth in the *read detector*, distortionless information signal amplification results. The *dc* level shift caused by temporary transient overload and the unsuppressed write component is reduced by at least 30 *db* by a clamp circuit. A strobe signal operates the clamp and is timed to take full advantage of the greater one-to-zero ratio beyond peaking time. Thresholding, regeneration and buffering complete the pulse regeneration.

Twistor wire is being produced today with a ninety per cent yield and coercive force is held to eleven per cent. This uniformity is not degraded in the memory because of the addition of a simple conductor pattern etched from copper clad laminate that is placed in registration with the word solenoid. As a result, bit interaction effects have been reduced to insignificance. The effects of ambient fields, which otherwise amounted to an equivalent ten per cent variation in coercive force, have also been reduced by at least a factor of *10* by a mu-metal shield around the memory. Using the most stringent program of stored data and all memory biases nominal, a measured threshold range for the entire store in excess of $\pm 24\%$ is typical. This is a measure of the worst signal-to-noise ratio of the entire store.

A comparison of end-of-life stabilities and the measured margins of the store is shown in Figure 5. With the special attributes of the *read detector*, the store operates successfully in the presence of post-write transients at cycle times as short as 4.2 $\mu$*sec*. Above 4.2 $\mu$*sec*, the margins improve rapidly so that at the design objective (5.0 $\mu$*sec*) the margins are adequate for a ten year life without readjustment.

The potential of the twistor is indicated by its competitive performance after three years of development, and because of a number of promising avenues of improvement such as precision transmission balance, closer bit packing, zero cancellation and reduced word spacing that have not yet been exploited.

***Acknowledgments***

The authors acknowledge with gratitude the help and encouragement of *T. R. Finch* and *E. A. Irland* in the *store development program* and the preparation of this material.

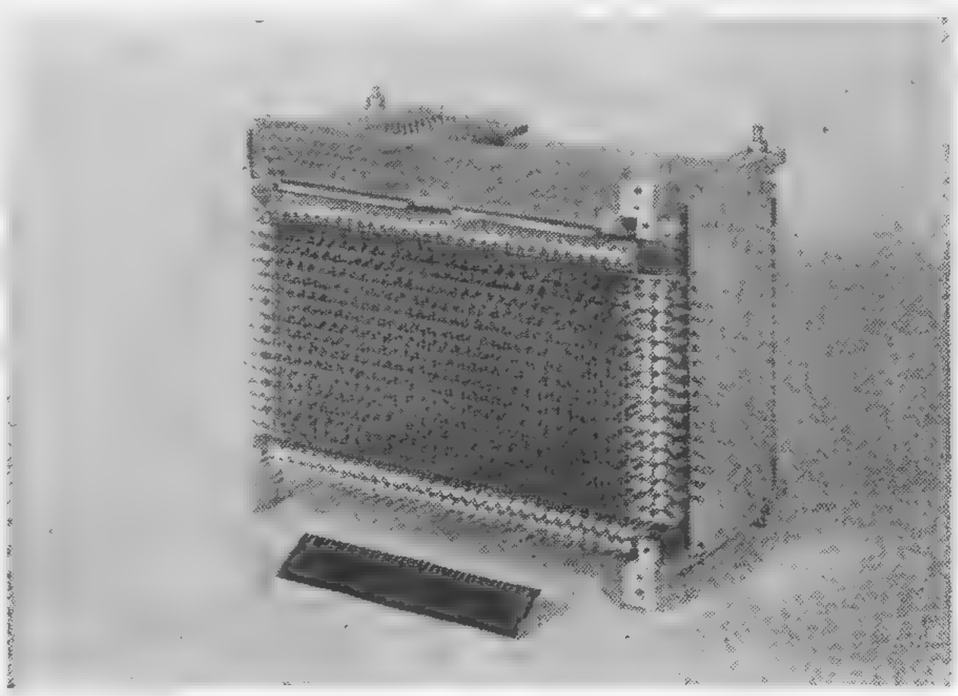


**Figure 1 — Memory unit with mu-metal shield removed.**

[1] Bobeck, A. H., "A New Storage Element Suitable For Large Sized Memory Arrays—The Twistor," *BSTJ*, p. 1319-1340; November, 1957.

[2] Preston, K., and Simkins, Q. W., "Twistor Buffer Store," International Solid-State Circuits Conference, *Digest of Technical Papers;* February, 1959.

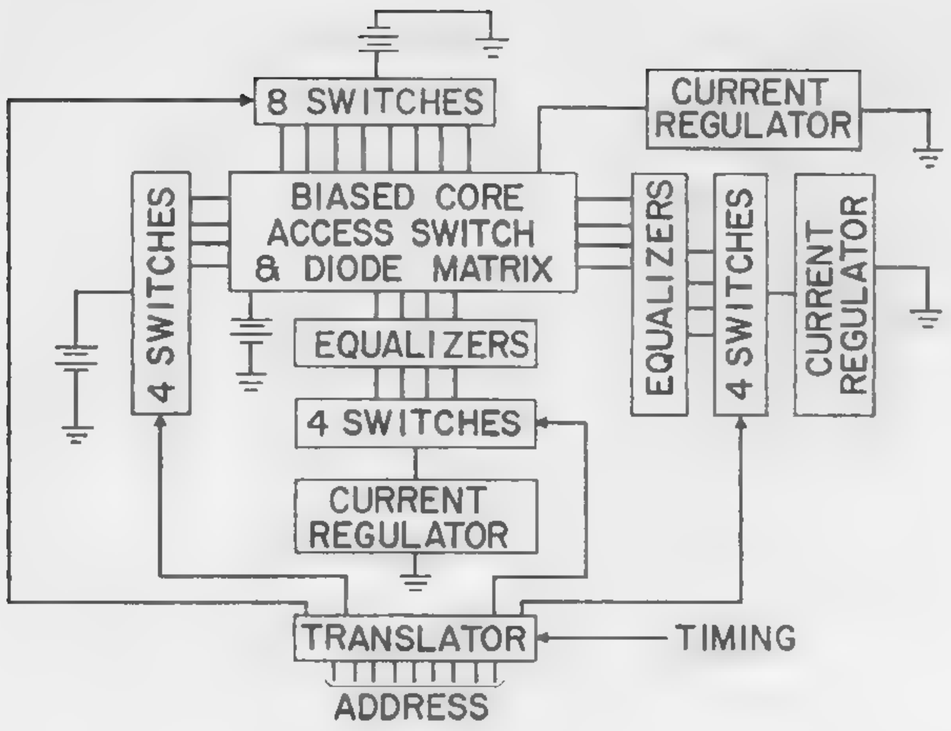



**Figure 2—The biased core switch in the memory unit, diode matrix and 0.6-ampere pulse circuits which constitute the *access* portion of the store.**

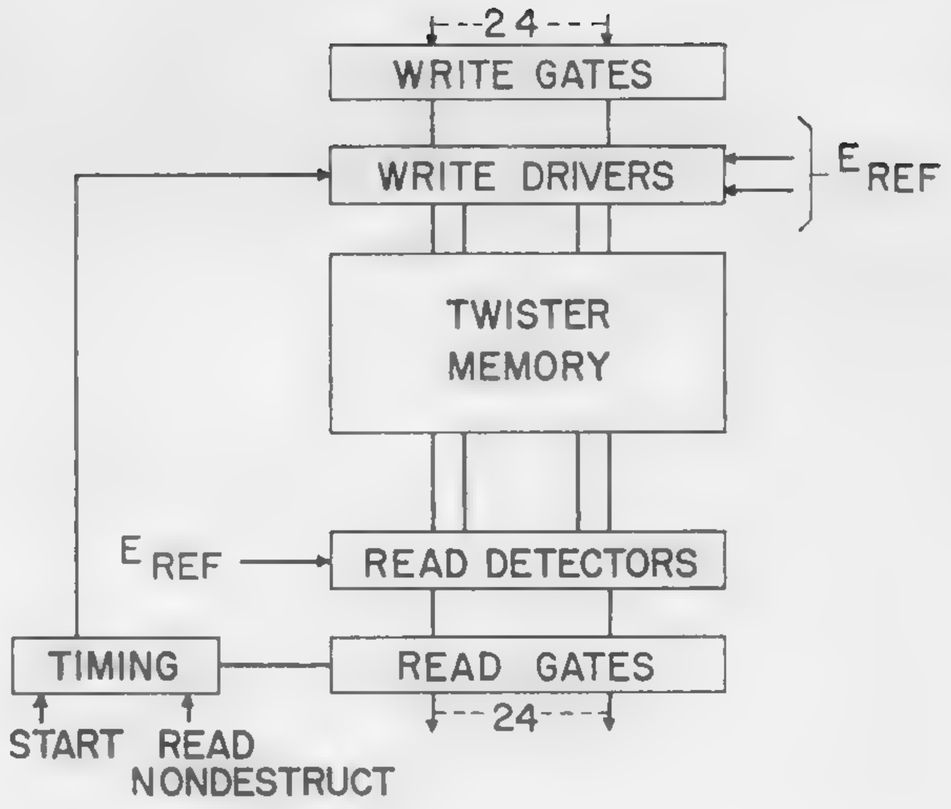



**Figure 3—The *data* portion of the store which consists of the storage elements of the memory, read and write circuits.**

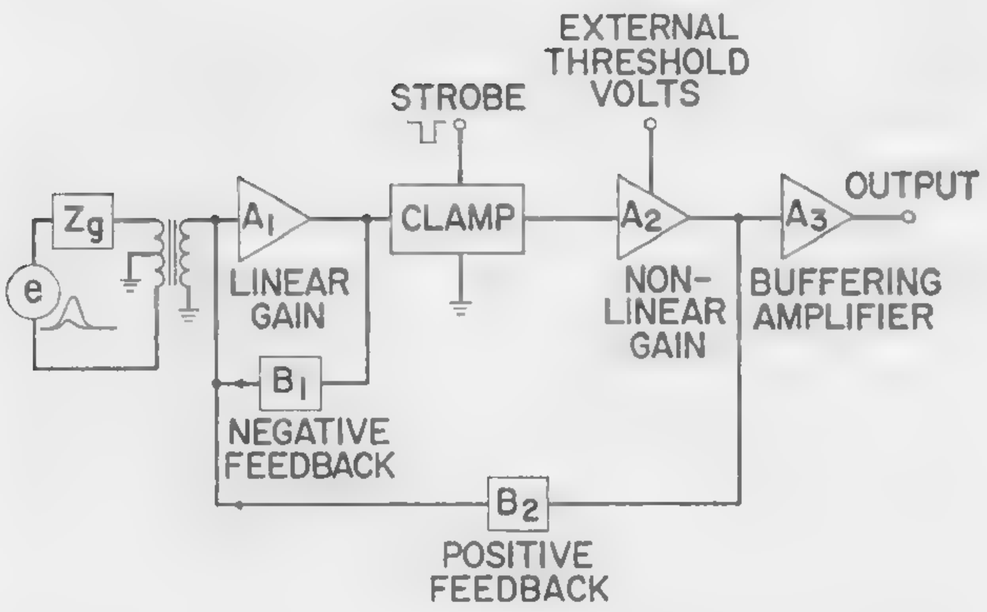



**Figure 4—The read detector which employs four mesa-type transistors and two diodes.**

| | CIRCUIT STABILITY | MEASURED MARGINS |
|---|---|---|
| BIT SELECT CURRENT | ±5% | ±21% |
| TWISTOR BIAS CURRENT | 6 | 53 |
| WORD SELECT CURRENT | 5 | 16 |
| ACCESS CORE BIAS CURRENT<br>BUFFER BIAS CURRENT | 3 | 11 |
| THRESHOLD | 1.5 | 24 |

**Figure 5—Summary of store margins.**

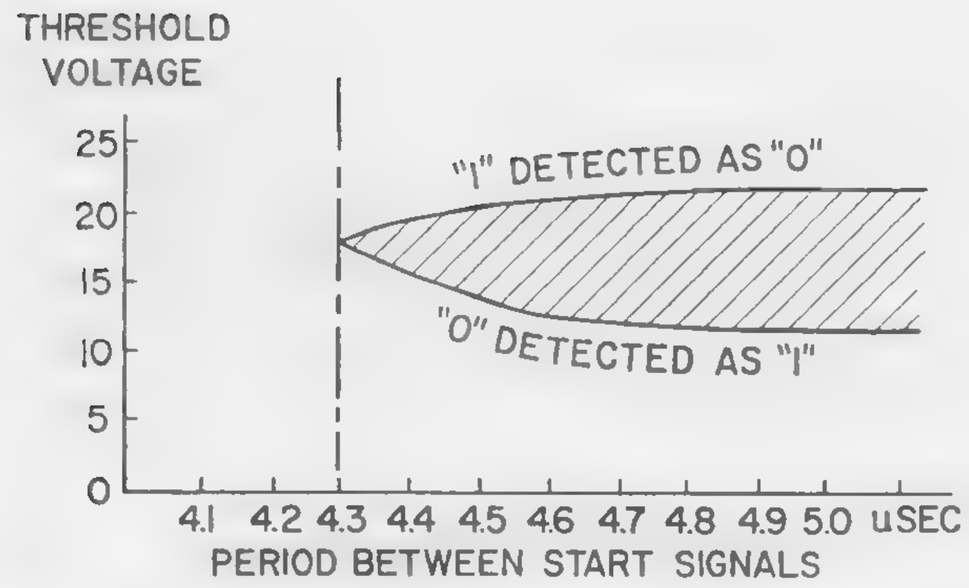



**Figure 6—Post-write transients which cause margins to degrade as cycle time is decreased.**

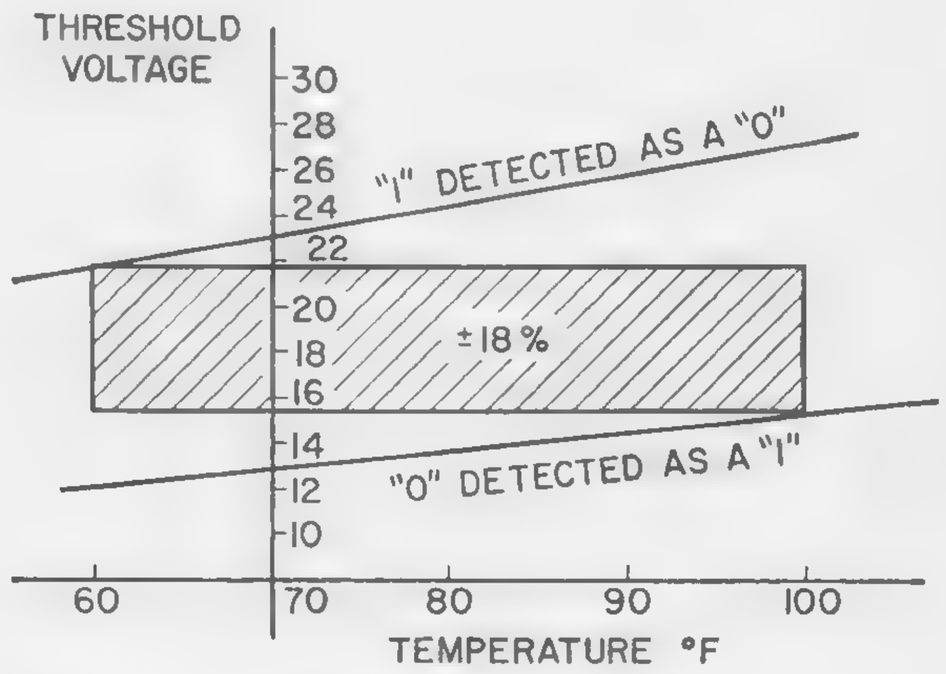



**Figure 7—The temperature characteristic of the store; it is linear and may be compensated with the threshold reference supply. The main contribution is from the biased core switch.**

## SESSION X: Storage

### 10.3: An Evaporated Film 135-Cryotron Memory Plane

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Kingston, N. Y.

THE 135-CRYOTRON memory plane to be described in this paper is the result of an investigation conducted to establish the requirements for fabricating, reproducing, and testing large numbers of interconnected cryotrons deposited on single substrates.

The thin film cryotron memory cell (Figure 1) is the unit-device basic to the entire *135*-cryotron plane. The memory cell shown is of the persistent current type, and contains *3* cryotrons. The film-width relationship of a single memory cell, to the entire plane, is shown in Figure 2. A cluster of memory cells on a plane is shown in Figure 3. A complete memory plane including input and output cryotrons is shown in Figure 4. This plane consists of 19 thin-film layers of lead, tin, and silicon monoxide, deposited in time-sequence through 17 masks.

A persistent current is set in the loop *CDEFC* (Figure 1) according to the following operating-sequence: (1) Apply $I_W$ to the *write* cryotron to hold the *write* gate normal; (2) apply information current $I_Z$ which will now have to go through branch *2* of the persistent current loop; (3) remove $I_W$—the information current $I_Z$ will now remain in branch *2* of the persistent current loop, even though the *write* gate is now superconductive; (4) remove information current $I_Z$.

The persistent current is destroyed in the loop by the application of $I_W$, causing the *write* cryotron to become resistive, while the information current $I_Z$ is zero in magnitude.

The presence or absence of a persistent current can be detected by monitoring the resistance between points *A* and *B* (Figure 1) while current $I_R$ is applied, thus causing the *read-out* cryotron to be resistive. When a persistent current is stored, the *read* cryotron is resistive (resistance appearing between points *A* and *B*). When a persistent current is not stored, the *read* cryotron is superconductive and there is no resistance between points *A* and *B*.

The memory is a word-oriented (*2*-dimensional) plane consisting of *8* word-registers with *5* bits-per-word, giving a total of *40* memory cells. Word-register selection is accomplished with room-temperature equipment. The *40* memory cells, with *3* cryotrons per cell, account for *120* (of the *135*) cryotrons. Ten cryotrons at the top of the substrate and also controlled by room temperature equipment are used in the logic operation of the memory; five biased in-line cryotrons at the bottom of the substrate produce the outputs when information is read out of the memory. The memory plane configuration permits register-to-register transfer within the memory itself, in addition to the conventional *read* and *write* instructions.

The *135*-cryotron thin film planes are fabricated in a 36-inch x 36-inch horizontally mounted stainless steel cylindrical vacuum tank. Each plane requires only one pump-down of the vacuum system; all evaporations occur at pressures approximating $10^{-7}$ *mm Hg*. Film thicknesses are automatically controlled by a rate-monitor which controls the rate of film deposition during a specific time interval.

Completed planes are fastened mechanically and electrically to a sample holder and are then placed in the liquid helium environment for testing.

Test data indicate successful fabrication techniques. Each plane tested contained the maximum of *40* operational memory cells: all *135* cryotrons comprising the memory cells and associated circuitry operated satisfactorily. Variation of cryotron characteristics across the planes, and from plane to plane, has not been significant. All memory planes can be interconnected to form one cryotron memory. The cells were also operated dynamically, and these tests were successful in all respects. Dynamic tests included a *write-read* memory cycle as well as a memory cycle to demonstrate the register-to-register transfer features of the memory. A listing of the critical controlling current magnitudes for the *read-out* cryotrons of a typical plane appear in Table 1.

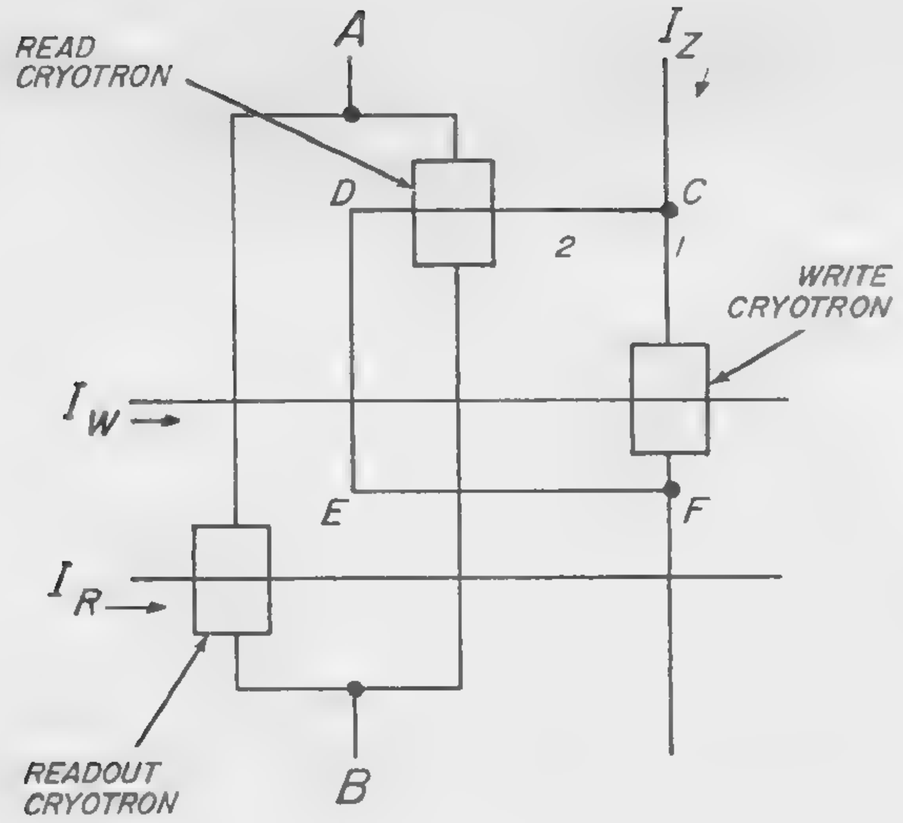



Figure 1—Schematic diagram of memory cell.

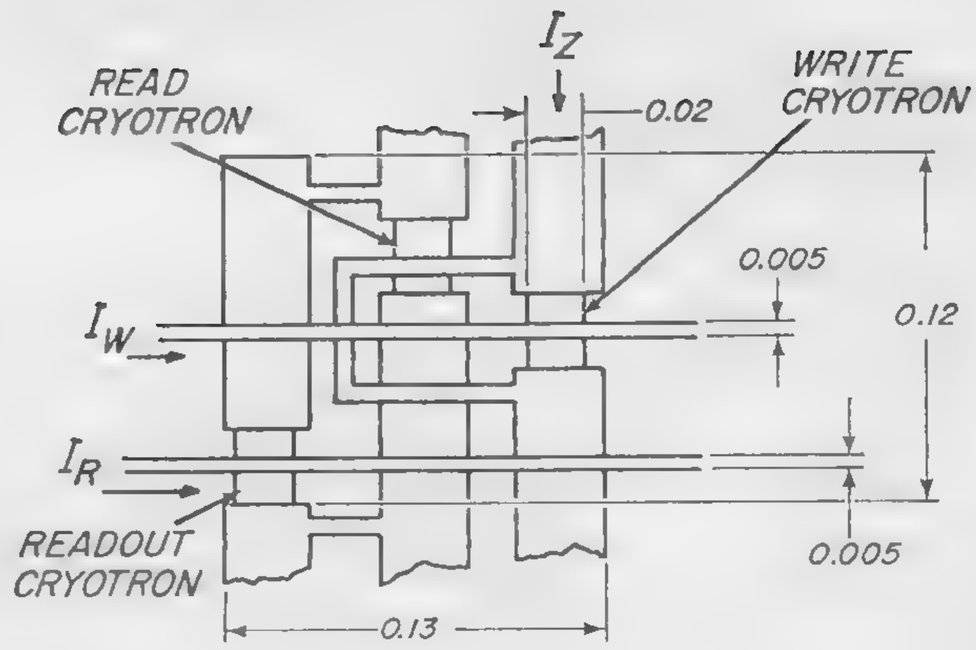



Figure 2—Wiring diagram of memory cell.

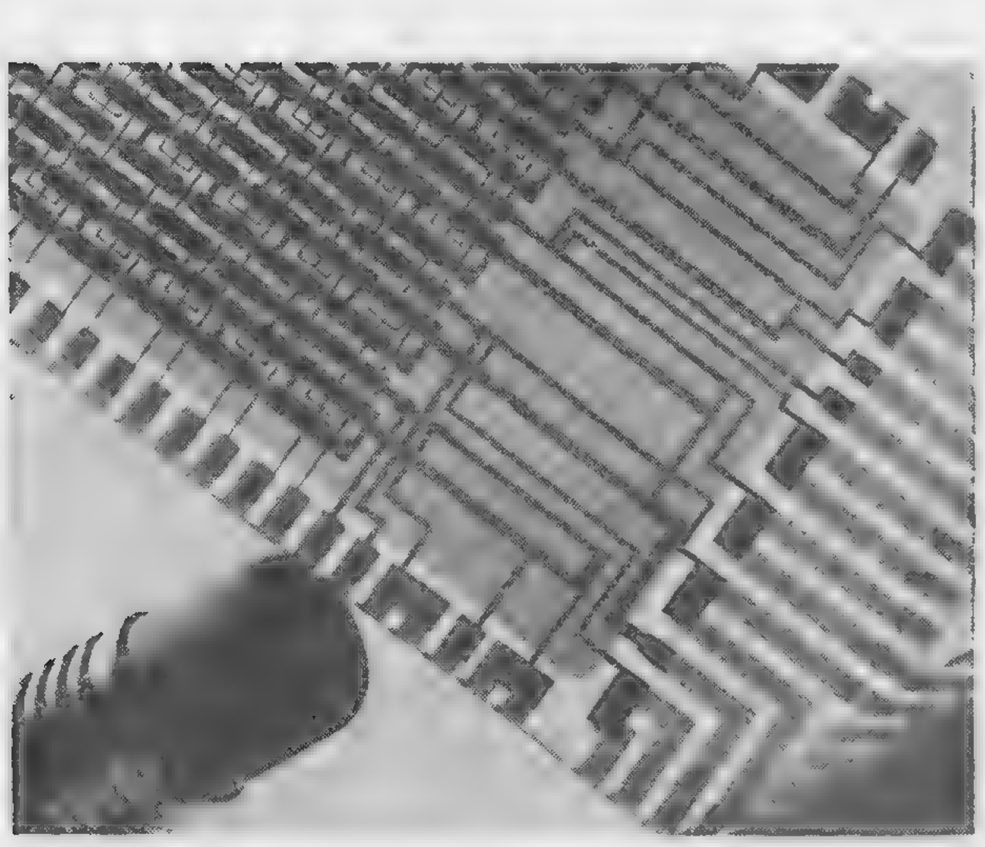


Figure 3—Closeup of memory cells on plane.

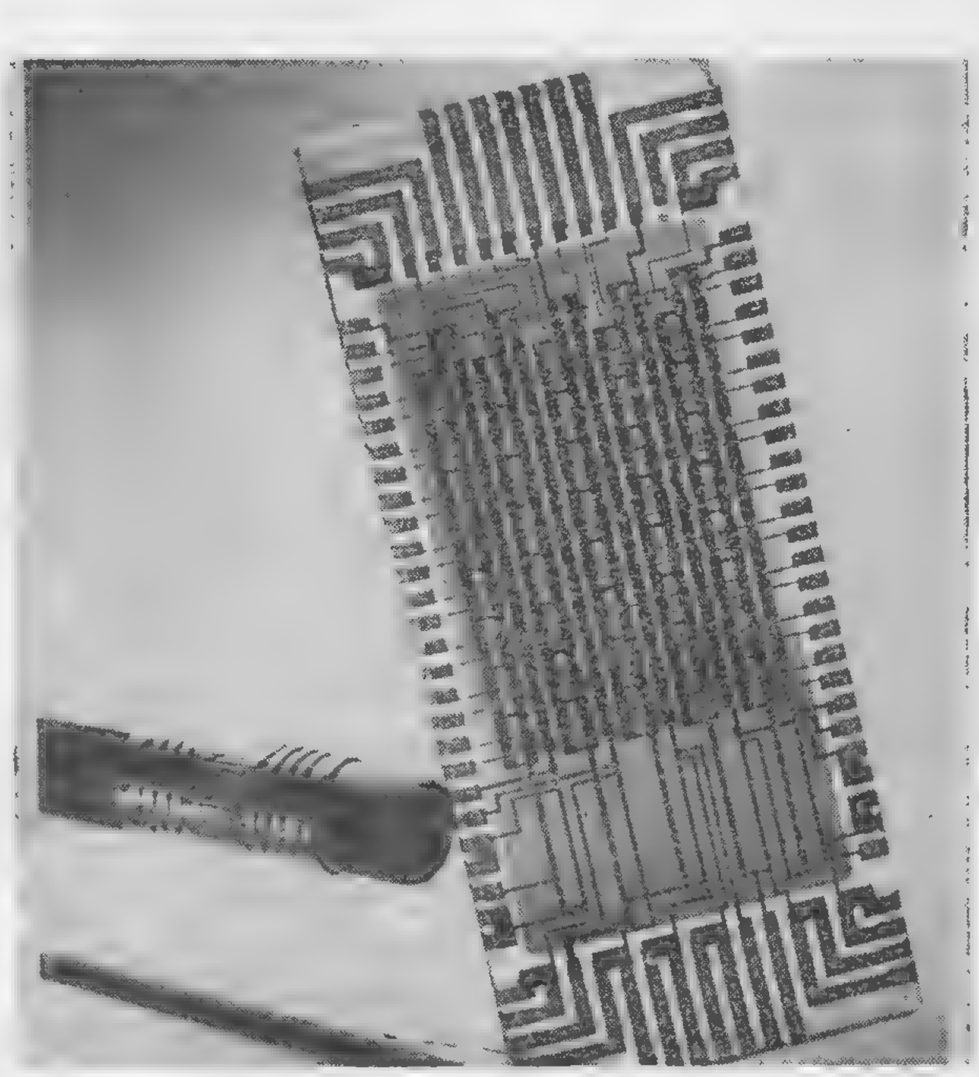


Figure 4 (right)—Complete plane: *135*-cryotron 40 memory cells.

BIT POSITION

| Word Register | A | B | C | D | E |
|---|---|---|---|---|---|
| 1 | 370 | 395 | 390 | 395 | 390 |
| 2 | 370 | 395 | 400 | 395 | 400 |
| 3 | 380 | 395 | 390 | 400 | 410 |
| 4 | 385 | 400 | 395 | 405 | 410 |
| 5 | 390 | 400 | 395 | 405 | 410 |
| 6 | 390 | 400 | 395 | 405 | 400 |
| 7 | 390 | 400 | 410 | 400 | 400 |
| 8 | 400 | 410 | 410 | 410 | 400 |

Table 1—Critical controlling currents (in milliamperes) of the readout cryotrons of a typical memory plane.

## SESSION X: Storage

### 10.4: A Coincident Current Superconductive Memory

L. L. Burns, G. A. Alphonse and G. W. Leck

RCA Laboratories

Princeton, N. J.

THE PHENOMENON OF SUPERCONDUCTIVITY and its related feature of exclusion of magnetic flux can be used advantageously for the storage of binary information in the form of persistent current in superconducting paths. An early practical version of a superconductive memory cell is illustrated in Figure 1. It operates on the basis that the current in the drive line causes a magnetic field to appear at the surface of the superconducting bridge between the two holes. The superconductor opposes the change of flux, but the latter will drive it to the normal state and penetrate it if its magnitude is larger than the *critical field* of the superconductor at the temperature of operation. After resumption of the superconducting state, a flux is trapped around the superconducting bridge and sustains a persistent current in it. The direction of the persistent current can be reversed by changing the polarity of the drive current. A voltage is induced in the sense winding each time the drive flux penetrates the memory plane and links the sense winding.

Ideally a cell of this type is suitable for use in a large capacity memory system, but it exhibits a severe lack of reproducibility due to non-uniformity and ragged edges around the holes. In this treatment, this is resolved by completely eliminating the holes in the memory plane. The memory plane now consists of a continuous superconducting plane in which normal regions are maintained by the flux of the stored persistent currient. The normal regions thus created have exactly the same effect as the holes in the previously described type of memory. For a given material with a certain amount of stored flux the size of the normal areas is a function of the critical field of the material. The persistent current thus circulates in the superconducting regions surrounding two circular normal areas. These areas, located at the places indicated by the two dots and the two crosses shown in Figure 2, illustrate a coincident current continuous memory cell. The storage process is analyzed in detail in Figure 3 where the fields of the drive pulses add up vectorially to destroy super-conductivity in the plane at the intersection of the drive lines. The field is also shown to be *locked* around an artificial superconducting bridge carrying the persistent current which represents the stored information.

Figure 4 illustrates a typical read-write cycle. The large pulse sets up the initial persistent current, the pulses of amplitude equal to $0.6\ I_c$ represent the net drive pulses, and the $0.3\ I_c$ pulses are the half-select signals which alone have no effect on the stored information and cause no output signal. An experimental *100*-bit memory plane appears in Figure 5, and an oscillogram of a 6-microsecond test cycle together with the corresponding sense output is shown in Figure 6. A small amount of stray pickup due to improper grounding also appears as part of the sense output.

The material used for the drive lines is lead (*Pb*) and the material for the memory plane is tin (*Sn*). Lead becomes superconducting at $7.2°K$ and can carry large currents at the temperature of operation ($3.6°K$) without becoming resistive. Since tin is superconducting at $3.7°K$ it requires only a relatively small magnetic field for its operation as a memory device. The total required drive current is approximately 300 ma. The cells have a very high packing density, and they are capable of very fast operation (storage times as short as one nanosecond have been observed). Figure 1 is an expanded view of the multilayer memory.

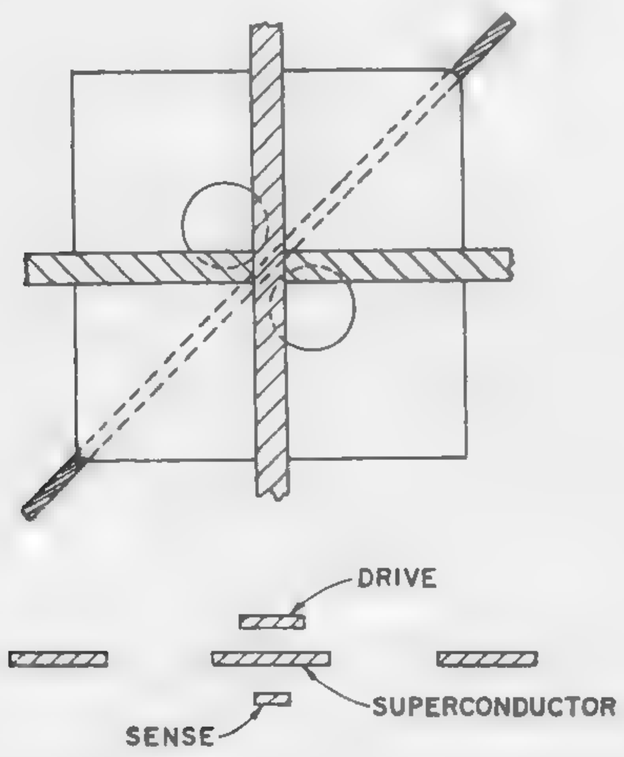



Figure 1—Two-hole persistent current memory cell.

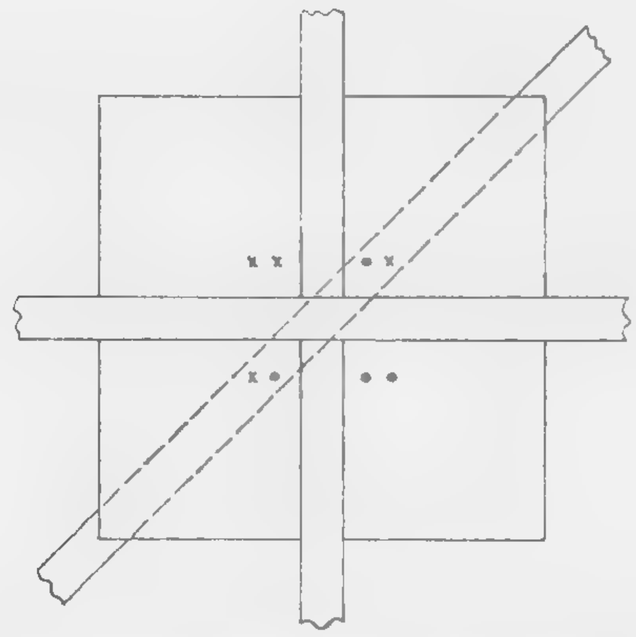
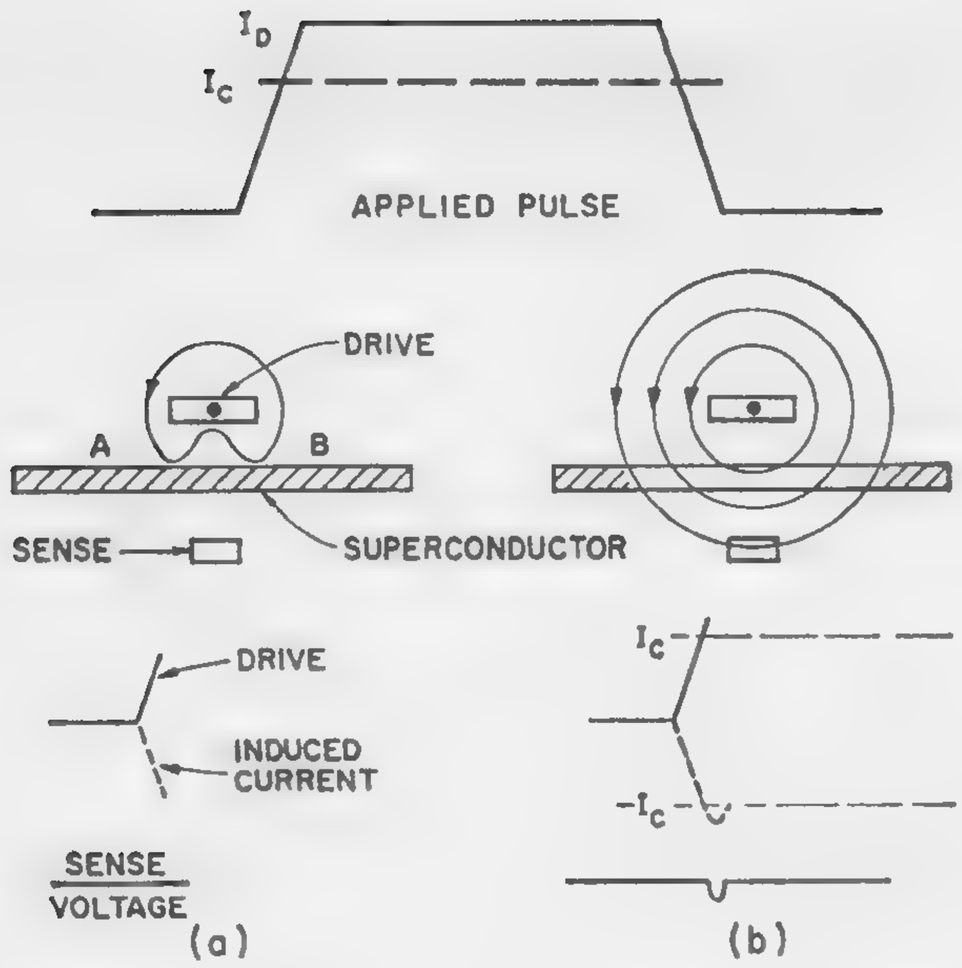
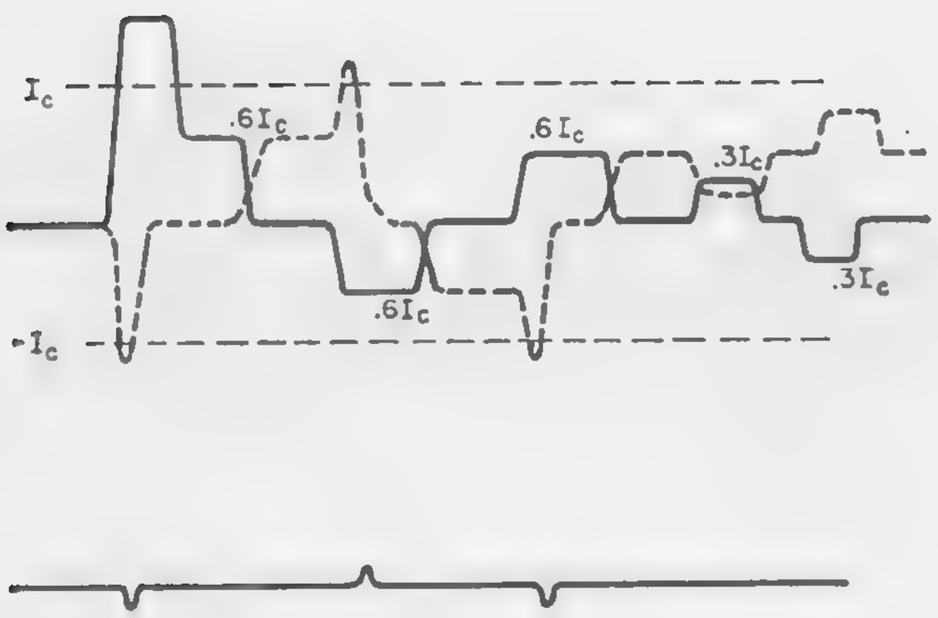


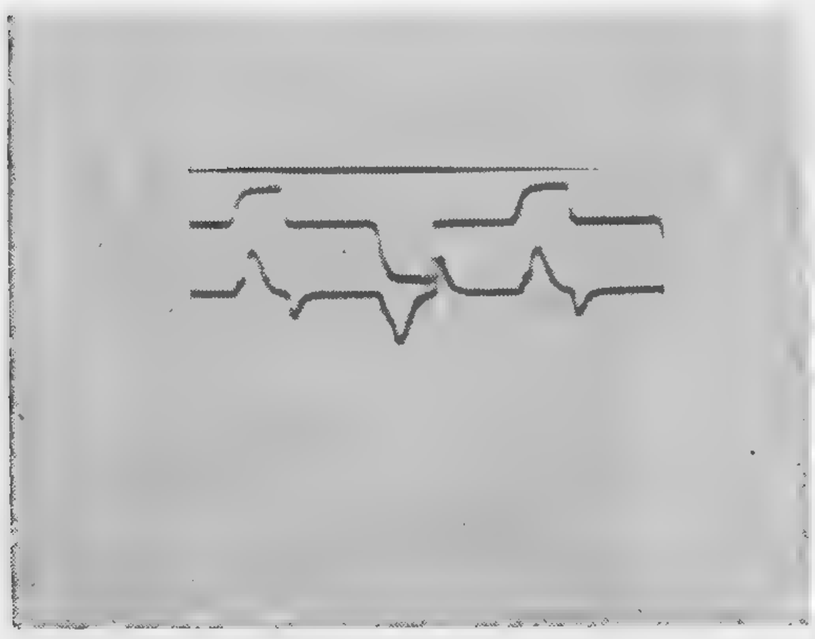
Figure 2—Continuous sheet coincident current memory.



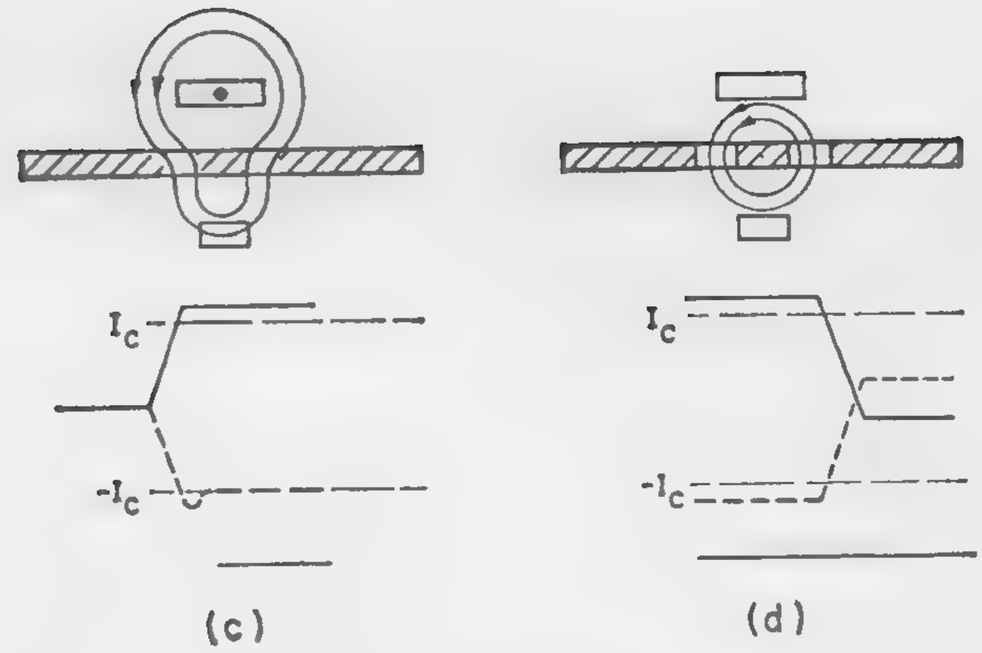

*(Above)*
**Figure 4—Typical read-write cycle.**

*(Right)*
**Figure 5—Experimental 100-bit memory of the continuous sheet type.**

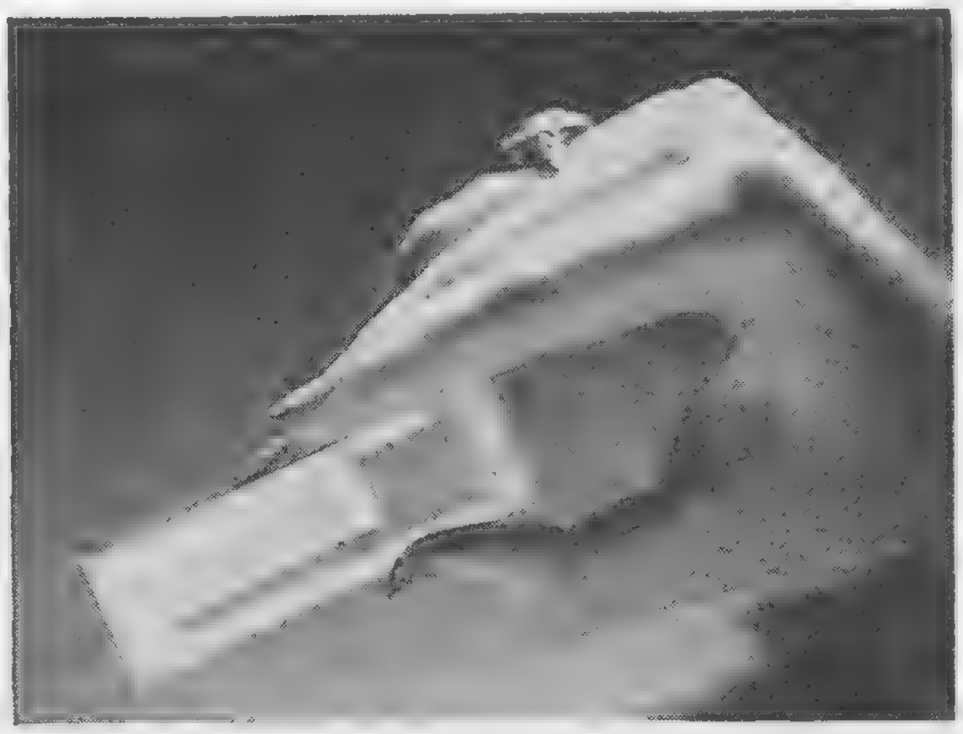


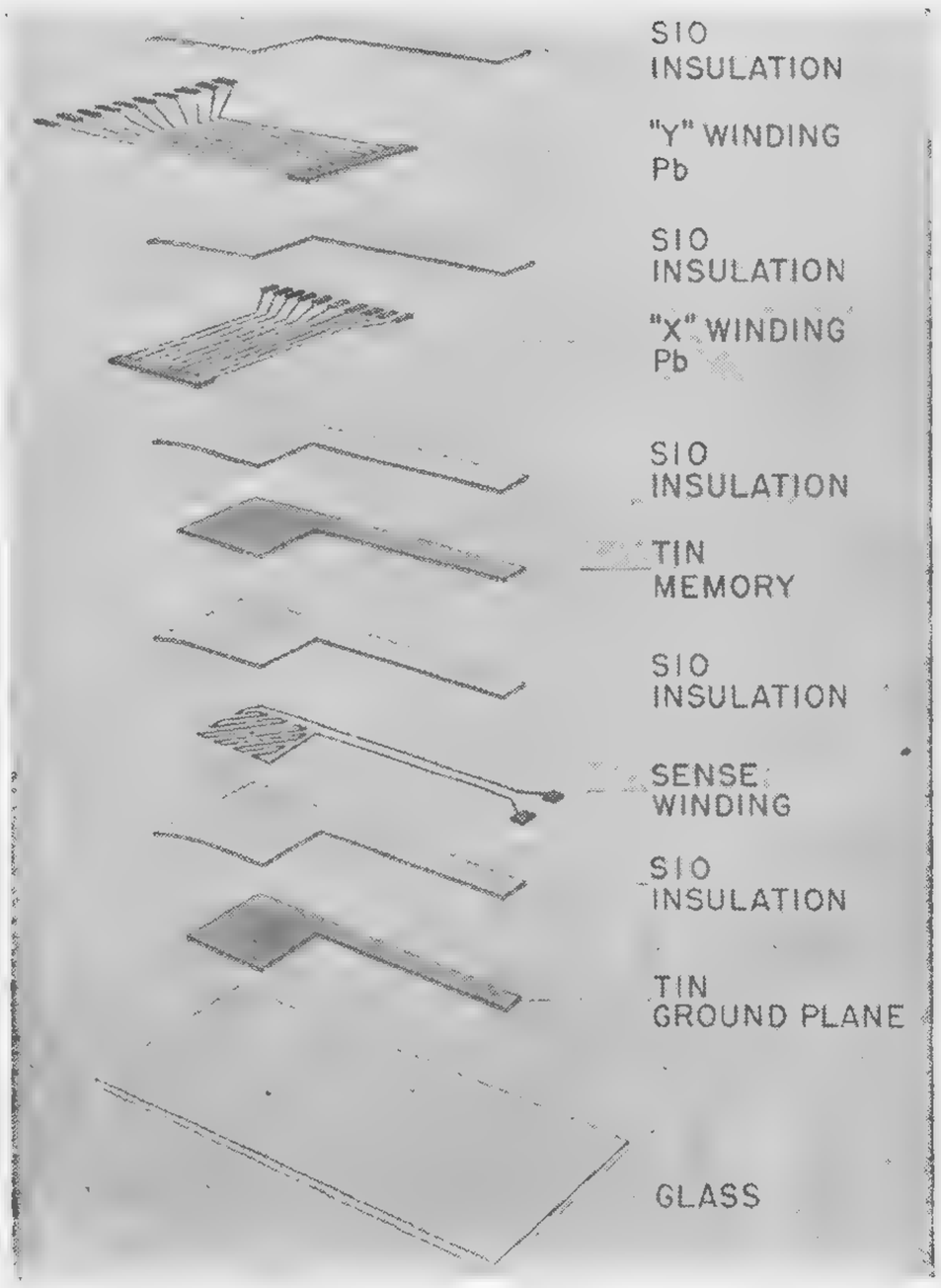
*(Above)*
**Figure 6—Oscillogram of a 6 μsec read-write cycle and corresponding sense output.**

*(Right)*
**Figure 7—Expanded view of a multi-layer continuous sheet memory.**




*(Left, Above)*
**Figure 3—Detail of persistent current storage in continuous sheet memory.**





## SESSION X: Storage

### 10.5: High-Speed Tunnel-Diode Memory

**D. L. Berry and E. A. Fisch**

Electronics Lab., General Electric Company

Syracuse, N. Y.

THE HIGH SWITCHING SPEED OF TUNNEL DIODES has allowed the construction of a non-destructively read random access memory with read and write cycle times of twenty nanoseconds each. The memory consists of twenty words of fifty bits each.

The memory is word organized with parallel readin and readout; Figure 1. Word selection is performed by an external address logic. Logic output is routed to the proper control generator through function enable gates. The memory is read non-destructively and requires both read control and strobe pulses. Writing involves resetting all the elements in a word and generating the write control and write pulses for inserting new information. The write signal generators are triggered from the input register at a time controlled by the write enable signal.

The memory is synchronized to the external circuitry, although certain internal processes are asynchronous; consequently timing is important. The memory timing is illustrated in Figure 2. A function enable signal initiates each cycle of operation. This signal opens the appropriate input gates on the control generators and triggers either the strobe or write generators.

*Use of Tapped Transmission Line*

The read-control pulse is applied to the memory elements by a tapped transmission line. This line has a certain propagation delay so that all the bits of a word are not readout simultaneously. Compensation is provided in the sense amplifier by adding delay between the amplifiers and strobe gates so that all signals reach the strobe gates simultaneously. The strobe gate eliminates writing noise and reclocks the signal before it enters the output register. The total time between the start of the read enable pulse and the time when the output of the strobe gates is available is twenty-five nanoseconds; however, this does not interfere with the next cycle of operation since the information is in the sense amplifiers or delay lines.

Writing requires that all the elements of the word be reset to zero. The write generators corresponding to the ONES to be written are triggered and in conjunction with the write control pulse serve to switch the appropriate elements.

*Single Diode Threshold Circuit*

A single-diode threshold circuit theoretically would serve as a memory element, but with practical diode and component tolerances it was not possible to use this circuit in the non-destructively read memory. The circuit shown in Figure 3 was used to provide a uniform one-zero ratio[1]. The circuit operation is quite similar to that of the single diode circuit, but the output is derived from comparing the dynamic impedances of the two diodes.

A memory element was exercised using a pattern of *five on, five off* for the reset and write control pulses and *two on, two off* for the write pulses. The output of the memory element itself is shown in Figure 4. The *dc* level change as a function of stored information is apparent. The processed output of the strobe circuit is shown in Figure 5.

The most pressing need is to increase the size of the array. The size is presently limited by the attenuation of the output signal. This attenuation is directly proportional to the number of words connected in parallel. To date, the limit is around twenty words for this memory. In addition, further improvements in speed appear possible.

The tunnel diode memory appears to be most useful as a small, high-speed buffer memory.

[1] Chow, W. F., *7th Annual Symposium on Computers and Data Processing;* July, 1960.

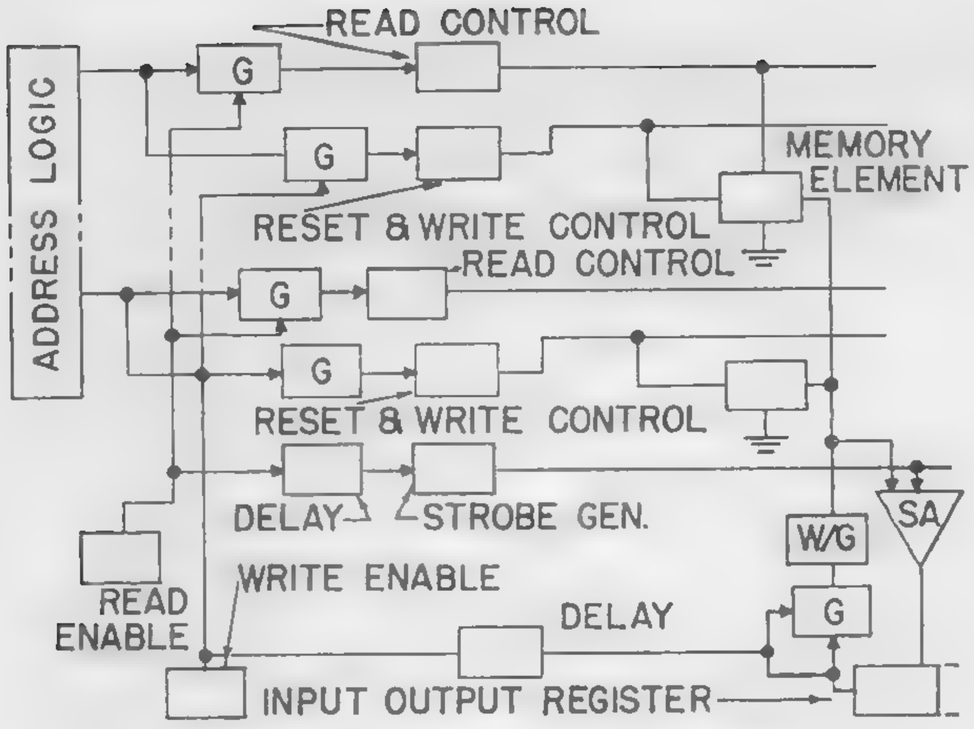



Figure 1—Memory block diagram.

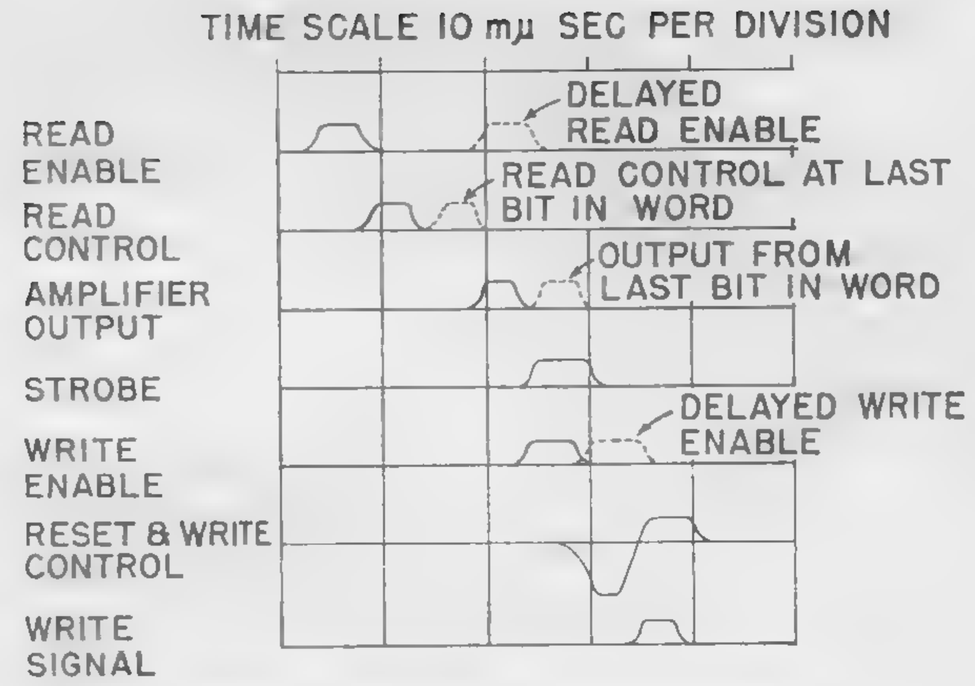
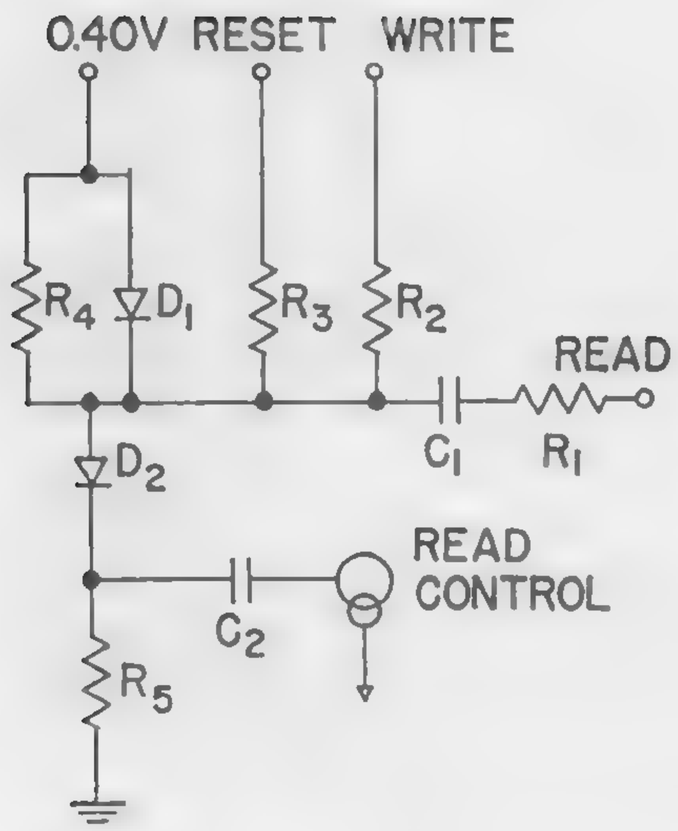



Figure 2—Memory timing diagram.




$R_1$ = 200
$R_2$ = 8.0K
$R_3$ = 5.0K
$R_4$ = 1.2K
$R_5$ = 30
$C_1$ = 20 μμf
C = 12 μμf

Figure 3—Basic memory element.

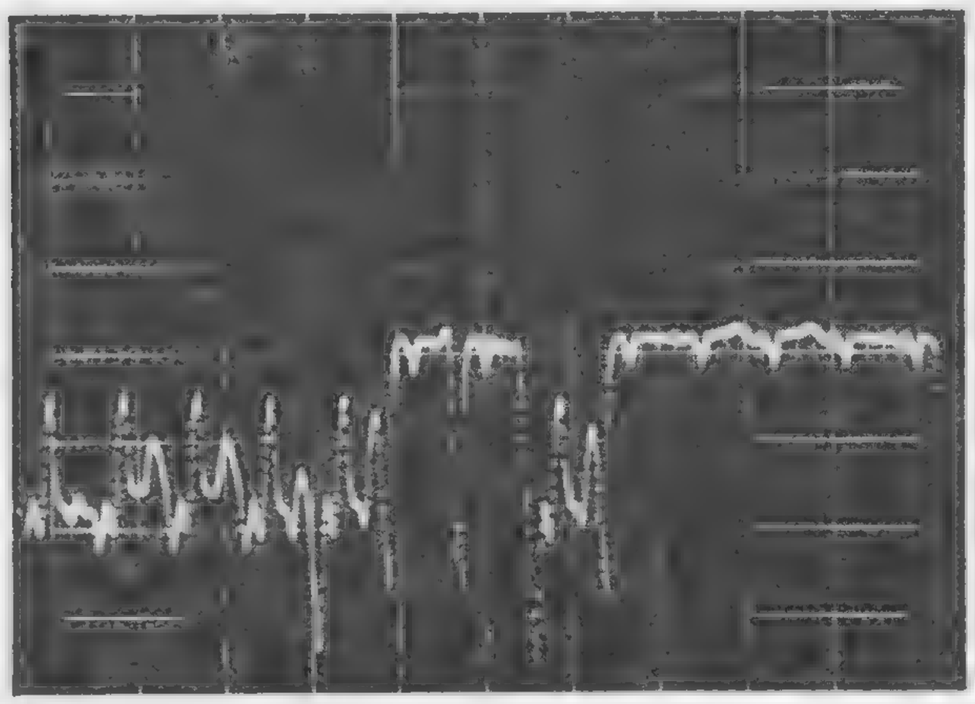


Figure 4—Output signal as read at memory element *0.2 v/div;* vertically *50 nsec/div.*

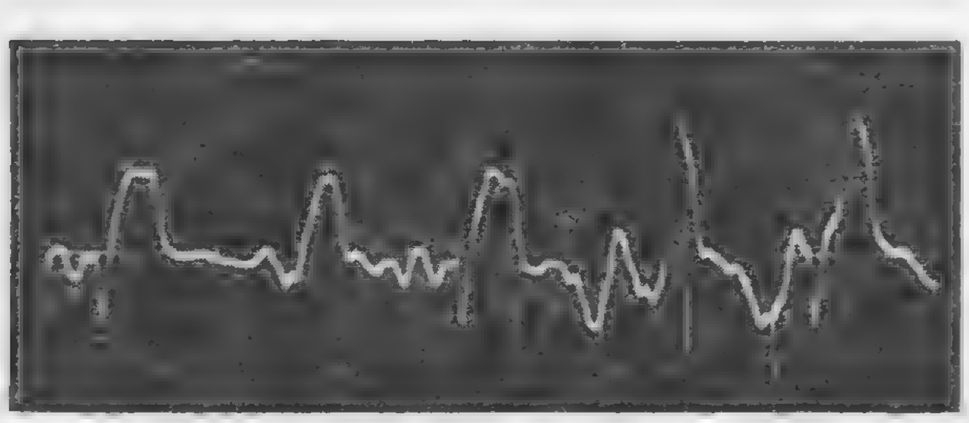


Figure 5—Output of strobe circuit; three *ZEROS* and two *ONES*—0.1 *v/div,* vertically 20 *nsec/div.*

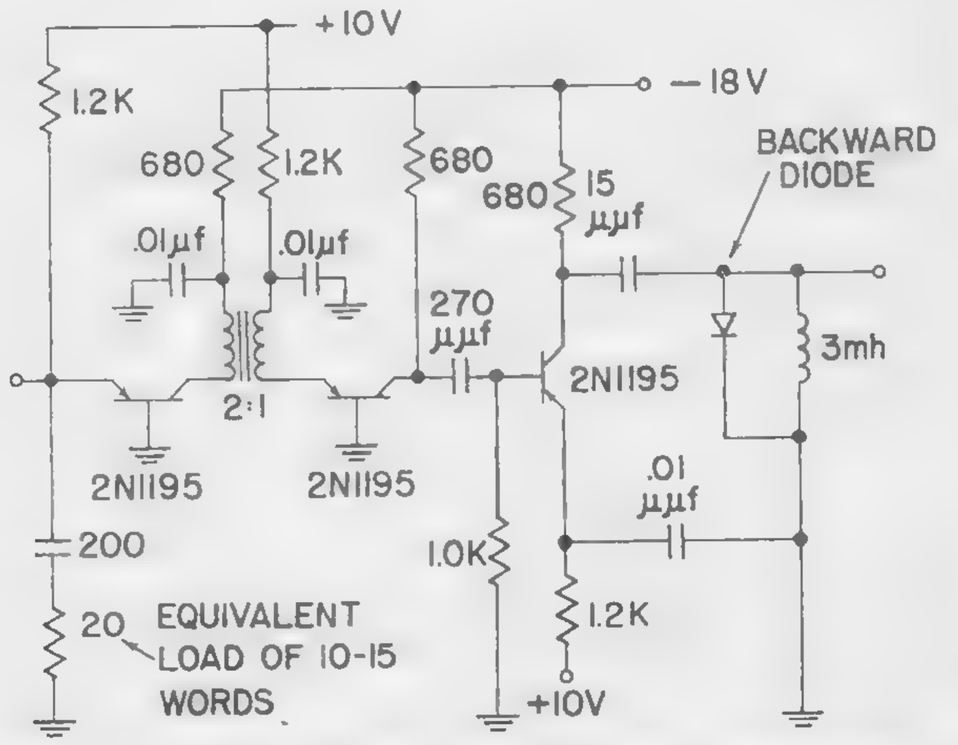



Figure 6—Sense amplifier circuit. This sense amplifier has a bandwidth of 2—150 *Mc* and a gain of 21 *db*. The delayed output of the amplifier is fed into the strobe gate.

## Notes

## Notes

## Scope of Conference

THE 1961 INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE features ten sessions at the University of Pennsylvania (Irvine Auditorium and University Museum) devoted to the broad advances in the field of solid-state device applications and circuits. Fifty-one papers covering new device characteristics, microwave amplifiers and applications, logic, computer magnetics, power and control, storage, communication circuits and techniques, and new technologies will be offered.

TWELVE INFORMAL SESSIONS, conducted by international leaders in the solid-state field, will be held on Wednesday and Thursday evenings in the Sheraton Hotel to provide registrants an opportunity to discuss the latest developments in the art. Among the topics on the agenda are tunnel diodes, micro-power circuit operation, new logic techniques, reliability, microwave applications, power conversion and controls. Additional subjects include low-frequency/low-signal amplification, microelectronics, high-frequency measurements and characterization, access and storage techniques, and solid state optical masers.

## Conference Digest of Technical Papers

ADDITIONAL COPIES of the DIGEST OF TECHNICAL PAPERS, priced at $5.00 per copy, may be obtained from H. G. Sparks, The Moore School of Electrical Engineering, University of Pennsylvania, 200 South 33 St., Philadelphia 4, Pa. Remittance (payable in U. S. currency) should be made to the order of: Solid-State Circuits Conference.

## Conference—Informal Session Locations

THE CONFERENCE is being held on the campus of the University of Pennsylvania in the Irvine Auditorium and in the University Museum.

IRVINE AUDITORIUM is located at the northwest corner of 34th and Spruce Streets, the University Museum is just east of the southeast corner of 34th and Spruce Streets, Philadelphia, Pennsylvania. Central Philadelphia can be reached by bus route 42 and the 30th Street station of the Pennsylvania Railroad is less than a mile from the University Campus.

THE INFORMAL Wednesday-Thursday evening sessions will be held in the Sheraton Hotel, 1725 Pennsylvania Boulevard, in central Philadelphia.

## Luncheons . . . Open-House Cocktail Hours

LUNCHEONS on Wednesday, Thursday and Friday will be served to a limited number in the University Museum, University of Pennsylvania.

OPEN-HOUSE COCKTAIL HOURS will be held on Wednesday and Thursday evenings (6:00-7:30 P.M.) in the Independence-Constitution Rooms of the Sheraton Hotel.

## Conference Fees

| | | |
|---|---|---|
| Registration— | Member AIEE or IRE: | $12.00 |
| | Non-Member: | 14.00 |
| | Wednesday Lunch: | 3.50 |
| | Thursday Lunch: | 3.50 |
| | Friday Lunch: | 3.50 |

Full-time students will be registered free-of-charge for all technical sessions.

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